Body-Tied Germanium FinFETs Directly on a Silicon Substrate

Che-Wei Chen, Cheng-Ting Chung, Guang-Li Luo, and Chao-Hsin Chien

Abstract—We fabricated body-tied Ge p-channel fin field-effect transistors (p-FinFETs) directly on a Si substrate with a high-κ/metal gate stack. This scheme is fully compatible with Si standard processing. The FinFET structure has excellent control on the channel potential and thus can improve the short-channel effect. The diode with p^+-Ge/n-Si heterojunctions illustrates a remarkably high $I_{ON}/I_{OFF} > 10^6$ despite the presence of misfit dislocations at the interface. The high-hole-mobility body-tied Ge p-FinFETs with a fin width W_{Fin} of $\sim$40 nm and a mask channel length L_{Mask} of 120 nm depict a driving current of 22 $\mu A/\mu m$ at $V_G = -2$ V and a low OFF-current of 3 nA/μm at $V_G = 2$ V. The subthreshold characteristics with a swing of 228 mV/dec and drain-induced barrier lowering of 288 mV/V are demonstrated.

Index Terms—Body-tied fin field-effect transistors (FinFETs), germanium, heterojunctions, high-mobility channel.

I. INTRODUCTION

THE high-mobility Ge p-channel metal–oxide–semiconductor field-effect transistor (pMOSFET) has been demonstrated as one of the possible candidates for continuously keeping up with the pace of device scaling [1]–[3]. Due to the excellent drive current and integration friendliness to the Si substrate, Ge pMOSFETs are viable for future high-speed digital-logic applications [4]–[7]. Moreover, the nonplanar fin field-effect transistor (FinFET) is an attractive replacement for the conventional planar transistor since it has better electrostatic integrity and is preferable for the ultrasmall devices [8]–[10]. To use the FinFETs for several technology nodes, there is a strong need to enhance the performance of the device with a high-mobility channel [11], [12]. However, the body-tied Ge p-channel FinFETs (p-FinFETs) have not been directly fabricated on the Si substrate yet.

In this letter, a lightly doped Ge film with low dislocation density was directly grown on an n-Si substrate channel material since we think the heteroepitaxial scheme is better

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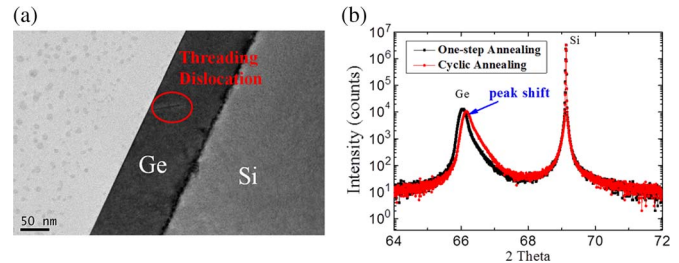Digital Object Identifier 10.1109/LED.2012.2217473

Fig. 1. (a) TEM image of a very low threading dislocation in the 120-nm blanket Ge film on the Si substrate with one-step annealing. (b) XRD of Ge on Si with one-step and cyclic annealing.

suited for the large size of the Si wafer. We find that a diode with a p^+-Ge/n-Si heterojunction exhibited a relatively high $I_{ON}/I_{OFF} > 10^6$ despite the presence of misfit dislocations at the Ge/Si interface caused by a 4.2% lattice mismatch. The body-tied Ge p-FinFET with a fin width W_{Fin} of $\sim$40 nm and a mask channel length L_{Mask} of 120 nm depicted a driving current of 22 $\mu A/\mu m$ and a remarkably low OFF-current of 3 nA/μm.

II. DEVICE FABRICATION

The lightly doped Ge film was grown on an n-Si (100) substrate using an ultrahigh vacuum chemical vapor deposition system after standard cleaning. After Ge deposition, the chamber temperature was raised to 900 °C annealing for 10 min (one-step annealing). Fig. 1(a) shows the cross-sectional transmission electron microscopy (TEM) image with a low threading dislocation for 120-nm blanket Ge on the Si substrate. We can see that 900 °C annealing is able to effectively reduce the threading dislocation density and improve single-crystalline Ge film quality [13]. In order to reduce threading dislocation density further, we also employed cyclic annealing through ten cycles of raising the temperature to 900 °C and then cooling it down to 420 °C over 10 min and then reheating to 900 °C and repeating the process through ten cycles [13]. In the X-ray diffraction (XRD) pattern, as shown in Fig. 1(b), we see that the position of the Ge peak shifted toward that of the Si peak, and the full-width at half-maximum [14] became more broad. These results imply the formation of a SiGe alloy at the interface by using cyclic annealing.

Active area was defined using electron-beam lithography. Boron ions were implanted (20 keV, 1×10^{15} cm^{-2}) in the source/drain region. Dopant activation was performed at 500 °C for 10 s in nitrogen ambient. After the Ge fin was patterned by lithography, the Ge fin was formed by using reactive ion etching (RIE) anisotropic etching in Cl$_2$/HBr ambient. In addition,
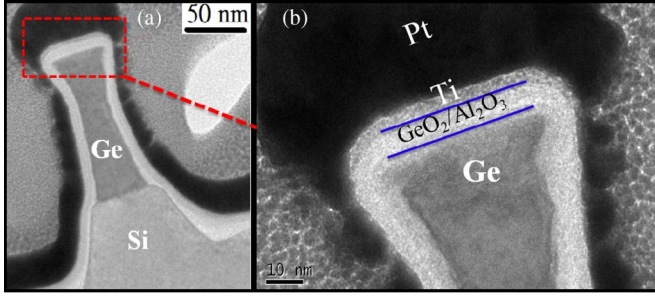
Fig. 2. (a) TEM image of the cross section of the Ge fin structure with GeO_2/Al_2O_3 and a Ti/Pt metal gate stack. (b) The gate stack structure can be clearly observed. The thickness of the GeO_2 layer is about 3 nm, and the thickness of the Al_2O_3 layer is about 5 nm.

Fig. 3. (a) $I–V$ characteristic of the p^+-Ge/n-Si heterojunction with $I_{ON}/I_{OFF} > 10^6$. (Inset) Schematic cross-sectional diagram of the Ge p-FinFET. (b) $I_{DS}–V_G$ transfer characteristic of the Ge p-FinFET with an L_{Mask} of 120 nm and a W_{Fin} of 40 nm. (c) $I_{DS}–V_{DS}$ output characteristic of the Ge p-FinFET with EOT ~4.9 nm. (d) S.S. and DIBL of the Ge p-FinFET with a W_{Fin} of 40 nm versus L_{Mask} of 120–1000 nm.

it should be noted that the Si substrate might be etched by Cl_2/HBr, too. The spin-on-glass was coated and etched back for the device isolation. The GeO_2 surface passivation using rapid thermal oxidation at 520 °C for 30 s and then atomic layer deposition (ALD) Al_2O_3 high-κ dielectric deposition was carried out after removing native oxide. The metal gate Ti (5 nm)/ Pt (100 nm) was deposited by sputtering. Finally, the low-resistance Ti (5 nm)/Pt (50 nm) contact metal was defined by the liftoff process and forming gas annealing at 300 °C for 30 min. The different L_{Mask} from 1 μm to 120 nm were fabricated.

III. RESULTS AND DISCUSSION

Fig. 2(a) shows the cross-sectional TEM image of the Ge p-FinFET with GeO_2/Al_2O_3 and a Ti/Pt metal gate stack. The Ge fin has a W_{Fin} of about 40 nm and an H_{Fin} of 120 nm. Fig. 2(b) clearly shows the gate stack structure. The thickness of the GeO_2 layer was about 3 nm, and the thickness of the Al_2O_3 layer was about 5 nm.

Fig. 3(a) shows the $I–V$ characteristic of the p^+-Ge/n-Si heterojunction with $I_{ON}/I_{OFF} > 10^6$. A schematic cross-sectional view of the Ge p-FinFET is shown in the inset in Fig. 3(a). Leakage current density J_R is 6.8×10^{-5} A/cm^2 at -1 V. The value of J_R is remarkably low, although lots of misfit dislocations have been clearly observed at the Ge/Si interface. This result is very exciting since the dislocations may make the leakage current at the drain be intolerable via generation. Although we do not know the exact reason for such a low leakage current level right now, we think there are two possible origins: First, the energy level of the misfit dislocation is not located at and/or near the middle of the band gap, and then, the generation and recombination is not so efficient. Second, the hole concentration in Si is much lower than that in Ge [15]. Fig. 3(b) shows the $I_{DS}–V_G$ transfer characteristic of the Ge p-FinFET with an L_{Mask} of 120 nm and a W_{Fin} of 40 nm in the linear region at $V_{DS} = 0.1$ V and in the saturation region at $V_{DS} = 1$ V. The total effective channel width ($W_{Eff} = 2 \times H_{Fin} + W_{Fin}$) was equal to 284 nm [16]. Drain current I_{DS} was normalized by W_{Eff}. The subthreshold characteristic with subthreshold swing (S.S.) was 228 mV/dec. With the surface passivation scheme, we believe that the value of S.S. can be significantly reduced. Drain-induced barrier lowering
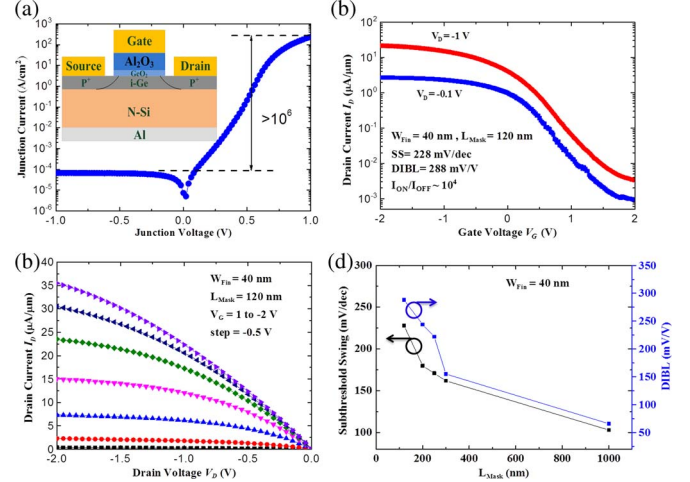
(DIBL) was 288 mV/V. This suggests that the equivalent oxide thickness (EOT) of 4.9 nm of the gate oxide is too thick and the channel dopant concentration is too low. We believe that further EOT reduction and increasing channel dopant concentration can effectively lessen DIBL. The I_{ON}/I_{OFF} ratio was ~10^4. For the Ge p-FinFET on the Si substrate, the I_{ON}/I_{OFF} ratio of ~10^3 has been reported in [7] based on the rapid melting growth. Recently, a study [17] has used epitaxial Ge on the silicon on insulator (SOI) substrate for a p-FinFET, and the reported ratio was ~2×10^4. One can see that the gate-induced drain leakage current was considerably large, particularly at $V_G = 2$ V ($I_{OFF} > 100$ $nA/\mu m$), in their device. Moreover, the S.S. value was 350 mV/dec. Our device ($L_{Mask} = 120$ nm) not only was much smaller than that ($L_g = 200$ nm) in [17] but also depicted a much steeper subthreshold slope. Due to the extremely low junction leakage of the p^+-Ge/n-Si heterojunction and low gate leakage (3.5 $pA/\mu m$ at $V_G = 2$ V), the OFF-state leakage current was as low as 3 $nA/\mu m$ at $V_G = 2$ V. More importantly, our device structure is a Ge body-tied FinFET, which is much preferred from the viewpoint of low cost. Threshold voltage $V_{T(lin)}$ was 0.47 V in the linear regime, and $V_{T(sat)}$ was 0.27 V in the saturation regime, which were determined by the linear extrapolation technique [18]. Certainly, these are not the required values for the high-performance circuit operation. We think V_T can be significantly shifted toward the anticipated value by adjusting the gate work function and the substrate doping profile. Fig. 3(c) shows the $I_{DS}–V_{DS}$ output characteristic of the Ge p-FinFET. The saturation current is 35 $\mu A/cm^2$ at V_{DS} and $V_{GS} = -2$ V. Both DIBL reduction and enhancement of saturation current can be also achieved through reducing EOT. Fig. 3(d) shows the S.S. and DIBL as a function of L_{Mask}. We find that the values of the S.S. and DIBL of the device are acceptable for the small devices. Therefore, we demonstrated the short-channel Ge p-FinFETs directly on the Si substrate with reasonable S.S. and DIBL with a fully Si-CMOS-compatible scheme.

IV. CONCLUSION

In conclusion, nonplanar body-tied Ge p-FinFETs directly on the Si substrate with a high-κ/metal gate stack have been fabricated using the top-down method. The short-mask-channel-length 120-nm Ge p-FinFET device with S.S. $= 228$ mV/dec and DIBL $= 288$ mV/V shows the short-channel effect, which can be improved. It also depicts a driving current of 22 μA/μm at $V_G = -2$ V and an OFF-state current of 3 nA/μm at $V_G = 2$ V. The device performance can be further improved by reducing EOT and germanide formation. We think our work can shed some light on future applications of the Ge p-FinFET for the high-performance logic circuit on a large-diameter Si wafer.

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