A 0.09 μW Low Power Front-End Biopotential Amplifier for Biosignal Recording

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***Abstract*—This work presents a biopotential front-end amplifier in which the MOS transistors are biased in subthreshold region with a supply voltage and current of 0.4–0.8 V and 0.23–1.86 μA, respectively, to reduce the system power. Flicker noise is then removed using a chopping technique, and differential interference produced by electrode impedance imbalance is suppressed using a Gm-C filter. Additionally, the circuit is fabricated using TSMC 0.18 μm CMOS technology with a core area of 0.77 $\times$ 0.36 mm^2. With a minimum supply voltage of 0.4 V, the measured SNR and power consumption of the proposed IC chip are 54.1 dB and 0.09μW, respectively.**

***Index Terms*—Biopotential recording, chopper amplifier, flicker noise, instrumentation amplifier.**

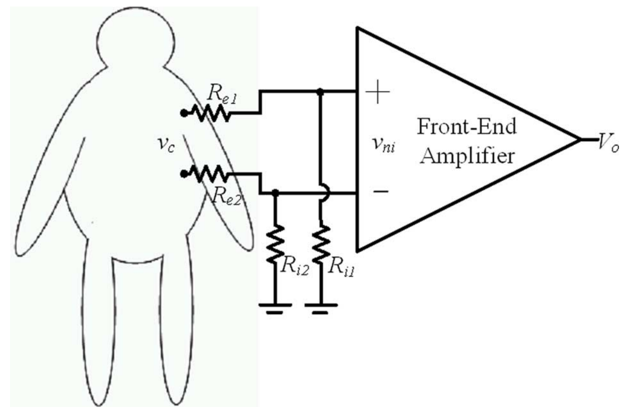

Fig. 1. A simplified circuit model of the biotelemetry system.

I. Introduction

Integrated circuit (IC) design has increasingly focused on lower power consumption, lower voltage and miniaturized size, contributing to the development of biomedical device [1]–[12]. Reducing the area diminishes the size and weight of electronic devices, making it more user-friendly. Low voltage and low power dissipation are essential to increasing battery lifetime in electronic devices. However, low power and low voltage correspond to poor noise immunity, especially when the device includes analogue circuitry. An important source of noise encountered in low-power and low-voltage biomedical devices is flicker (or $1/f$) noise, which is associated with the circuitry of an operational amplifier (OPAMP) [13], [14].

Beside the flicker noise, the biotelemetry systems based on biosignal recording, including ECG, EEG, and EMG, also incur severe electrical interferences, owing to its lack of a ground electrode. Fig. 1 illustrates a simplified circuit model of the biotelemetry system. Where R_{e1} and R_{e2} denote the electrode resistors, R_{i1} and R_{i2} represent the input resistances of a front-end amplifier constructed by an instrumentation amplifier (IA). Interference v_{ni} [15]–[18] at the input of the front-end amplifier for biotelemetry recording is simplified as

$$v_{ni} = v_c\left(\frac{1}{\text{CMRR}} + \frac{\Delta R}{Z_c}\right),$$
$$\Delta R = |R_{e1} - R_{e2}|, Z_c = \frac{R_{i1}+R_{i2}}{2}. \quad (1)$$

Where v_c refers to the common mode noise, mainly including static charge of the human body and 60 Hz noise from the power line. CMRR is the common mode rejection ratio of the front-end amplifier. Where ΔR and Z_c denote the difference impedance between two input electrodes and the common mode input impedance of the front-end amplifier. Interference v_{ni} of the IA includes the common and differential mode interference represented by the first and second terms of (1), respectively.

Many effective methods had been developed in recent decades to reduce or cancel out the dominant noise of the front-end amplifier of the biotelemetry [19]–[25]. The chopper method is one of the most effective means of reducing the flicker noise, and has been widely developed in the low power analog circuitry design of bio-signal recording systems [26]–[34]. Regarding the v_{ni}, (1) indicates that increasing the CMRR and Z_c of the front-end amplifier and reducing ΔR of the two electrodes cancel out the v_{ni}.

In addition to the noise cancellation problem, designing a low power and low voltage system based on the current VLSI circuit approach is also limited in a conventionally adopted method in which MOS transistors are designed to operate in saturation mode. This work design a low-power and low-noise front-end biopotential amplifier IC based on an approach in which the MOS circuits operate in a subthreshold region. A chopper-stabilized instrumentation amplifier proposed elsewhere [26]–[29]

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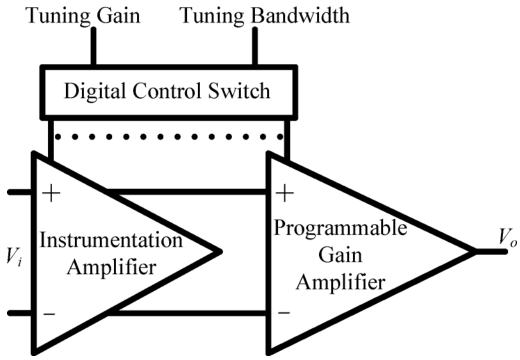

Fig. 2. Architecture of the front-end biopotential amplifier.

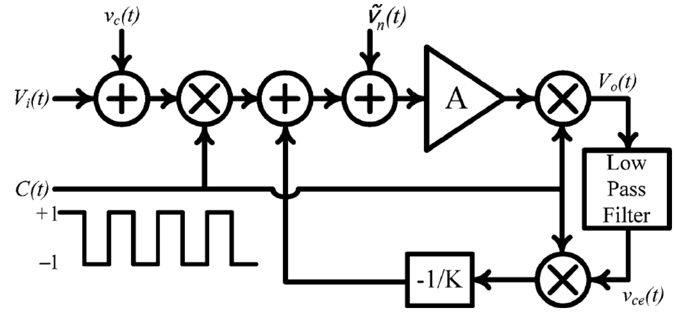

Fig. 3. Diagram of a chopping IA with a common mode interference cancellation.

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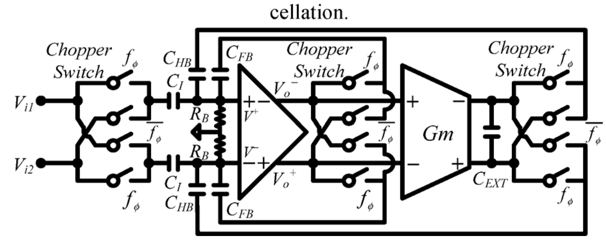

Fig. 4. Circuit diagram of the proposed IA.

is adopted to reduce the flicker noise. Additionally, the common and differential mode interference caused by a mismatch of the impedance of the two input electrodes for telemetry systems is analyzed using a simplified model. Moreover, a wide range of biopotential signals is recorded using a programmable gain amplifier (PGA), thus providing the proposed front-end amplifier design with a tunable gain and a wide application bandwidth.

II. Design of Front-End Biopotential Amplifier IC

Fig. 2 schematically depicts the front-end biopotential amplifier, which consists of an instrumentation amplifier (IA), a programmable gain amplifier (PGA), and digital control interface. The IA amplifies the signal with a strong rejection of interference. To accommodate the recording of the various biopotential signals, the programmable gain amplifier offers a variable gain and a bandwidth that is controlled via a digital switch.

A. The Chopper Stabilized IA With Common Mode Interference Cancellation

Flicker noise $(1/f)$ is concentrated in low-frequency bands and arises from the channel of the MOS transistor, since the silicon crystal at the interface between the gate oxide and the silicon substrate in the MOSFET is imperfect. The chopper technique efficiently reduces the flicker noise in the design of an analog circuit. Fig. 3 displays diagram of chopper IA with a common mode interference cancellation scheme. The chopper IA comprises an OPAMP, a low pass filter, three multipliers, which are controlled by a chopping square wave of with values $+1$ and -1, and a chopper feedback function with a loop gain of 1/K. The terms $V_i(t)$ and $V_o(t)$ denote the system input and output signals, respectively; $v_c(t)$ represents common mode interference; $v_{ce}(t)$ denotes an estimated common mode interference, and $\tilde{V}_n(t)$ is the flicker noise of the amplifier.

The $V_i(t)$ and $v_c(t)$ are modulated to the odd harmonic frequency of the square waveform $C(t)$ of the chopper using the first multiplier. The modulated $V_i(t)$ and $v_c(t)$ are mixed with $\tilde{V}_n(t)$. Then, the amplifier and second multiplier amplify and demodulate $V_i(t)$ back to the original signal band, respectively, and $\tilde{V}_n(t)$ is modulated to the high-frequency band. Finally, the system output signal $V_o(t)$ is given by

$$V_o(t) = AV_i(t) + C(t) \times \tilde{v}_n(t) + A\left(v_c(t) - \frac{1}{K}v_{ce}(t)\right). \quad (2)$$

TABLE I
Value of the Related Parameters in Fig. 4

C_I	11 *pf*
C_{FB}	0.1 *pf*
C_{HB}	0.5 *pf*
C_{EXT}	0.33 *μf*
R_B	100M *Ω*
Gm	1.04 *μA/V*
A_d	68 dB
A_c	-98 dB

Where $\tilde{v}_n(t)$ represents the $\tilde{V}_n(t)$ being amplified by a gain factor of A. The third term of the (2) indicates that the estimated $v_{ce}(t)$, extracted from $V_o(t)$ by a low pass filter and a chopper feedback loop, is applied to cancel the $v_c(t)$.

Fig. 4 shows the circuit diagram of the proposed IA. Table I presents the values of the related parameters in Fig. 4. To reduce the common mode voltage and thermal noise, a chopper-stabilized amplifier with a Gm-C feedback filter was developed. The bootstrapped NMOS chopper is adopted in the system since a low power and low voltage are required.

The proposed IA has two feedback paths: one provides the close-loop gain of the system via feedback capacitors $C_{\rm FB}$, while the other cancels out the interference that is caused by the common mode voltage and the mismatch of the impedance of the two input electrodes, which is extracted by a Gm-C filter and via feedback capacitors $C_{\rm HB}$. The two feedback paths were formed from capacitors, because the capacitive closed-loop configuration dissipates less power than the resistive feedback one. The output voltages of the proposed IA are

$$V_o^- = -A_d(V^+ - V^-) + \frac{A_C}{2}(V^+ + V^-) \quad (3)$$

$$V_o^+ = A_d(V^+ - V^-) + \frac{A_C}{2}(V^+ + V^-). \quad (4)$$

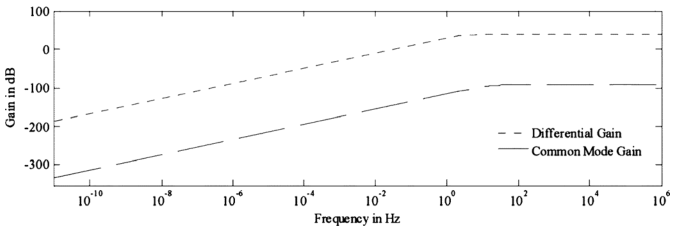

Fig. 5. Differential and common mode gain of the proposed IA.

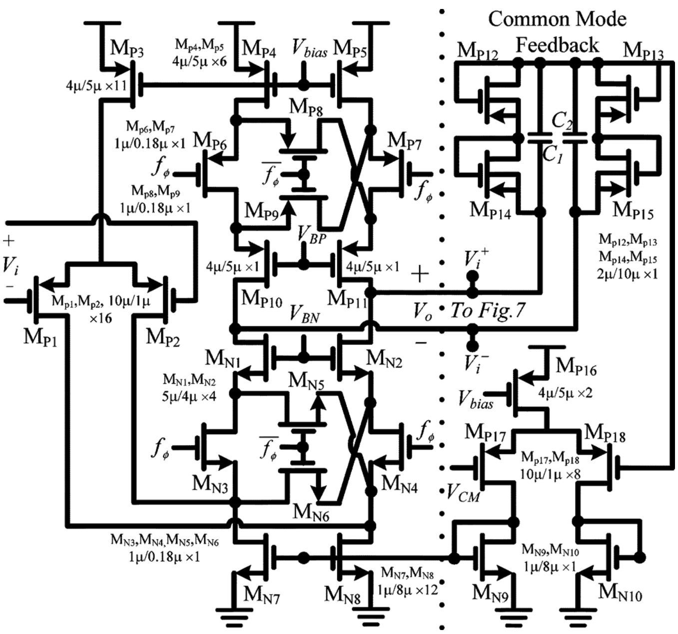

Fig. 6. Circuit diagram of the proposed OPAMP.

Where A_d, and A_c represent the differential and common mode open loop gain of the OPAMP, respectively. The differential and common mode gain (G_d and G_c) of the proposed IA can be derived as

$$V_o^- - V_o^+ = G_d(V_{i1} - V_{i2}), \quad G_d = \frac{-C_I}{C_{\rm FB}} \frac{1}{\left(1 + \frac{G_m C_{\rm HB}}{sC_{\rm FB}C_{\rm ext}}\right)} \tag{5}$$

$$V_o^- + V_o^+ = G_c(V_{i1} + V_{i2}), \quad G_c = \frac{A_C \times C_I}{(C_I + C_{\rm FB}(1 - A_C))\left(1 + \frac{1}{sR_B(C_I + C_{\rm FB}(1-A_c))}\right)}. \tag{6}$$

Equations (5) and (6) describe a high pass filter with 3 dB high pass poles of $(G_m C_{\rm HB})/(C_{\rm FB}C_{\rm ext})$ and $1/(R_B(C_I + C_{\rm FB}(1 - A_c)))$. Fig. 5 plots the differential and common mode gain as function of frequency. The results indicate that the CMRR of the system exceeds 125 dB when signal frequency below 10 kHz.

B. Operational Amplifier

Fig. 6 schematically depicts the circuit diagram of the OPAMP used in design of the proposed IA. The OPAMP comprises a fully differential folded-cascode amplifier with two choppers and a common mode feed back (CMFB) circuit. The PMOS transistors $(\mathrm{M_{P1}} - \mathrm{M_{P3}})$ are utilized in the input circuit to reduce the flicker noise and the circuit mismatch caused by the process variation, increase the range of the input common

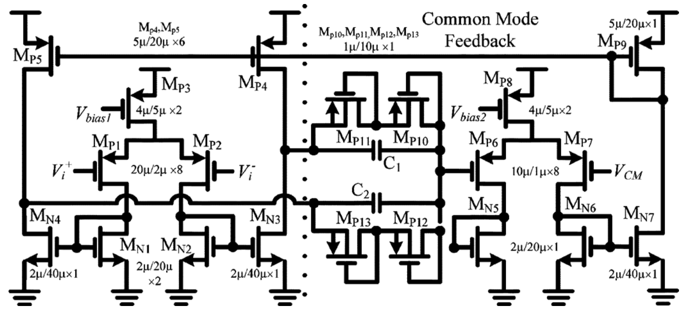

Fig. 7. Circuit diagram of the OTA.

mode voltage. The proposed mixer is then constructed using a group of the PMOS $(\mathrm{M_{P6}} - \mathrm{M_{P9}})$ and NMOS $(\mathrm{M_{N3}} - \mathrm{M_{N6}})$ chopping switches to eliminate the residual offset of the circuit. This work also develops a novel continuous time CMFB $(\mathrm{M_{P12}} - \mathrm{M_{P18}}, \mathrm{M_{N9}}, \mathrm{M_{N10}}$, and $C_1, C_2)$ with a long channel PMOS-resistor to reduce the degradation of the open loop gain A_d in the conventional CMFB circuit with a resistance voltage divider. The long channel PMOS pseudo-resistors are implemented as a light loading circuit with a bias current below 20 nA which reduce the effect upon the swing of the OPAMP especially for the low speed input signal.

To maximize the loop gain and minimize the power of the IA system, the MOS transistors are biased to operate in the region of the weak inversion. Consequently, the open loop gain, common mode gain and unit gain bandwidth are 68 dB, -98 dB and 100 kHz, respectively.

By using an operational transconductance amplifier (OTA) with a fully differential current-mirror, this work constructs a Gm filter since the performance of the OTA circuit is less sensitive to the process variation. Fig. 7 shematiclly depicts the OTA circuit.

To ensure a stable operation, this work designs the dominant pole of the OTA circuit at the output node to increase its time constant. The output of the OTA circuit is connected to an external capacitor with a capacitance of 0.33 μF in order to form a low pass filter with a 3 dB frequency of 0.5 Hz, thus diminishing the interference caused by an imbalance of the electrode impedance.

Fig. 8 presents an input-referred noise density of the proposed IA circuit by using the Cadence Spectre tool. The thermal noise floor is 70 nV/$\sqrt{\rm Hz}$. The amount of the flicker noise is inversely proportional to the frequency below the corner frequency of around 1 kHz. The upper line of the figure presents an input-referred noise of 10000 nv/rtHz without using the chopping method and the lower line 73 nv/rtHz when activating the chopping method. Fig. 8 indicates that the chopping method reduces the flicker noise of the IA system several hundred times than without using the chopping method.

C. Programmable Gain Amplifier

Owing the significant variation in the amplitudes of biopotential signals, an amplifier can be designed with a tunable gain to satisfy the specification. Here, such a tunable gain is provided using a PGA. Fig. 9 illustrates the PGA, which is a capacitive differential amplifier that consists of a single-end current-mirror OTA with a capacitive gain feedback, pseudo resis-

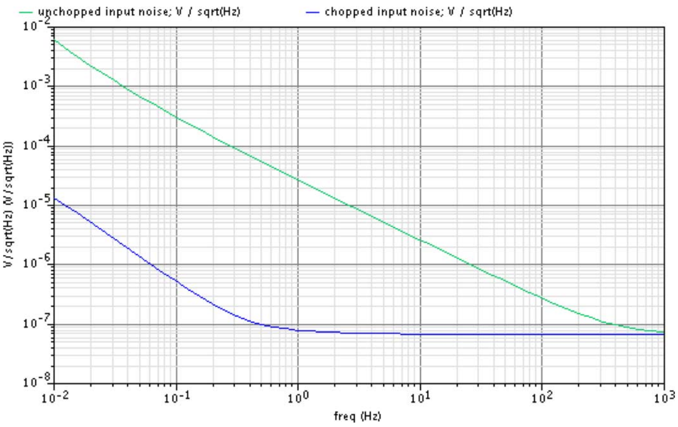

Fig. 8. Input-referred noise density by Cadence Spectre.

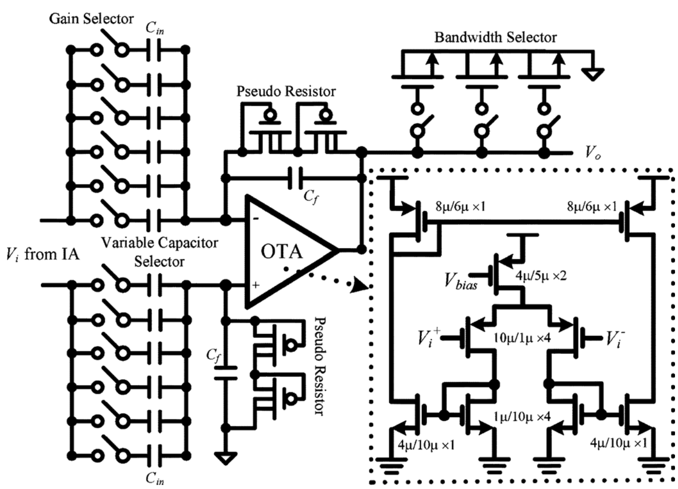

Fig. 9. Circuit diagram of the PGA.

tors made from PMOS transistor, and switches for tuning the gain. The gain selector is made from 12 capacitors of the same type, providing variable gains of 0, 6 and 30 dB. The bandwidth selector consists of 3 capacitors made by NMOS transistors, which produce system 2 selectable frequency bands of 0.5–100 and 10–400 Hz. During blocking the DC offset, a high pass filter with an extremely low 3 dB frequency is established using the positive terminal feedback path. The differential gain of the PGA system can be derived as

$$\frac{V_o}{V_I} = \frac{-C_{\rm in}}{C_f}\frac{1}{\left(1+s\frac{C_{\rm in}C_L}{C_f G_m}\right)}. \quad (7)$$

A selectable $C_{\rm in}$ was employed to control the system gain. When $\omega \ll (C_f G_m)/(C_{\rm in} C_L)$, the differential gain is $C_{\rm in}/C_f$. The maximum variable gain of the PGA is set to 30 dB.

D. Fully-Differential Boosted Clock Driver

A residual offset voltage is introduced due to the charge injection of the MOS switches in the chopper IA circuit. The residual offset voltage $(V_{\rm RO})$ can be derived as

$$V_{\rm RO} = 2 \times f_\phi \times V_{\rm spike} \times \tau. \quad (8)$$

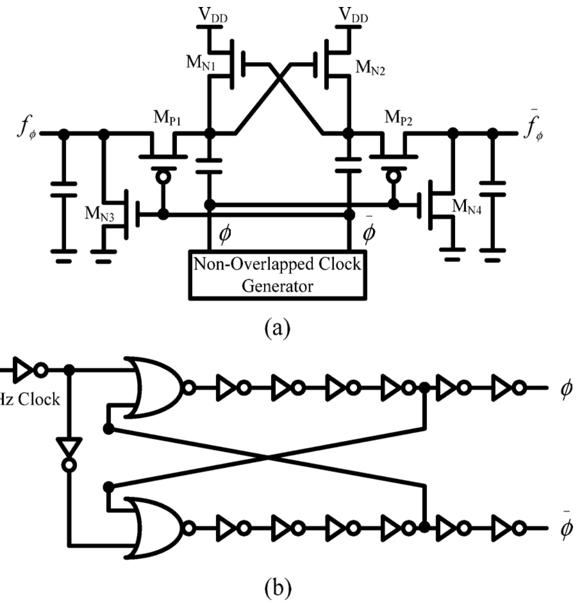

Fig. 10. (a) Circuit diagram of the proposed fully-differential boosted clock driver. (b) Logic diagram of the non-overlapped clock generator.

Where f_ϕ is the chopping frequency, $V_{\rm spike}$ is the spike magnitude due to the charge injection of the input MOS switches, and τ refers to the settling time constant of the OPAMP. However, according to (8), a smaller τ and lower f_ϕ can reduce the $V_{\rm RO}$ yet also increase the power consumption and the flicker noise of the IA system.

Applying a fully-differential boosted clock driver reduces $V_{\rm RO}$ and increase the output clock voltage from $V_{\rm DD}$ to $2\,V_{\rm DD}$ without consuming the system power. Fig. 10(a) shows the circuit diagram of the proposed fully-differential boosted clock driver. Fig. 10(b) illustrates the logic diagram of the proposed non-overlapped clock generator composed of NOR gates and inverter chains. All of the circuits in the proposed non-overlapped clock generator are designed using standard cells of minimal sizes since the f_ϕ is a low speed clock below several kilo hertz. Notably, the f_ϕ must be designed larger than the corner frequency 1 kHz shown in Fig. 8 to increase the system SNR. Based on Fig. 8 and (8), the 4 kHz chopper frequency f_ϕ is applied in the proposed IA circuit, which capable of reducing the $V_{\rm RO}$ and the flicker noise and with a 3 kHz spacing frequency from the corner frequency suitable for boisignal recording.

III. Common and Differential Mode Interference Rejection in the Proposed IA

A simplified circuit model shown in Fig. 11 is applied to calculate the interference of the proposed amplifier under various conditions. C_{n60} is the capacitance between the power line and the human body; i_{n60} represents the noise current that is coupled from the power line into the human body; V_s is the noise of the static charge on the human body; V_n denotes the input noise of the circuit; C_B and C_G are the capacitance from the human body and the amplifier to the ground, respectively; Z_i

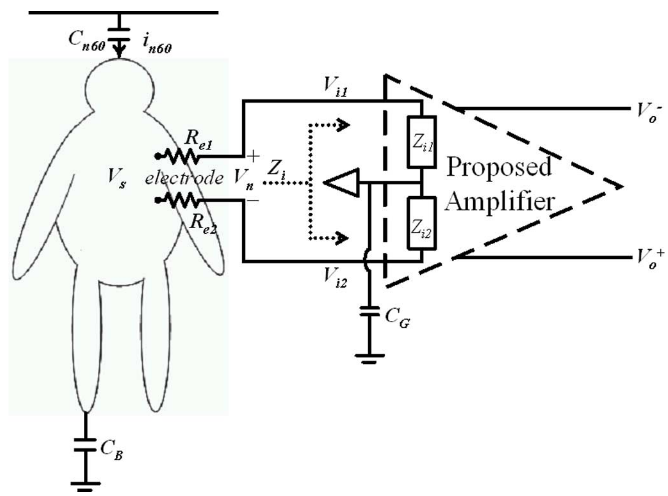

Fig. 11. A simplified circuit model for the proposed IA.

represents the input equivalent impedance of the IA which includes the common mode input impedance Z_{ic} and the differential mode input impedance Z_{id}. Z_{ic} and Z_{id} are derived as

$$Z_{id} = \frac{1}{sC_I} + \frac{1}{s((1+2A_d)C_{\rm FB}+C_{\rm HB}) + \frac{1}{R_B} + \frac{4A_dC_{\rm HB}G_m}{C_{\rm ext}}} \tag{9}$$

$$Z_{ic} = \frac{1}{sC_I} + \frac{1}{s(1-A_c)C_{\rm FB}+\frac{1}{R_B}}. \tag{10}$$

The common mode interference V_{ncs} and V_{nc60} are

$$V_{ncs} = \frac{1}{\rm CMRR} \times \frac{\left|\frac{Z_{ic}}{2}\right| V_s}{\left|\frac{Z_{ic}}{2}\right| + \left|\frac{1}{sC_G}\right|} \tag{11}$$

$$V_{nc60} = \frac{1}{\rm CMRR} \times \frac{\left|\frac{Z_{ic}}{2}\right| \times \left|\frac{1}{sC_B}\right| i_{n60}}{\left|\frac{Z_{ic}}{2}\right| + \left|\frac{1}{sC_G}\right| + \left|\frac{1}{sC_B}\right|}. \tag{12}$$

With the impedance mismatch of the input electrodes, a very large differential mode interference, to which the common mode interference contributes, will be coupled into the proposed circuit, reducing SNR (signal to noise ratio) of the system. Therefore, the differential mode interference V_{nds} and V_{nd60} due to V_s and i_{n60}, respectively, can be obtained as

$$V_{nds} = \frac{\Delta R \times V_s}{\left|\frac{Z_{id}}{2}\right| + \left|\frac{1}{sC_G}\right|} \tag{13}$$

$$V_{nd60} = \frac{\Delta R \times \left|\frac{1}{sC_B}\right| i_{n60}}{\left|\frac{Z_{id}}{2}\right| + \left|\frac{1}{sC_G}\right| + \left|\frac{1}{sC_B}\right|}. \tag{14}$$

Figs. 12 and 13 plot the noise level of the proposed amplifier, obtained from (11)–(14), for various values of V_s, i_{n60} and ΔR. These plots indicate that the proposed amplifier suffer maximum common mode and differential mode interference of less than

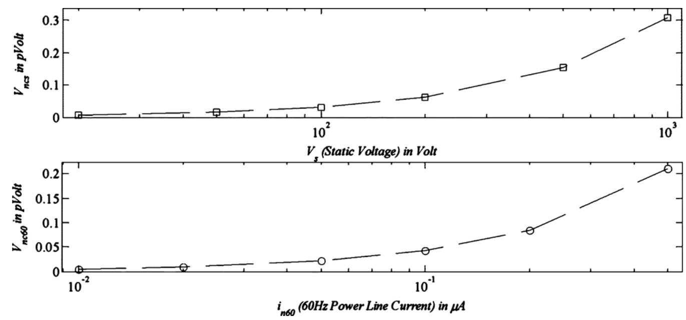

Fig. 12. Estimated results of common mode interference for the proposed IA.

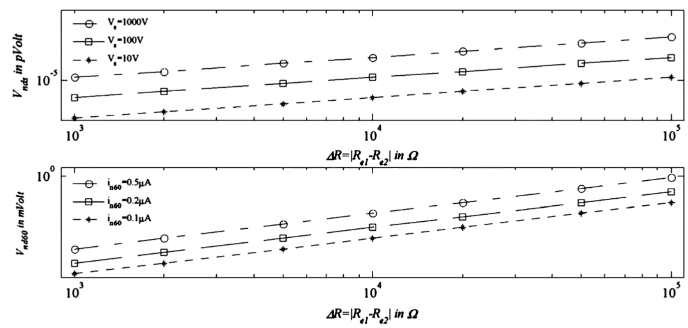

Fig. 13. Estimated results of differential interference for the proposed IA.

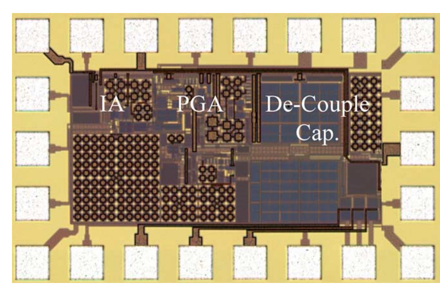

Fig. 14. Die photo of the proposed front-end biopotential amplifier IC.

0.35 pV and 0.85 mV, respectively, in the worst case with $V_s = 1000$ V and $i_{n60} = 0.5\ \mu$A, $\Delta R = 100$ kΩ. Hence, the IA has high CMRR and input impedance Z_i with greater immunity to interference.

IV. Implementation and Measurement

The proposed front-end amplifier is fabricated using TSMC 0.18 μm CMOS technology. Fig. 14 presents a die photograph, including an IA circuit with a GM-C filter, a PGA, output buffers and MOS capacitors. The chip area is 1.03×0.62 mm^2 and the core area is 0.77×0.36 mm^2.

A. Measurement of the Human Body Noise

During measurement of the human body noise, the left wrist of the human body and Agilent-54832D oscilloscope are connected by applying one electrode (Kendall H99SG). Fig. 15 shows the measurement results of the human body noise and its frequency spectrum. The frequency spectrum indicates that the main noise sources of the human body are below 10 kHz, composed mainly of the 60 Hz power line noise and its harmonics. The measured human body noise v_c with an amplitude of ± 670 mV is coupled into the IA system by using the form

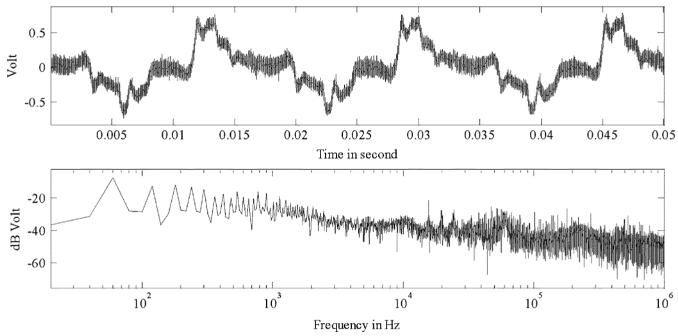

Fig. 15. The measured human body noise (measured by Agilent Oscilloscope 54831D).

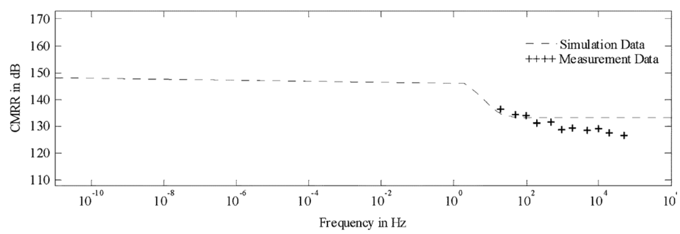

Fig. 16. The simulation and measurement results of the CMRR.

of common and differential mode as shown in (1), which saturates the front-end amplifier of the IA system and significantly reduces the system SNR.

B. CMRR Measurement Result of the Proposed IA

By using 12 test stimuli, this work measures the CMRR of the proposed front-end amplifier with ± 1 V sinusoidal signals ranging from 20 Hz to 100 kHz. The test stimulus are then generated and received by using an Agilent 33250A wave generator and an Agilent E4440 RF spectrum analyzer, respectively. The supply voltage of the proposed front-end amplifier is set to 0.4 V to bias the MOS transistors operating in the subthreshold region. Fig. 16 summarizes the simulation (from (5)–(6)) and measurement results of the CMRR. According to this figure, the measured result of the CMRR closely resembles the calculated results derived from (5)–(6). The maximum difference between the calculation and measurement results is <10 dB when the signal frequency is 100 kHz. The minimum CMRR is larger than 125 dB, which is sufficient to reject the common and differential mode noise shown in (1) and Fig. 1.

C. Measurement of the 60 Hz Differential Interference Arising Due to Impedance Mismatch of the Input Electrodes

This work measures how 60 Hz differential interference arises due to impedance mismatch of the two electrodes and affects the proposed analog front-end amplifier. A variable resistor is connected between the positive input terminal of the IA circuit and its electrode, subsequently providing an impedance mismatch ΔR, shown as the second term of (1) from 0 Ω to 100 kΩ. The two electrodes are then connected together and placed on the right wrist that mimics the environment, as shown in Fig. 11. Next, the 60 Hz body noise with a noise current i_{n60} of about 0.7 μA (peak-to-peak) becomes differential noise coupled into the IA circuit. Additionally, the output noise

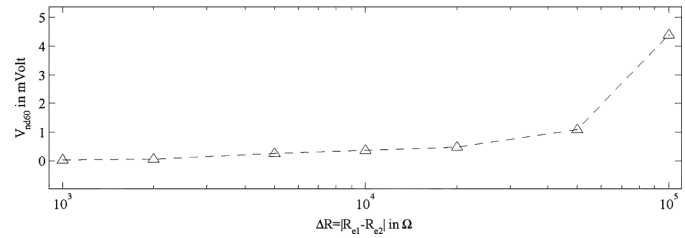

Fig. 17. Measurement result of the 60 Hz differential noise.

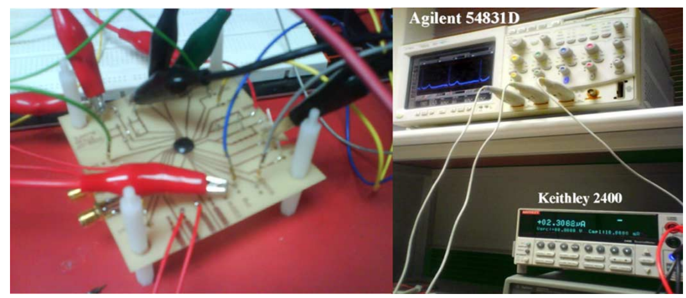

Fig. 18. Photo of the measurement setup.

amplitude of the IA circuit is measured using an agilent E4440 RF spectrum analyzer. Fig. 17 shows the measurement results of the 60 Hz differential noise due to impedance mismatch of the two electrodes of the front-end amplifier with a different ΔR. According to (1)–(5), the measurement result indicates that increasing ΔR will increase the amount of the body noise into the IA circuit. The maximum 60 Hz differential input noise of the IA is only 4.5 mV when ΔR equal 100 kΩ since high input impedance exists at the input of the proposed IA circuit which is the same as the description of the (13) and (14).

D. Measurements of ECG, EEG, and EMG

Feasibility of the proposed approach is verified by estimating the SNR of an ECG signal first, and then measuring EEG and EMG signal, respectively. Fig. 18 displays the experimental setup. Two electrodes (Kendall H99SG) connect the measured body directly to the input of the proposed front-end amplifier. Next, the ECG signal is obtained from the proposed front-end amplifier by using an Agilent 54831D mixed-signal oscilloscope, at a sampling rate of 400 kHz, subsequently yielding 2M data points at a time interval of 5 second. The Keithley 2400 source meter employs to measure the dissipated current and power of the proposed amplifier.

Fig. 19 plot the ECG measurement made by using different supply voltages ($V_{DD} = 0.8$ V, 0.6 V and 0.4 V) and the same in the frequency domain, respectively. The voltage gain of the proposed IC circuit is set to 40 dB, and the output amplitude of the ECG is 270 mV. According to these figures, although no static charge or 60 Hz interference occurs in the circuit, some flicker noise is modulated to high frequency and the intrinsic noise of the oscilloscope is present with a maximum peak-to-peak voltage of 10 mV. The proposed IC chip achieves a dynamic range (1% THD) of 61 dB with a total power current of 0.226 μA under a supply voltage of 0.4 V.

Fig. 20 illustrates the ECG measured results of a commercial bio-signal recording amplifier generally made by INA114

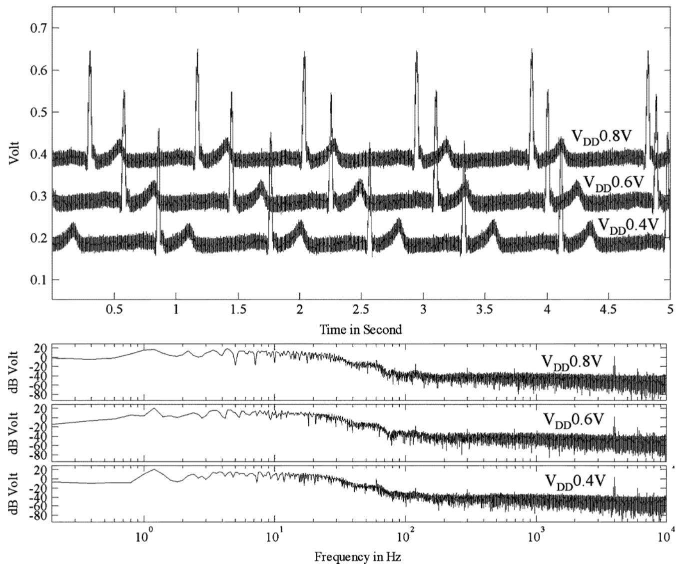

Fig. 19. ECG recording and frequency spectrum results of the proposed front-end amplifier.

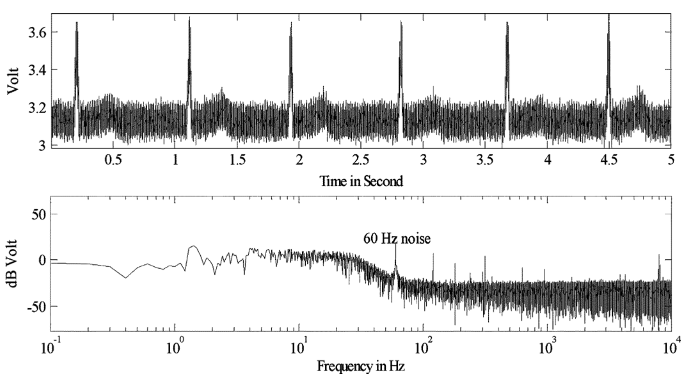

Fig. 20. The ECG measured results of a commercial bio-signal recording amplifier made by INA114 and opa121.

and opa121, in which 60 Hz and 8.25 kHz noise occurs in the recording amplifier under a high noise floor 150 $\mu V/\sqrt{Hz}$ and peak-to-peak voltage of 100 mV. This finding suggests that the amount of the CMRR and the input impedance of the commercial recording amplifier are insufficient to reject the 60 Hz power line noise. The measured SNR is 21 dB with a supply voltage of 6.2 V and total power consumption of 50 mW. Fig. 21 shows an ECG measurement result of a commercial telemetry biopotential recorder (BioRadio150 made by Cleveland Medical Devices Inc.) with a 3 V supply voltage and 350 μW power consumption [35]. Table II summarizes the performance of the proposed amplifier and the commercial biopotential recorder, indicating the proposed amplifier performs better than the commercial biopotential recorder (BioRadio150) in power consumption and the commercial bio-signal recording amplifier (INA114 and opa121) in all respect.

This work also measure EEG and EMG signals by placing two electrodes on the occipital lobe and the right forearm, respectively. The two electrodes are about 2 cm apart from each other. The sampling rate of the Tektronix TPS 2024 oscilloscope is set to 500 Hz. Fig. 22 shows the measurement results of a α

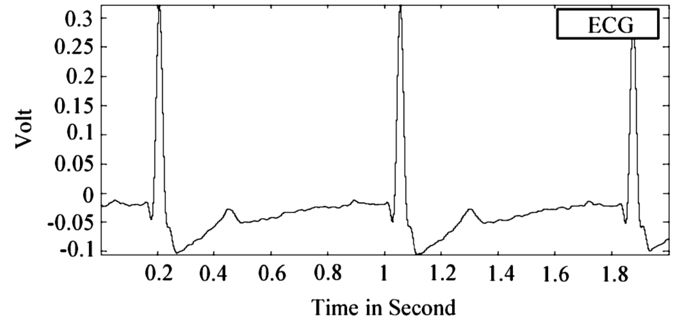

Fig. 21. The ECG measured results of a commercial telemetry recording system-BioRadio150 made by Cleveland Medical Devices Inc.

TABLE II
PERFORMANCES OF THE PROPOSED IC CHIP

Technology	TSMC 0.18 μm CMOS			INA114 & OPA121	BioRadio 150
Chip Area/ Core Area	$1.03\times0.62mm^2$/ $0.77\times0.36mm^2$				
Supply voltage (V)	0.8	0.6	0.4	6.2	3
Supply current (μA)	1.86	1	0.226	8,000	117
Power (μW)	1.49	0.6	0.09	50,000	350
SNR (dB)	66.2	63.6	54.1	21	NA
Noise floor @ 10 Hz (nV/ $\sqrt{Hz}$)	57	129	1760	150,000	NA
Dynamic range (dB) (1% THD)	66	63	61	NA	NA
Input Referred Noise @ 0.5 – 100 Hz	0.88	5.41	72.1	NA	NA

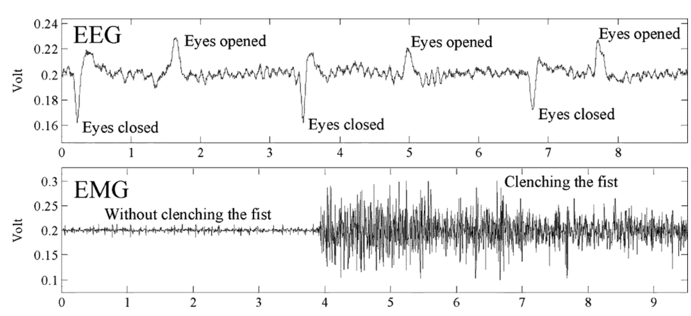

Fig. 22. The measurement results of the EEG and EMG signal.

wave of EEG with eyes opened and eyes closed control signal, as well as an EMG signal of the right forearm with and without clenching the fist, respectively. Based on those results, maximum peak-to-peak amplitude of 40 mV and 100 mV of EEG and EMG signal are measured, respectively, under maximum noise peak-to-peak amplitude of 8 mV from the intrinsic noises of the oscilloscope.

Measurement results of ECG, EEG and EMG signal verify the CMRR, and the input impedance of the proposed front-end biopotemtial amplifier is sufficiently large to reject the common and differential interference significantly, which is suitable for a biosignal recording system. Table III summarizes the performance and comparison results of the bio-potential front-end amplifier.

TABLE III
COMPARISON RESULTS OF THE BIO-POTENTIAL FRONT-END AMPLIFIER

Amplifier	This work Measured	T. Denison, JSSC 07	R.F. Yazicioglu, JSSC 06	K.A. Ng, TCASI 05	R. R. Harrison, JSSC 03
Supply Current	0.226μA	1.2μA	11.1μA	485μA	180nA
Supply Voltage	0.4V	1.8V	3V	±1.5V	±2.5V
Power	0.09μW	2.16μW	33.3μW	1.45mW	0.9μW
NEF	4.7	4.9	7.8	59	4.8
Gain (dB)	40-70	45.5	>60	80	40
Input-referred Noise RMS (μV)	0.88 (100Hz)	0.93 (100Hz)	0.65 (100Hz)	0.73 (100Hz)	1.6 (30Hz)
CMRR (dB)	>120	>100	>110	>110	>85
High Pass 3dB Frequency(Hz)	0.5, 10	0.5	0.5,10	0.3	0.014
Low Pass 3dB Frequency(Hz)	100,400	250	>150	150	30
Core Area(mm^2)	0.28	0.7	2	4.81	0.16
Technology	0.18μm	0.8μm	0.5μm	0.5μm	1.5μm

V. CONCLUSION

A low power front-end biopotential amplifier IC that can be adopted in biosignal recording is implemented. The MOS transistors in the proposed IC are operating in subthreshold region to reduce the system power. Chopping technique is applied to remove the flicker noise in the MOS circuit into the high frequency band. A Gm-C filter is utilized to detect and cancel out the differential interference that was generated by imbalance of the electrodes impedance. AC-coupling with capacitive feedback gives the IA a high CMRR and high input impedance.

Calculation and measurement results demonstrate that the CMRR of the proposed biopotential amplifier is greater than 125 dB, and has maximum common mode and differential mode interference of less than 0.35 pV and 4.5 mV, respectively, in the worst case with $V_s = 1000$ V and $i_{n60} = 0.7$ μA, $\Delta R = 100$ kΩ.

The proposed device has been fabricated in TSMC 0.18 μm process with a chip area of 1.03×0.62 mm^2 and a core area of 0.77×0.36 mm^2. Measurements results have revealed that the implemented IC has a SNR of 54.1 dB under a supply voltage of 0.4 V and a power consumption of 0.09 μW.

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REFERENCES

[1] M. J. Burke and D. T. Gleeson, "A micropower dry-electrode ECG preamplifier," *IEEE Trans. Biomed. Eng.*, vol. 47, no. 2, pp. 155–162, Feb. 2000.

[2] C.-J. Yen, W.-Y. Chung, and M. C. Chi, "Micro-power low-offset instrumentation amplifier IC design for biomedical system applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 4, pp. 691–699, Apr. 2004.

[3] J. N. Y. Aziz, R. Genov, B. L. Bardakjian, M. Derchansky, and P. L. Carlen, "Brain—Silicon interface for high-resolution *in vitro* neural recording," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 1, pp. 52–62, Mar. 2007.

[4] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energy-efficient micropower neural recording amplifier," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 2, pp. 136–147, Jun. 2007.

[5] R. F. Yazicioglu, P. Merken, R. Puers, and C. V. Hoof, "A 200 μW eight-channel EEG acquisition ASIC for ambulatory EEG systems," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 3025–3038, Dec. 2008.

[6] M. Mollazadeh, K. Murari, G. Cauwenberghs, and N. Thakor, "Micropower CMOS integrated low-noise amplification, filtering, and digitization of multimodal neuropotentials," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 1, pp. 1–10, Feb. 2009.

[7] L. Fay, V. Misra, and R. Sarpeshkar, "A micropower electrocardiogram amplifier," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 5, pp. 312–320, Oct. 2009.

[8] M. Mollazadeh, K. Murari, G. Cauwenberghs, and N. Thakor, "Wireless micropower instrumentation for multimodal acquisition of electrical and chemical neural activity," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 6, pp. 388–397, Dec. 2009.

[9] O. T. Inan and G. T. A. Kovacs, "An 11 μW, two-electrode transimpedance biosignal amplifier with active current feedback stabilization," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 2, pp. 93–100, Apr. 2010.

[10] F. Shahrokhi, K. Abdelhalim, D. Serletis, P. L. Carlen, and R. Genov, "The 128-channel fully differential digital integrated neural recording and stimulation interface," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 3, pp. 149–161, Jun. 2010.

[11] E. Greenwald, M. Mollazadeh, C. Hu, W. Tang, E. Culurciello, and N. Thakor, "A VLSI neural monitoring system with ultra-wideband telemetry for awake behaving subjects," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 2, pp. 112–119, Apr. 2011.

[12] F. Zhang, J. Holleman, and B. P. Otis, "Design of ultra-low power biopotential amplifiers for biosignal acquisition applications," *IEEE Trans. Biomed. Circuits Syst.*, 2012, accepted for publication.

[13] Y. Netzer, "The design of low-noise amplifier," *Proc. IEEE*, vol. 69, no. 6, pp. 728–741, Jun. 1981.

[14] W. M. Leach, Jr., "Fundamentals of low-noise analog circuit design," *Proc. IEEE*, vol. 82, no. 10, pp. 1515–1538, Oct. 1994.

[15] N. V. Thakor and J. G. Webster, "Ground-free ECG recording with two electrodes," *IEEE Trans. Biomed. Eng.*, vol. BME-27, no. 12, pp. 699–704, Dec. 1980.

[16] B. B. Winter and J. G. Webster, "Reduction of interference due to common mode voltage in biopotential amplifiers," *IEEE Trans. Biomed. Eng.*, vol. 1, no. 1, pp. 58–62, Jan. 1983.

[17] J. G. Webster, *Medical Instrumentation: Application and Design*. New York: Wiley, 1998.

[18] R. Pallàs-Areny, "Interference-rejection characteristics of biopotential amplifier: A comparative analysis," *IEEE Trans. Biomed. Eng.*, vol. 35, no. 11, pp. 953–959, Nov. 1988.

[19] E. M. Spinelli and M. A. Mayosky, "AC coupled three op-amp biopotential amplifier with active DC suppression," *IEEE Trans. Biomed. Eng.*, vol. 47, no. 12, pp. 1616–1619, Dec. 2000.

[20] E. M. Spinelli* and M. A. Mayosky, "Two-electrode biopotential measurements: Power line interference analysis," *IEEE Trans. Biomed. Eng.*, vol. 52, no. 8, pp. 1436–1442, Aug. 2005.

[21] T. Degen and H. Jäckel, "A pseudodifferential amplifier for bioelectric events with DC-offset compensation using two-wired amplifying electrodes," *IEEE Trans. Biomed. Eng.*, vol. 53, no. 2, pp. 300–310, Feb. 2006.

[22] B. Gosselin, M. Sawan, and C. A. Chapman, "A low-power integrated bioamplifier with active low-frequency suppression," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 3, pp. 184–192, Sep. 2007.

[23] R. Harrison, H. Fotowat, R. Chan, R. J. Kier, R. Olberg, A. Leonardo, and F. Gabbiani, "Wireless neural/EMG telemetry systems for small freely moving animals," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 2, pp. 103–111, Apr. 2011.

[24] V. Majidzadeh, A. Schmid, and Y. Leblebici, "Energy efficient low-noise neural recording amplifier with enhanced noise efficiency factor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 3, pp. 262–271, Jun. 2011.

[25] R. Rieger, "Variable-gain, low-noise amplification for sampling front ends," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 3, pp. 253–261, Jun. 2011.

[26] M. A. T. Sanduleanu, B. Nauta, and H. Wallinga, "Low-power low-voltage chopped transconductance amplifier for noise and offset reduction," in *Proc. 23rd Euro. Solid-State Circuits Conf.*, Oct. 1997, pp. 204–207.

[27] M. Sanduleanu, A. J. M. van Tuijl, R. F. Wassenaar, M. C. Lammers, and H. Wallinga, "A low noise, low residual offset, chopped amplifier for mixed level applications," in *Proc. IEEE Int. Conf. Electron. Circuits Syst.*, 1998, vol. 2, pp. 333–336.

[28] T. Denison, K. Consoer, W. Santa, G. Molnar, and K. Miesel, "A 2.2 μW 94 nV/rtHz, chopper-stabilized instrumentation amplifier for EEG detection in chronic implants," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, Feb. 11–15, 2007, pp. 162–594.

[29] T. Denison, K. Consoer, W. Santa, A.-T. Avestruz, J. Cooley, and A. Kelly, "A 2 μW 100 nV/$\sqrt{}$Hz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2934–2945, Dec. 2007.

[30] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, 2003.

[31] K. A. Ng and P. K. Chan, "A CMOS analog front-end IC for portable EEG/ECG monitoring applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 11, pp. 2335–2347, Nov. 2005.

[32] R. F. Yazicioglu, P. Merken, R. Puers, and C. V. Hoof, "A 60 μW 60 nV/$\sqrt{}$Hz readout front-end for portable biopotential acquisition systems," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1100–1110, May 2007.

[33] R. Wu, K. A. A. Makinwa, and J. H. Huijsing, "A chopper current-feedback instrumentation amplifier with a 1 MHz $1/f$ noise corner and an AC-coupled ripple reduction loop," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 332–3242, Dec. 2009.

[34] J. Xu, R. F. Yazicioglu, B. Grundlehner, P. Harpe, K. A. A. Makinwa, and C. V. Hoof, "A 160 μW 8-channel active electrode system for EEG monitoring," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 6, pp. 555–567, Dec. 2011.

[35] "BioRadio 150 hardware specification," Cleveland Medical Devices Inc.

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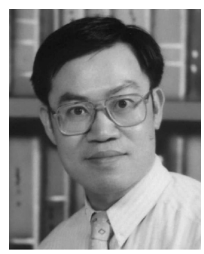

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