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# Flip-Chip Packaging of $In_{0.6}Ga_{0.4}As$ MHEMT Device on Low-Cost Organic Substrate for W-Band Applications

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A discrete low noise $In_{0.6}Ga_{0.4}As$ MHEMT device with 150 nm gate length was flip-chip assembled on the low-cost RO3210 organic substrate for wireless communication applications. The measured DC characteristics were very similar before and after flip-chip assembly. The flip-chip packaged MHEMT device showed a high drain current density of 516 mA/mm and a maximum transconductance of 576 mS/mm at a $V_{DS}$ of 0.8 V. The insertion gain of the flip-chip packaged device was decayed less than 2 dB up to 100 GHz as compared to the data of bare die. Moreover, the measured minimum noise figure was less than 2 dB as measured at $V_{DS}$ of 0.7 V and $V_{GS}$ of -0.7 V in the frequency range from 20 to 64 GHz for the device after flip-chip assembly. The excellent performance of the flip-chip packaged MHEMT device demonstrates the feasibility of using low cost organic substrate for high frequency applications up to W band.

## Introduction

The indium-rich $In_xGa_{1-x}As/In_xAl_{1-x}As$ based MHEMT (Metamorphic high electron mobility transistor) are gaining increasing popularity for many applications, such as high speed telecommunication systems and high frequency wireless systems. This is due to high electron mobility and saturation velocity of the InGaAs materials (1). The device with high indium content can be used in low noise amplifier (LNA), which plays an important role in determining the sensitivity of the system performance. High gain and low noise figure with minimum power consumption are always preferred for low noise amplifier to be used in millimeter-wave applications.

From the technical point of view, package technology is very important for semiconductor devices used in high frequency applications. Packages can protect the integrated circuit from external hazards such as environmental influences, mechanical stress and humidity (2). The rapid growth of market in wireless communication applications requires packaging technology to be more compactness, low cost and high performances (3). Flip-chip is known as one of the most attractive approaches for chip-level packaging at millimeter-wave frequencies, which provides excellent performance due to lower interconnect parasitic effects as compared to the conventional wire-bonding (4). Flip-chip technique connects a die to a substrate using pillar bump which greatly shortens the signal transmission path and therefore enhances the electrical performances of the whole system (5, 6).

In the past, the packaging substrates used for high frequency applications were primarily provided by ceramics-based substrates such as alumina. However, cost considerations and limitations on ceramic substrates have pushed the industry to find new solutions (7). Many of today's low cost package types are not suited for high frequency applications. The electrical performance of packages has a determining impact on the behavior of applications, especially at W-band frequencies. The growing organic copper clad laminates' market has targeted to replace the ceramic substrates, specifically for plastic ball grid array (BGA). Therefore, the investigation of low-cost package with good performances at high operating frequencies is badly needed. Hence, this paper presents a flip-chip assembled MHEMT device on low-cost RO3210 organic substrate. DC characteristics and RF performances of the assembled MHEMT were measured up to W-band.

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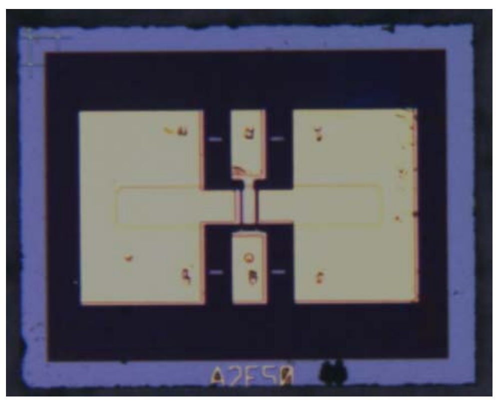
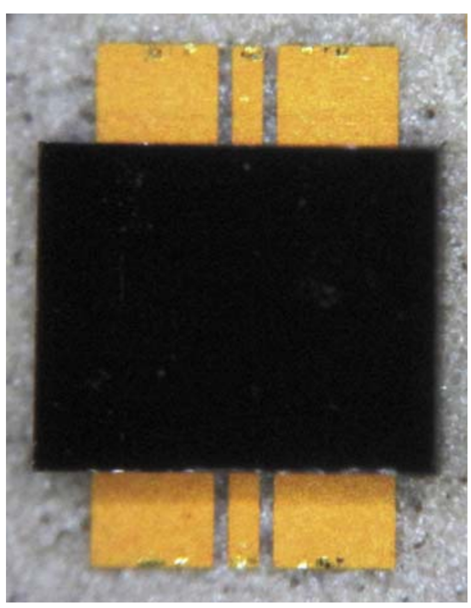
## Experiment

The epitaxial layer of the MHEMT was grown by MBE on 3-in GaAs substrate. The $In_{0.6}Ga_{0.4}As$ MHEMT device with 150 nm gate length was in-house fabricated and the process can be found in our previous report (8). The photolithography and electroplating process were used for fabricating RO3210 substrate in flip-chip assembly. First of all, the substrate was deposited with Ti/Au seed layers on the top surface with the thickness of 500 and 1000 Å. A thin photoresist was then applied on the substrate surface and exposed by UV light for CPW patterns. The 50 Ω CPW transmission line pattern was electroplated to 3 um thick in a cyanide-based gold plating bath. After electroplating, the remaining photoresist was removed with acetone solution.

After that, a thick layer photoresist was coated on the substrate with the thickness of 30 um. Then, the substrate was exposure by UV light and developed in a developer to obtain bump patterns. The gold bump was electroplated in the same cyanide-based solution. The remaining thick photoresist was removed by acetone solution. Next, the seed layers of Ti and Au were removed away with potassium iodide/iodine ($KI/I_2$) and hydrofluoric acid (HF) solutions. The MHEMT device was then flip-chip bonded on the substrate with optimized bonding parameters. The photographs of the MHEMT device before and after flip-chip assembly are shown in Figures 1(a) and 1(b).



(a)



(b)

Figure 1. Photographs of (a) InGaAs MHEMT bare die device and (b) flip-chip package device.

## Results and Discussion

Before the fabrication process, a 50 Ω CPW thru line as shown in Figure 2 was calculated and simulated by microwave calculator and HFSS simulation tool, respectively. The total length of the CPW line is 854 μm, which is exactly equal to the total length of the flip-chip assembled MHEMT as shown in Figure 1 (b). The CPW thru line was fabricated on RO3210 organic substrate for RF performance investigation. The fabricated CPW thru line was measured by using on wafer probing measurement with LRRM (Thru-Reflect-Reflect-Match) calibration. The RF measurements were performed in a frequency range from 2 to 110 GHz using HP 8510XF broadband vector network analyzer (VNA). Figure 3 compares the measured and simulated S-parameters in the frequency ranging from 2 to 110 GHz. Both measured and simulated insertion loss (S21) matched quite well with less than 0.7 dB difference up to 110 GHz. The measured data of CPW thru line was quite good with return loss below 20 dB up to 90 GHz. Overall, the organic substrate demonstrates low insertion loss and return loss at W-band frequencies.

Figure 4 presents the I-V characteristics of the flip-chip assembled MHEMT device on RO3210 substrate. The measurement result shows a high drain-source current, $I_{DS}$ = 516 mA/mm at a $V_{DS}$ = 0.8 V with $V_{GS}$ ranging from -1.4 to 0 V. The transconductance (Gm) is measured under two bias conditions at $V_{DS}$ of 0.5 and 0.8 V as illustrated in Figure 5. The highest Gm peaks were 576 and 600 mS/mm for the two bias conditions after flip-chip assembly. Besides, the device pinched-off quite well at various bias conditions. As can be observed in the figures, the IV curves and transconductances of bare die did not change much after flip-chip assembly. The good flip-chip packaged MHEMT device showed great performances after packaging, which may be attributed to the low contact resistance of interconnect between substrate and device.

Figure 6 shows the measured insertion gain up to 110 GHz. The insertion gain decayed less than 2 dB up to 100 GHz after flip-chip assembly. This is due to the low-loss signal transition between the substrate and device. The low noise performance of the MHEMT device measured from 18 to 64 GHz at a $V_{DS}$ bias of 0.7 V. The minimum noise figure ($NF_{min}$) with of less than 2 dB is obtained in this frequency range and illustrated in Figure 7. The associated gain ($G_a$) was above 5 dB up to 64 GHz at the same bias conditions. The results of bare die and flip-chip package show great performances in DC and RF characteristics also including noise figure from DC to 64 GHz. Therefore, this low-cost flip-chip packaging using RO 3210 organic substrate is suitable for low-noise applications up to W-band frequencies.

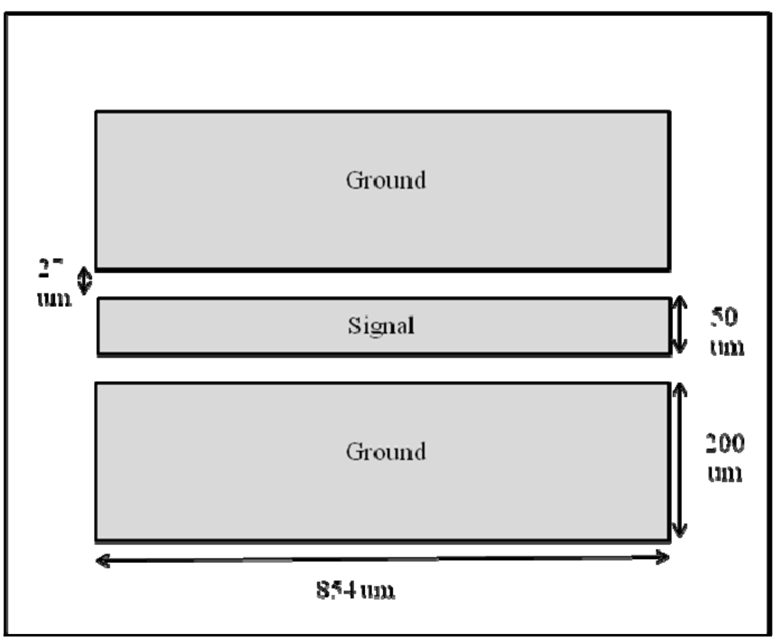



Figure 2. The dimension of CPW thru line with 50 Ω characteristic impedance.

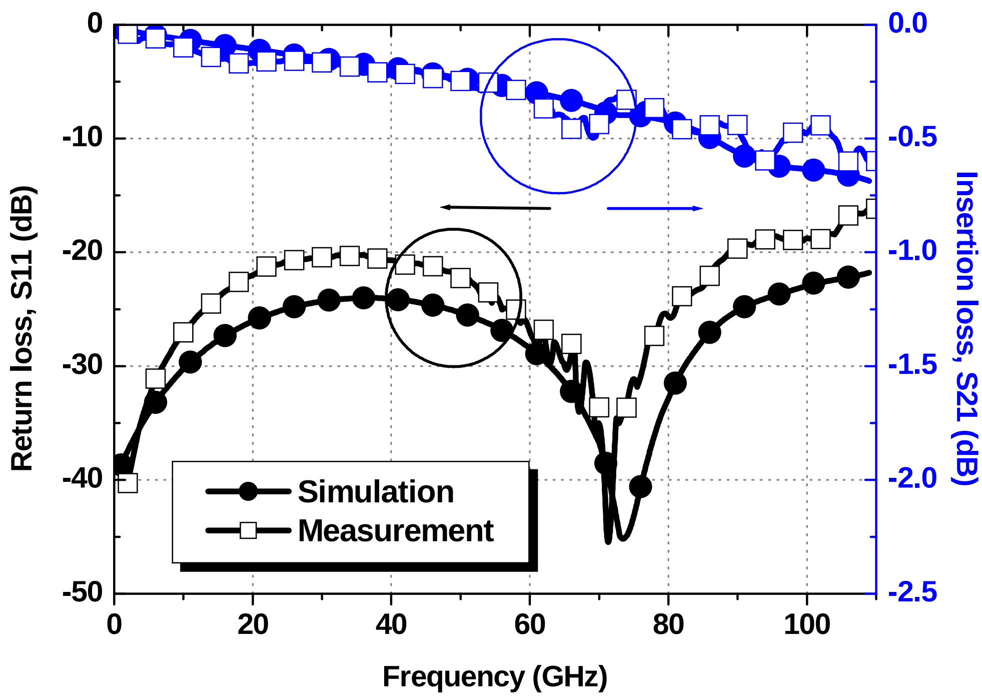



Figure 3. Comparison between the measured and simulated result of the CPW thru line on RO 3210 organic substrate.

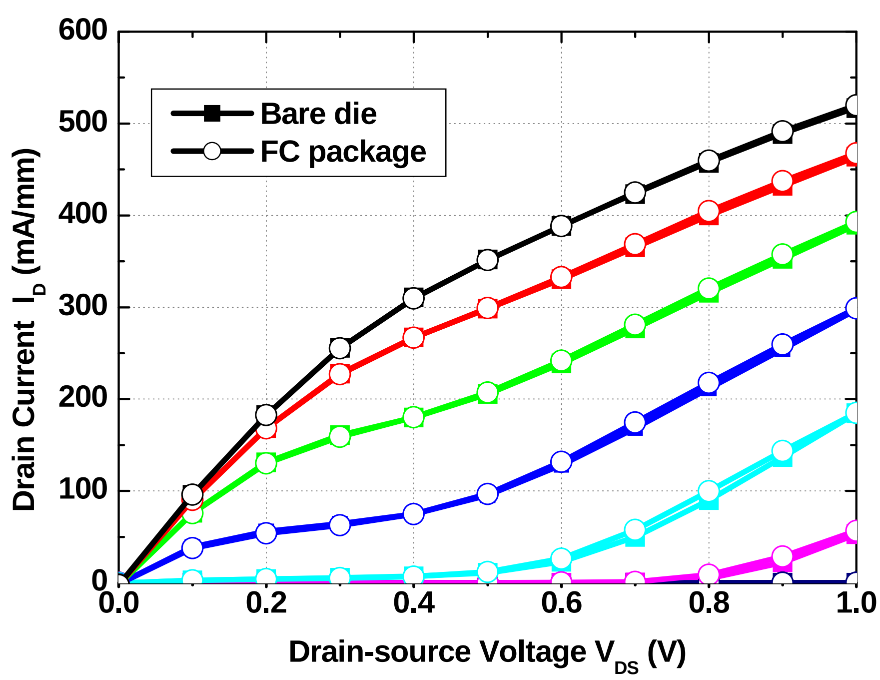



Figure 4. Measured IV characteristics of the bare die and after flip-chip package.

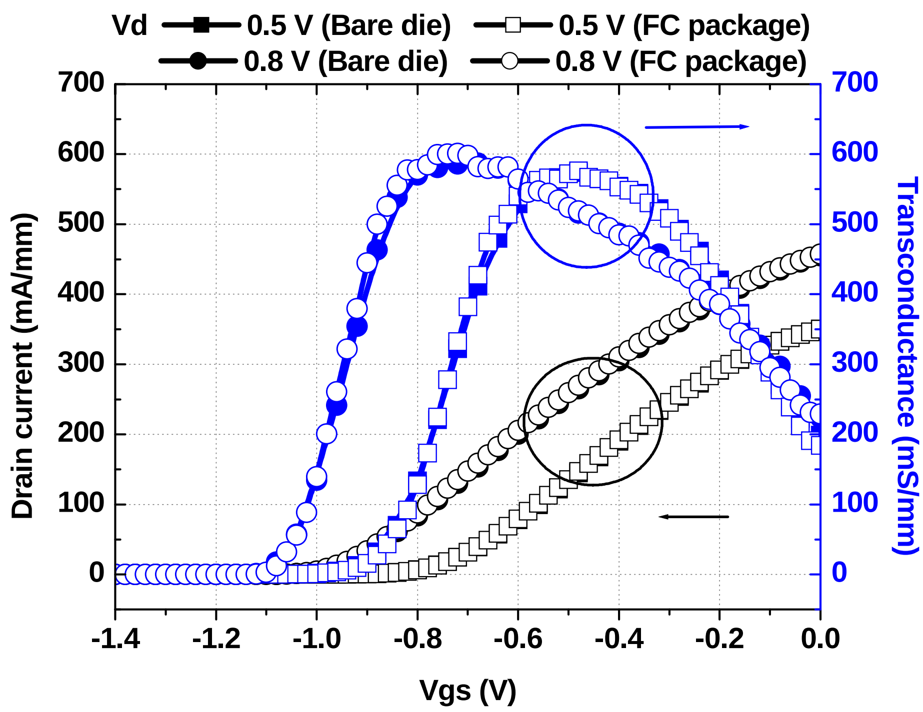



Figure 5. Transconductance ($G_m$) of the bare chip and packaged device at $V_{DS}$ = 0.5 V and 0.8 V.

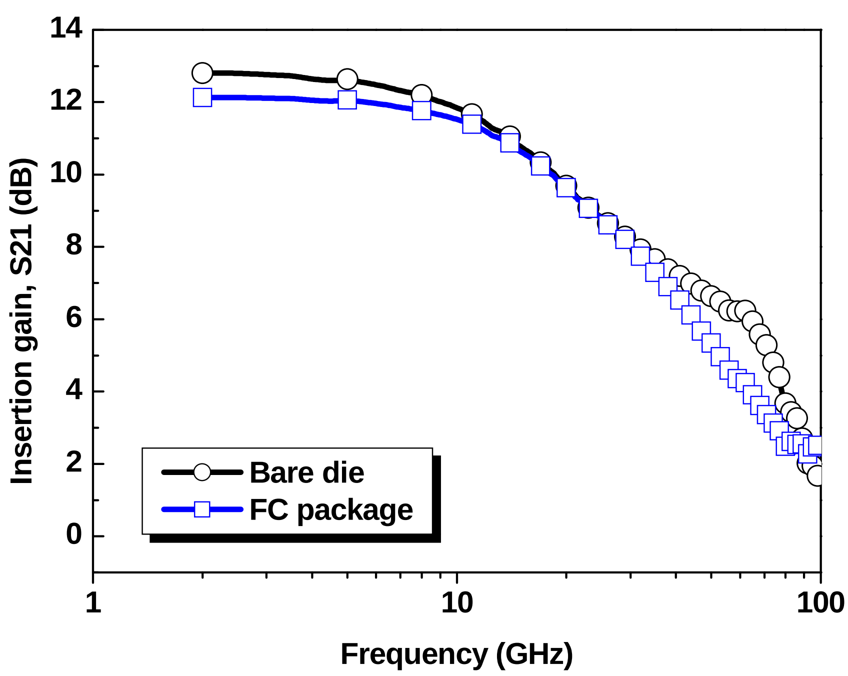



Figure 6. The insertion gain of flip-chip packaged MHEMT device on RO 3210 substrate at $V_{DS}$ = 0.8 V.

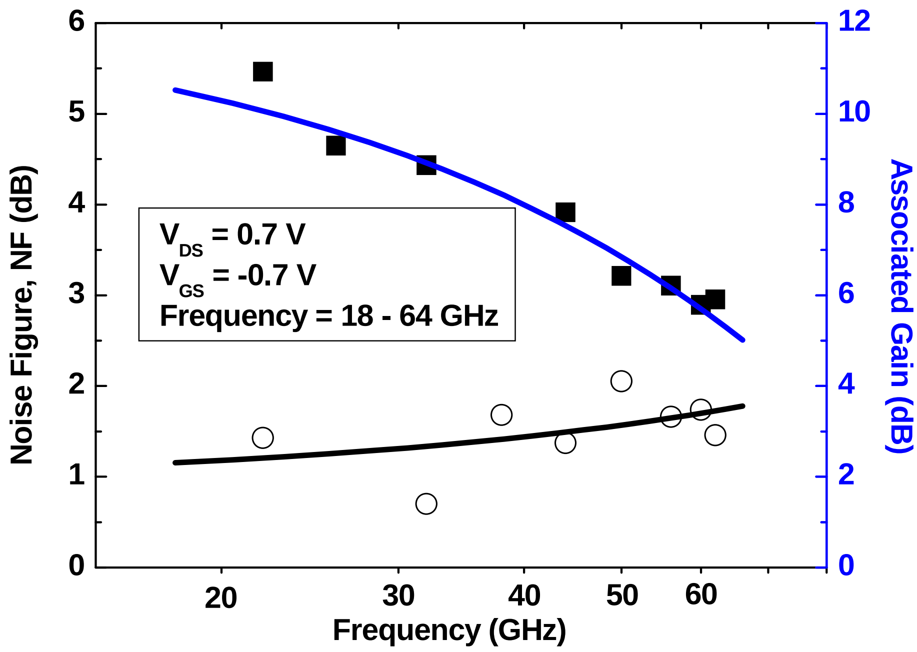



Figure 7. Measured noise figure and associated gain of the flip-chip packaged MHEMT.

## Conclusion

A 150 nm gate length $In_{0.6}Ga_{0.4}As$ MHEMT device was successfully fabricated and flip-chip assembled on low-cost RO3210 organic substrate. The measured DC and RF characteristics of the MHEMT device after assembly exhibited nearly similar performance as the bare die. The packaged device shows a high drain-source current of 516 mA/mm and a maximum transconductance of 600 mS/mm at $V_{DS}$ of 0.8 V, which is comparable to the performance of the bare die before assembly. In addition, the packaged device demonstrated good associated gain of above 5 dB and low noise figure of less than 2 dB from 18 to 64 GHz after flip-chip assembly. These results demonstrate the feasibility of using low-cost RO3210 substrate for flip-chip packaging of MHEMT devices for low-noise applications up to W-band frequencies.

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## References

1. B. H. Lee, D. An, M. K. Lee, B. O. Lim, S. D. Kim, and J. K. Rhee, IEEE EDL, Vol. 25, no. 12 (2004).
2. Wolfgang Heinrich, IEEE International Workshop on Radio-Frequency Integration Technology, (2005).
3. M. Ito, K. Maruhashi, K. Ikuina, N. Senba, N. Takahashi and K. Ohata, IEEE MTT-S, Vol. 1 (2000).
4. W. Heinrich, A. Jentzsch, and H. Richter, Electronics Letters, Vol. 37, No. 3 (2001).
5. Axel Tessmann and at al., IEEE MWCL, Vol. 14, No. 4 (2004).
6. S Kim, S Song, W Choi, S Lee, W KO, Y Kwon, K Seo, IEEE 16th IPRM (2004).
7. Hideki Kusamitsu and et al., IEEE Transactions on Electronics Packaging Manufacturing, Vol. 22, No. 1 (1999).
8. C. I. Kuo, H. T. Hsu, E. Y. Chang, Y. Miyamoto, and W. C. Tsern, Japan Journal of Applied Physics, vol, 47, no. 9, pp. 7119-7121, 2008.