Fault Models and Test Methods for Subthreshold SRAMs

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Abstract—Due to the increasing demand of an extra-low-power system, a great amount of research effort has been spent in the past to develop an effective and economic subthreshold SRAM design. However, the test methods regarding those newly developed subthreshold SRAM designs have not yet been fully discussed. In this paper, we first categorize the subthreshold SRAM designs into three types, study the faulty behavior of open defects and address decoders faults on each type of designs, and then identify the faults which may not be covered by a traditional SRAM test method. We will also discuss the impact of open defects and threshold-voltage mismatch on sense amplifiers under subthreshold operations. A discussion about the temperature at test is also provided.

Index Terms—SRAM, subthreshold, sub-V_{th}, testing, stability fault, open defect

1 Introduction

Lowering supply voltage is the most straightforward but effective method to reduce circuit's overall power consumption, which is especially suitable for those portable, power-limiting, and not-timing-critical applications such as wireless sensor systems and implanted biomedical chips. Previous works [1], [2] have shown that the most power-saving supply voltage falls around the subthreshold region for CMOS digital circuits and some subthreshold digital circuits have already been demonstrated in silicon successfully. Also, the performance degradation imposed by the subthreshold operations can be compensated by using proper parallel architecture [3], [4], which further extends the application of a subthreshold system.

In the process of developing a robust subthreshold system, operating SRAMs at a subthreshold voltage is more challenging than operating digital circuits. Under subthreshold operations, the typical 6T SRAM design needs to face the following two major problems: 1) decrease of the static noise margin and 2) decrease of the write margin [5], [6]. It means that a 6T SRAM bit-cell operating at subthreshold region is more vulnerable to the noise and at the same time harder to write. The detailed reasons of the above phenomenon were explicitly discussed in [6]. Also, in order to increase the write margin, the size of the pass transistors in a 6T SRAM bit-cell needs to be increased, which may further jeopardize the static noise margin. Thus, for a 6T SRAM bit-cell, a proper combination of the six transistors' sizes are extremely hard to obtained under subthreshold operations, especially when the local process variation of advanced process technologies may significantly change the device characteristics and in turn break the fragile balance between the currents of the six transistors for read, write, and hold operations. Previous results [7] have shown that the minimum supply voltage for operating a 6T SRAM design is 0.7 V based on a bulk CMOS 65 nm technology [8] and a dynamic-double-gate SOI technology.

To overcome the above two problems and successfully operate a SRAM at subthreshold region, several new SRAM bit-cell designs [9], [10], [11], [12], [13], [14], [15], [16] were proposed. Tackling the weak static noise margin, [9], [10], [11], [14], [15] utilized an extra read path (in addition to the original pass transistors) in their SRAM designs to isolate the cross-coupled inverters from the bit-lines during a read operation, which can effectively avoid potential half select or deceptive read destruction. Tackling the inability to write, techniques were utilized to either strengthen the driving capability of the pass transistors or loose the hold ability of the cross-couple inverters during the write operation. To achieve the former one during a write operation, Calhoun and Chandrakasan [9] specified a boosted word-line voltage to access the pass transistors and Kim et al. [16] designed the pass transistor in a way that its reverse short channel effect can be utilized under subthreshold operations. To achieve the latter one during a write operation, Singh et al. [13] broke the loop of the cross-coupled inverters with additional transistors and Zhai et al. [12], Chang et al. [14], Chang and Hwang [15] destroyed the functionality of one or both inverters by adjusting the voltage at its virtual ground and/or virtual VDD.

Although a significant amount of research effort has been put into the area of developing an effective and economic subthreshold SRAM design, however, the testing methodologies for those new subthreshold SRAM designs have not been fully discussed in the literature yet. In this

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TABLE 1
Categorization of Subthreshold SRAM Designs

Type	Q1	Q2	Sub-Vt-SRAM designs
A	Yes	Yes	[9][10][11]
B	No	Yes	[12][13]
C	Yes	No	[14][15]
D	No	No	Typical 6T SRAM

paper, we will first categorize the new subthreshold SRAM designs into three types based on their design characteristics. For each type of subthreshold SRAM designs, we will then discuss the fault models associated with open defects and identify the faults which may or may not be easily detected by a traditional SRAM test algorithm. We will further discuss the corresponding test methodologies for each of the above hard-to-detect faults. Also, we will discuss the faulty behavior of address decoder faults (ADFs) on those new subthreshold SRAMs and show their difference to the address decoder faults on the traditional 6T SRAM. Next, we will discuss the impact of open defects and V_{th} mismatch on sense amplifiers (SA) and compare their differences between subthreshold operations and superthreshold operations. A short discussion about the test temperature is provided as well. All the experimental results are collected from the simulation using an UMC 65 nm low-leakage process technology.

2 Categorization of Subthreshold SRAM Designs

The fault models of a subthreshold SRAM design is associated with its bit-cell structure, and so are their test methodologies. In this section, we categorize the subthreshold designs [9], [10], [12], [13], [11], [14], [15] based on the following two criteria regarding the bit-cell structure (Q1 and Q2). The later discussion about the fault behaviors will be based on the result of this categorization.

- Q1: Is its read path different from its write path?
- Q2: Does the design use a single-ended sense amplifier?

Based on Q1 and Q2, the subthreshold SRAM designs can be divided into Types A, B, C, and D as shown in Table 1. In fact, Type D represents the bit-cell sharing the read/write paths and utilizing a differential sense amplifier, i.e., the traditional 6T SRAM design. Thus, our later discussion will focus on the fault models and test methods only for the designs in Types A, B, and C. Note that the reason why Q1 and Q2 are used for categorization is because these two criteria can divide the subthreshold SRAM designs into categories that result in similar faulty behaviors.

In order to analyze their fault models, we used a UMC 65 nm low-leakage process to implement each of the above bit-cell designs in a 128×32 array (128 bit-cells at a bit-line and 32 bit-cells at a word-line), including write drivers and sense amplifiers. Each row contains only one word and the word size is 32-bit. Under the defect-free condition, we first identified the minimum required cycle time for correct read or write operations at the TT corner and $25°\mathrm{C}$, and then defined the cycle time as 20 percent longer than the minimum required cycle time for each bit-cell design. On top of a defect-free design, we will later inject open defects and simulate whether the faulty design can function correctly within the defined cycle time. A defect is detected if the result of the sense amplifier reports the wrong value.

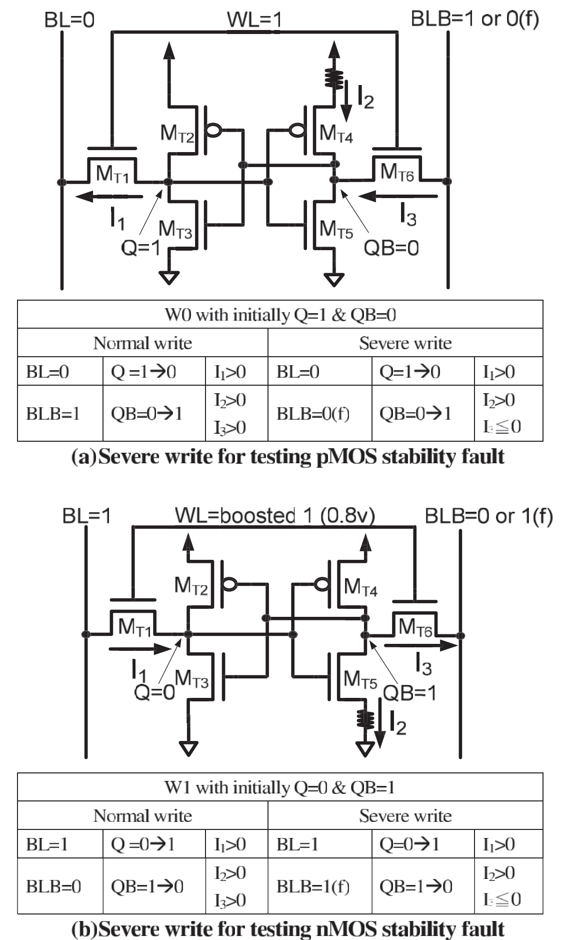

Fig. 1. Illustration of severe write.

3 Test Methods for Stability Faults

3.1 Background of Stability Faults

A *stability fault* defined in [17], [18], [19], [20] refers to a small open defect on the source/drain of the four cross-coupled transistors, which may not fail a read or write operation under a typical operating condition but may fail under some corner conditions (such as significant IR drop, noise, or soft error). As a result, a stability fault may decrease the reliability of the SRAM but may not be easily detected by a conventional march sequence. Therefore, testing stability faults has become one of the most challenging task in current SRAM testing. Several test methods were proposed to detect the stability faults with as small resistance as possible [17], [18], [19], [20].

For traditional 6T SRAMs, the past research effort mainly focused on the stability faults located on the source/drain of the pull-up pMOS transistors (such as M_{T2} and M_{T4} in Fig. 1) and ignored the stability faults locating on the pull-down nMOS transistors (such as M_{T3} and M_{T5} in Fig. 1), which can be detected relatively easily by a read operation

because the bit-lines in general SRAMs are precharged to VDD during a read operation. If the nMOS transistors cannot successfully pull down a bit-line due to the open defects, then the precharged value (floating 1) will be read out, which is opposite to the expected value. On the other hand, if the pMOS transistors cannot successfully pull up the bit-line due to an open defect, then the precharged value (floating 1) just happens to be the expected value and hence the open defect cannot be detected.

However, for subthreshold SRAM designs, the read path can be separated from the write path, meaning that the weak pull-down ability of nMOS transistors will not directly affect the voltage at RBL during a read operation. Therefore, the importance of detecting the stability faults on the pull-down nMOS transistors (M_{T2} and M_{T4}) become more significant for subthreshold SRAM design than that for traditional 6T SRAMs. In this paper, we will validate the effectiveness of the following test methods for defecting the stability faults locating on both the pMOS and nMOS transistors of subthreshold SRAMs. These testing methods include: 1) read equivalent stress, 2) severe write, and 3) low-V-write/high-V-read.

3.2 Read Equivalent Stress

The idea of the read equivalent stress in the 6T SRAM design is to perform consecutive read operations to a designated bit-cell such that its word-line kept opened and its data stored by the cross-coupled inverters can be constantly attacked by the precharged VDD (floating 1) at bit-lines [17], [21]. However, for the subthreshold SRAMs which utilizes a different read path from its write path (such Type-A and Type-C), a read operation will turn on only its read word-line but not its write word-line. Such a read operation cannot attack the stored data and detect stability faults. Thus, to be able to apply read equivalent stress for Type-A and Type-C subthreshold SRAMs, specialized DFT circuit is required to turn on the write word-line and apply floating 1 at write bit-lines during a read operation at the test mode.

3.3 Severe Write

The idea of severe write in the 6T SRAM design is to perform a write operation by setting BL and BLB to floating 0 and strong 0 at the test mode, instead of strong 1 (or floating 1) and strong 0 at the normal mode (as shown in Fig. 1) [20]. With such a write operation, successfully writing in data becomes more difficult since the floating 0 is opposite to the target value at Q or QB. As a result, if an open defect falls on the source/drain of pMOS transistors (such as M_{T2} and M_{T4}) and weakens the pull-up ability of an inverter, then the severe-write operation will fail to write the correct data and hence detect the open defect. Fig. 1a illustrates how a severe write helps to detect an open defect on the pMOS transistor M_{T4}.

In fact, the above severe write (floating 0 and strong 0) can only detect open defects on pMOS transistors. To detect the stability faults on nMOS transistors, a severe write should set BL and BLB to floating 1 and strong 1. However, the nMOS pass transistors (M_{T1} and M_{T6}) are not suitable for passing a value 1, especially when operating at the subthreshold region (0.4 V in our cases). Such a severe write cannot correctly write a data even when no defect exists in

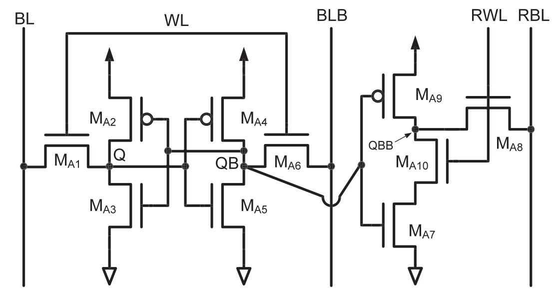

Fig. 2. First Type-A subthreshold SRAM design [9].

the subthreshold SRAM. Therefore, in order to use a severe write to detect stability faults on nMOS transistors, we need to boost the voltage at WL by another V_t (0.8 V in our case) to enhance the ability of passing a value 1 through the nMOS pass transistors during the test mode, which also requires extra DFT circuitry to realize. Fig. 1b illustrates how this refined version of severe write can help the detection of an open defect on the nMOS transistor M_{T5}.

3.4 High-V-Write/Low-V-Read

The idea of low-V-write/high-V-read is similar to the severe write, which increases the difficulty of a write operation such that the degradation of pull-up or pull-down capability caused by an open defect may fail to write the correct data. At the same time, we also need to make sure that this difficult condition for write will not fail the design without any defect. It means that the low operating voltage for write cannot be too far away from the normal voltage. Also, changing the operating voltage on test equipments takes a significant amount of time (around 10 micro seconds in our experience). Thus, we need to apply the low-V write to each word, change the operating voltage to normal, and then read each word. A high-V read immediately after a low-V write is not allowed due to its large overhead on test-application time.

4 Analysis of Open Defects in Type-A Subthreshold SRAMs

4.1 Design Overview of Type-A Subthreshold SRAMs

According to the categorization, Type-A subthreshold SRAM designs utilize a single-ended sense amplifier for read and build an extra read path in addition to the traditional 6T SRAM, which can protect the value stored in the cross-coupled inverters during read operations and improve its read SNM to the same level as its hold SNM. Fig. 2 shows the first Type-A subthreshold SRAM design [9], where M_{A1} to M_{A6} represent the transistors in the traditional 6T SRAM and M_{A7} to M_{A10} represent the transistors in the read path. In this design, the original word-line (WL), bit-line (BL), and bit-line-bar (BLB) are only used for write operations. The new read word-line (RWL) and single-ended read bit-line (RBL) are only used for read operations. During a read operation, the value stored at QB (Q bar) will determine the value at QBB (Q bar bar) through an inverter (formed by M_{A7}, M_{A9}, and M_{A10}), and then determine the value at RBL. Also, the value of QBB is kept at 1 (VDD) or floating during the hold mode to reduce the leakage current of M_{A8} to RBL.

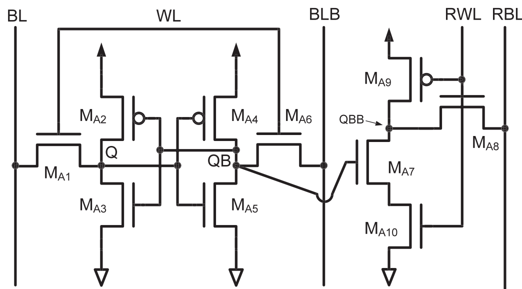

Fig. 3. Second Type-A subthreshold SRAM design [10].

Fig. 3 shows the second Type-A subthreshold SRAM design [10]. Similar to Calhoun and Chandrakasan [9], Kim et al. [10] also use four transistors (M_{A7} to M_{A10}) to build an extra read path. However, its QBB is always kept at 1 during the hold mode since the M_{A9} in [10] is controlled by RWL instead of QB. When reading a value 0 out, QBB is pulled down through the path formed by M_{A7} and M_{A10}. However, when reading a value 1 out, QBB is floating since M_{A9} is turned off by RWL. As a result, the precharged floating 1 at RBL will be read out.

Fig. 4 shows the third Type-A subthreshold SRAM design [11], which uses two transistors and one extra signal (named *buffer-foot*) to build the extra read path. During read, the signal buffer-foot is set to GND and hence its read mechanism is the same as [10]. It means that QBB is 0 and floating when reading 0 and 1, respectively. During hold, the signal buffer-foot is set to VDD, meaning that QBB is either 1 or floating based on the value of QB.

4.2 Impact of Open Defects on Type-A Subthreshold SRAMs

In the following experiments, we inject an open defect with different resistances on each terminal (gate or source/drain) of each transistor and report the minimum resistance which can cause a failure on a read operation or a write operation for Type-A subthreshold SRAM designs. Table 2 lists the minimum detectable resistance of each open defect (in Column 5) and the operation which the defect cause a failure at (in Column 4). Note that the result reported in Table 2 is obtained based on the first Type-A design [9] at the TT corner and 25°C. A similar result can be obtained for the other two Type-A designs [10], [11]. In addition, once a defect can generate a read failure or write failure, this defect can be easily detected by a conventional SRAM march sequence. Therefore, we only need to consider the open defects with a faulty resistance less than the minimum detectable resistance.

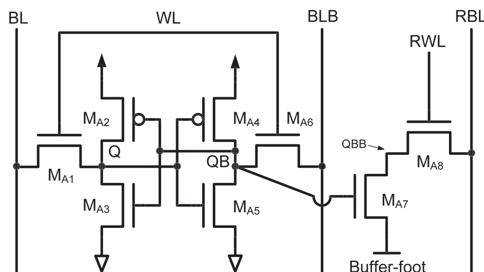

Fig. 4. Third Type-A subthreshold SRAM design [11].

TABLE 2
Faulty Behavior of Open Defects on Type-A Designs (Figs. 2, 3, and 4)

Transistor property	Transistor name	Transistor terminal	Faulty behavior	min detectable resistance
write pass transistor	M_{A1}	G	W0 fail	482MΩ
		S/D	W0 fail	3.8MΩ
	M_{A6}	G	W1 fail	500MΩ
		S/D	W1 fail	3.2MΩ
pull-up pMOS	M_{A2}	G	W0 fail	900MΩ
		S/D	W1 fail	60MΩ
	M_{A4}	G	W1 fail	800MΩ
		S/D	W0 fail	60MΩ
pull-down nMOS	M_{A3}	G	W1 fail	370MΩ
		S/D	-	∞
	M_{A5}	G	W0 fail	370MΩ
		S/D	-	∞
read pass transistor	M_{A8}	G	R0 fail	200MΩ
		S/D	R0 fail	16.9MΩ
read-path pull-down1	M_{A7}	G	R0 fail	440MΩ
		S/D	R0 fail	5.1MΩ
read-path pull-down2	M_{A10}	G	R0 fail	240MΩ
		S/D	R0 fail	5.1MΩ
read-path QBB set	M_{A9}	G	R0 fail	2GΩ
		S/D	-	∞

As Table 2 shows, the open defects locating on the original 6T bit-cell (M_{A1} to M_{A6}) all fail on a write operation. The open defects locating on the source/drain of the four cross-coupled transistors (M_{A2} to M_{A5}) are first highlighted by a gray background color in Table 2. Those defects are classified as a stability fault in Section 3. Opposite to traditional 6T superthreshold SRAMs, no stability faults on the nMOS transistors (M_{A3} and M_{A5}) can be detected, but the stability faults on the pMOS transistors can be detected with a 60 MΩ minimum detectable resistance for Type-A designs. This result demonstrates that detecting the stability faults on nMOS transistors is more critical than that on pMOS transistors for Type-A designs. Also, all open defects on the gate of the six transistor (M_{A1} to M_{A6}) have a minimum detectable resistance larger than 370 MΩ, and hence are also relatively hard to detect.

On the other hand, the open defects locating on the extra read path (M_{A7} to M_{A10}) all fail on a read-0 operation. Also, the open defects on both gate and source/drain of M_{A9} are almost undetectable even though those open defects may reduce the ability of pulling up QBB. However, the read-1 operation do not rely on M_{A9} to pull up RBL and hence the malfunction of M_{A9} can hardly fail a read operation. For M_{A7}, M_{A8}, and M_{A10}, the open defects on their gate is harder to detect than those on their source/drain.

4.3 Effectiveness of Test Methods for Type-A Designs

In the following experiment, we attempt to reduce the minimum detectable resistance of each stability fault by applying 1) read equivalent stress (denoted as *RES*), 2) severe write, and 3) low-V-write/high-V-read (denoted as *LVW-HVR*) to Type-A subthreshold SRAM designs. Note that the

TABLE 3
Effectiveness of Test Methods for Detecting STFs in Type-A Designs

Transistor property	Transistor name	W+R	RES	Severe W	LVW-HVR (0.36V)
pull-up pMOS	M_{A2}(S/D)	60MΩ	∞	6.6MΩ	39.4MΩ
	M_{A4}(S/D)				
pull-down nMOS	M_{A3}(S/D)	∞	790MΩ	4.3MΩ	∞
	M_{A5}(S/D)				

read equivalent stress performed in this experiment will not stop repeating read operations until the minimum detectable resistance can hardly be decreased, which usually takes less than 10 repeated read operations. Also, the operating voltage for write and read in low-V-write/high-V-read is 0.36 V and 0.4 V, respectively. Table 3 reports the minimum detectable resistance achieved by each test method. In Table 3, the test method *W+R* means a simple read operation after a write operation, which will actually achieve the same minimum detectable resistance as listed in Table 2.

As Table 3 shows, severe write outperforms the other two test methods by achieving a $6.6\ \mathrm{M}\Omega$ minimum detectable resistance for pMOS stability faults and a $4.3\ \mathrm{M}\Omega$ minimum detectable resistance for nMOS stability faults. Meanwhile, read equivalence stress cannot detect any pMOS stability faults and its minimum detectable resistance for nMOS stability faults is still high ($790\ \mathrm{M}\Omega$). Note that the read equivalence stress performs even worse than the simple read after write (W+R) for pMOS stability faults. This is because the W+R fails at its write operation but the read equivalent stress assumes that its initial value can be successfully written. Also, the low-V-write/high-V-read cannot detect any nMOS stability faults. In fact, if the boosted WL used in severe write is set to 0.7 V, the minimum detectable resistances will be further decreased to the order of hundred-kΩ. However, if the boosted WL is set to 0.6 V, no data can be written into the bit-cell even when no defect exists. Thus, defining a proper boosted voltage at WL is a critical factor when using severe write.

In addition, the severe write and LVW-HVR can also help to reduce the minimum detectable resistance at the gate of M_{A1} to M_{A6}, while read equivalent stress cannot. Table 4 shows the corresponding results, in which LVW-HVR achieves a lower minimum detectable resistance at the gate of write pass transistors and pull-up pMOS transistors (M_{A1}, M_{A2}, M_{A4}, and M_{A6}) while the severe write achieves a lower minimum detectable resistance at the gate of pull-down nMOS transistors (M_{A3} and M_{A5}). Overall, severe write is still the most effective test method for Type-A designs since it can cover open defects at the most places.

TABLE 4
Effectiveness of Test Methods for Detecting Fail-to-Write Gate Open Defects in Type-A Designs

Transistor property	Transistor name	W+R	RES	Severe write	LVW-HVR (0.36V)
write pass transistor	M_{A1}(G)	482MΩ	∞	350MΩ	32.4MΩ
	M_{A6}(G)	500MΩ	∞	420MΩ	29.9MΩ
pull-up pMOS	M_{A2}(G)	900MΩ	∞	180MΩ	60MΩ
	M_{A4}(G)	800MΩ	∞	200MΩ	60MΩ
pull-down nMOS	M_{A3}(G)	370MΩ	∞	110MΩ	260MΩ
	M_{A5}(G)	370MΩ	∞	230MΩ	290MΩ

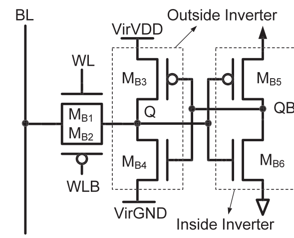

Fig. 5. First Type-B subthreshold SRAM design [12].

5 Analysis of Open Defects in Type-B Subthreshold SRAMs

5.1 Introduction of Type-B Subthreshold SRAMs

According to the categorization shown in Table 1, a Type-B subthreshold SRAM design utilizes a single-ended sense amplifier for read and its read operations share the same path with its write operations. Such a bit-cell structure implies that its write operation is performed through a single bit-line as well, which further increases the difficulty of a write operation. Thus, in order to successfully write data through a single bit-line, Type-B subthreshold SRAM designs heavily rely on the design techniques which can effectively reduce the hold ability of the cross-coupled inverters during the write operation.

Fig. 5 shows the first Type-B subthreshold SRAM design [12], which can adjust the hold ability of the cross-coupled inverters by controlling the voltage at virtual VDD ($VirVDD$) and virtual GND ($VirGND$). During a read operation or the hold mode, $VirVDD$ and $VirGND$ are set to VDD and GND as general SRAMs. During a write operation, $VirVDD$ and $VirGND$ will become an offset lower and an offset higher, respectively, which can break the outside inverter (formed by M_{B3} and M_{B4}) and allows the voltage at Q to be directly affected by BL. Also, this design [12] utilizes a pMOS pass transistor (M_{B2}) in addition to a normal nMOS pass transistor (M_{B1}) simultaneously, such that both 1 and 0 can effectively passed through either M_{B2} or M_{B1}.

Fig. 6 shows the second Type-B subthreshold SRAM design [13], which decreases the hold ability during a write

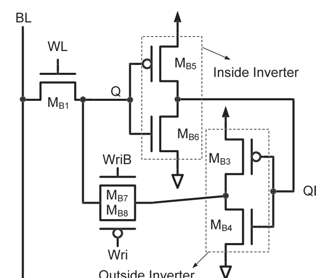

Fig. 6. Second Type-B subthreshold SRAM design [13].

TABLE 5
Faulty Behavior of Open Defects on Type-B Designs (Figs. 5 and 6)

Transistor property	Transistor name	Transistor terminal	Faulty behavior	min detectable resistance
write pass transistor	M_{B1}	G	W0/R0 fail	2GΩ
		S/D	R0 fail	6.4MΩ
	M_{B2}	G	W1 fail	590MΩ
		S/D	W1 fail	7.6MΩ
outside pull-up pMOS	M_{B3}	G	W0 fail	4GΩ
		S/D	-	∞
inside pull-up pMOS	M_{B5}	G	W0 fail	870MΩ
		S/D	W0 fail	160MΩ
outside pull-down nMOS	M_{B4}	G	W1 fail	2GΩ
		S/D	R0 fail	900kΩ
inside pull-down nMOS	M_{B6}	G	W1 fail	970MΩ
		S/D	W1 fail	120MΩ
cross-coupled loop switch	M_{B7}	G	W1 fail	2GΩ
		S/D	R0 fail	45.8MΩ
	M_{B8}	G	W0 fail	29GΩ
		S/D	-	∞

operation by breaking the loop of the cross-coupled inverters through the control signals Wri and $WriB$ (at M_{B8} and M_{B7}). Once the loop is broken, the value at BL can be easily written into the bit-cell. After the write operation, the loop of the cross-coupled inverters will be recovered as normal.

5.2 Impact of Open Defects on Type-B Subthreshold SRAMs

Table 5 lists the minimum detectable resistance and the corresponding faulty behavior of each open defect in Type-B designs. As Table 5 shows, the open defect at the source/drain of M_{B4} does not cause a stability fault since the open defect falls on the path of read-0 and can be easily detected by a read-0 operation (with a 900 kΩ minimum detectable resistance). Also, the stability fault at the outside pull-up pMOS M_{B3} is harder to detect than that at the inside transistors M_{B5} and M_{B6}. This is because the outside inverter is either destroyed or disconnected during a write operation, so that the value at Q is always correct. Even if a defect occurs on the outside pMOS M_{B3}, its weak pull-up ability will not lead to a wrong value at Q since the value at Q is already set by BL. However, if a defect occurs on the inside inverter, its weak pull-up or pull-down ability may delay the signal at QB and in turn result in a conflict at Q.

Table 5 also shows that the open defects on the gate and source/drain of M_{B8} can hardly be detected, implying that the design [13] may not really need a pMOS transistor to pass a value 1 at the outside inverter's output to Q when the cross-coupled loop is reconnected right after a write operation. In addition, the minimum detectable resistance at each transistor's gate is still high and hence the corresponding open detect is also hard to detect.

5.3 Effectiveness of Test Methods for Type-B Designs

Table 6 reports the minimum detectable resistance achieved by each test method for each stability fault in Type-B designs. Note that the severe write can only be applied to the design utilizing differential write mechanism (with BL and BLB), and hence cannot be applied to Type-B designs, which uses only one bit-line for write. As Table 6 shows, only read equivalent stress can detect the most hard-to-detect stability fault (at M_{B3}) in Type-B designs. This is because, by breaking the hold ability of the cross-coupled inverters, write 1 to Q is easy. As a result, detecting stability fault at M_{B3} cannot be achieved by using a weak write. We can only rely on read operations to detect it. Also, read equivalent stress can reduce the minimum detectable resistance of the other two stability faults. In addition, LVW-HVR cannot effectively reduce the minimum detectable resistance at transistors' gate for Type-B designs as it does for the Type-A designs. Table 7 shows the corresponding result at each transistor's gate. Therefore, read equivalent stress is more preferable than LVW-HVR for Type-B designs overall.

TABLE 6
Effectiveness of Test Methods for Detecting STFs in Type-B Designs

Transistor property	Transistor name	W+R	RES	LVW-HVR	
				0.38V-W	0.36V-W
pull-up pMOS	M_{B3}(S/D)	∞	300kΩ	∞	< 0
	M_{B5}(S/D)	160MΩ	160MΩ	150MΩ	< 0
pull-down nMOS	M_{B6}(S/D)	120MΩ	62MΩ	43.7MΩ	< 0

In Table 5, open defects on the source/drain of M_{B1}, M_{B4}, and M_{B7} may result in a read-0 fail. Since Type-B designs use a single read path and BL is precharged to floating 1 for a read operation, a read-1 operation will never fail by an open defect on the bit-cell. In fact, the worse case of performing a read-0 operation occurs when the value of all other bit-cells at the same BL is set to 1, such that the leakage current from M_{B1} and M_{B2} can prevent the BL from being pulled down by the accessed bit-cell. Also, the devices need to be in the FF corner and operated at a high temperature. Such a condition can result in a more significant leakage current, even though the pull-down capability of the targeted read path is also increased at a higher temperature (will discuss more in Section 9).

TABLE 7
Effectiveness of Test Methods for Detecting Fail-to-Write Gate Open Defects in Type-B Designs

Transistor property	Transistor name	W+R	LVW-HVR (0.38V-W)
write pass transistor	M_{B1}(G)	2GΩ	2GΩ
	M_{B2}(G)	590MΩ	410MΩ
pull-up pMOS	M_{B3}(G)	4GΩ	3GΩ
	M_{B5}(G)	870MΩ	790MΩ
outside pull-down nMOS	M_{B4}(G)	2GΩ	430MΩ
inside pull-down nMOS	M_{B6}(G)	970MΩ	410MΩ
cross-coupled loop switch	M_{B7}(G)	2GΩ	3GΩ
	M_{B8}(G)	29GΩ	190GΩ

TABLE 8
Impact of Using Different Backgrounds when Testing Fail-to-Read Open Defects in Type-B Designs

Transistor name	Same background	Opposite background
M_{B1}(S/D)	∞	8.1MΩ
M_{B4}(S/D)	∞	90kΩ
M_{B7}(S/D)	150MΩ	20.4MΩ

In the following experiment, we attempt to observe the impact of setting the data of all other bit-cells at the same BL to the same value (0) or the opposite value (1) to the accessed bit-cell when performing a read-0 operation in Type-B designs. Table 8 lists the minimum detectable resistance of the three read-0-fail open defects with both background settings. The simulation is conducted based on the FF corner at 75°C. As the result shows, with the same data background, a large open defect may not be even detectable since the leakage at the same BL can help to pull down the data. With the opposite background, the minimum detectable resistance can be significantly reduced. Note that we have tried a similar experiment to Type-A designs but its difference of using different backgrounds is limited.

To apply this all-1 background for a read-0 operation at each bit-cell, the march sequence in use needs to include the march element ($w0$, $r0$, $w1$). This march element can generate a read 0 out of a all-1 BL background and then recover the target bit-cell to 1, such that the background can remain all 1 when moving to the next address. Note that the march element ($w0$, $r0$, $w1$) is not included in a conventional SRAM march sequence, such as March C-.

6 Analysis of Open Defects in Type-C Subthreshold SRAMs

6.1 Introduction of Type-C Subthreshold SRAMs

According to the categorization shown in Table 1, a Type-C subthreshold SRAM design utilizes a differential sense amplifier for read and its read path is different from its write path. It means that each of Q and QB needs to be read out through a different extra read path to BL or BLB instead of through the pull-up or pull-down paths of the cross-coupled inverters. Once the read paths are independent from the cross-coupled inverter, the read static noise margin can be protected. Also, Type-C subthreshold SRAM designs utilize a virtual GND to destroy the original stored data and improve its write ability.

Fig. 7 shows the first Type-C subthreshold SRAM design [14], which embeds a 6T-SRAM design (with M_{C2}, M_{C4}, M_{C5}, M_{C6}, M_{C7}, and M_{C8}) in the center and one extra read path on a side to read out the value of Q (with M_{C1} and M_{C3}) or QB (with M_{C9} and M_{C10}). Also, two word-lines ($WL1$ and $WL2$) are used in this design. During a read operation, $WL1$ is set to 0 and $WL2$ is set to 1. Then, the precharged BL will be pulled down by M_{C3} if $Q = 1$ and will remain floating 1 if $Q = 0$, meaning that the value read out from BL (or BLB) is different from the value at Q (or QB). During a write operation, both $WL1$ and $WL2$ are set to 1 and virtual GND is pulled up to VDD, which changes

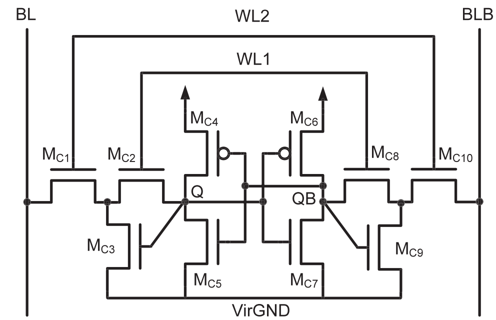

Fig. 7. First Type-C subthreshold SRAM design [14].

the original stored value at Q and QB to a voltage around 0.5 VDD and provides a weaker initial value at the cross-coupled inverters for write. After the write operation, the virtual GND will be pulled down to GND, which separates the voltages at Q and QB further apart. During the hold mode, both $WL1$ and $WL2$ are set to 0.

Fig. 8 shows the second Type-C subthreshold SRAM design [15], which further improves the first Type-C design [14] with the following modification. In [15], its BL is connected to the output of the inverter formed by M_{C6} and M_{C7} (through M_{C1} and M_{C2}) instead of that by M_{C4} and M_{C5}. Similarly, its BLB is connected to the output of the inverter formed by M_{C4} and M_{C5} (through M_{C8} and M_{C10}). As a result, the value read out at BL will be the same as the value at Q. Also, during its hold mode, $WL2$ is set to 0 but $WL1$ is set to 1. Under this setting of word-lines, M_{C3} or M_{C9} can help to pull down QB or Q during the hold mode, which can further increase its hold ability. In addition, because the value at Q equals to the value at BL during a read operation, the leakage of M_{C2} in [15] can be significantly reduced when compared to [14]. Similar situation applies to the leakage of M_{C8} during a read operation. Since [15] is a more refined version of [14], we will only consider the case of [15] in our later discussion regarding Type-C subthreshold SRAM designs.

6.2 Impact of Open Defects on Type-C Subthreshold SRAMs

Table 9 lists the minimum detectable resistance and the corresponding faulty behavior of each open defect in Type-C designs. As Table 9 shows, the stability faults on the nMOS transistors M_{C5} and M_{C7} cannot be detected at all. However, the stability faults on the pMOS transistors M_{C4} and M_{C6} are relatively easy to detect (with 11 MΩ minimum detectable

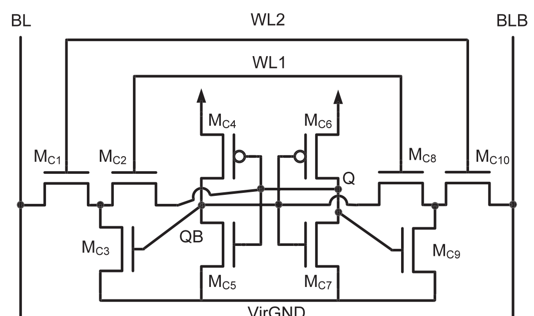

Fig. 8. Second Type-C subthreshold SRAM design [15].

TABLE 9
Faulty Behavior of Open Defects on Type-C Designs (Figs. 7 and 8)

Transistor property	Transistor name	Transistor terminal	Faulty behavior	min detectable resistance
write only pass transistor	M_{C2} & M_{C8}	G	W1 fail	58MΩ
		S/D	W1 fail	16MΩ
write/read pass transistor	M_{C1} & M_{C10}	G	R1 fail	39MΩ
		S/D	R1 fail	2MΩ
pull-up pMOS	M_{C4} & M_{C6}	G	W1 fail	64MΩ
		S/D	W0 fail	11MΩ
pull-down nMOS	M_{C5} & M_{C7}	G	W1 fail	410MΩ
		S/D	-	∞
read-path pull-down	M_{C3} & M_{C9}	G	W1 fail	170MΩ
		S/D	R1 fail	3MΩ

TABLE 10
Effectiveness of Test Methods for Detecting STFs in Type-C Designs

Transistor property	Transistor name	W+R	RES	Severe write	LVW-HVR (0.26v)
pull-up pMOS	M_{C4}(S/D)	11MΩ	17MΩ	6MΩ	930kΩ
	M_{C6}(S/D)				
pull-down nMOS	M_{C5}(S/D)	∞	∞	∞	16MΩ
	M_{C7}(S/D)				

resistance), even compared to other stability faults in Type-A and Type-B designs. This is because the write mechanism in Type-C design relies on M_{C4} (or M_{C6}) to strongly hold the value 1 at QB (or Q) at the end of a write-0 operation, while $VirGND$ just turns from VDD to GND. Thus, a small open defect on the source/drain of M_{C4} or M_{C6} may fail the write operation. In addition, the open defect at a transistor's gate is also relatively easier to detect when compared to that in Type-A and Type-B designs.

6.3 Effectiveness of Test Methods for Type-C Designs

Table 10 reports the minimum detectable resistance achieved by each test method for each stability fault in Type-C designs. As the result shows, only LVW-HVR can detect the stability faults on nMOS transistors M_{C5} and M_{C7} while both RES and severe write cannot. However, the write voltage for LVW-HVR need to be carefully assigned such that the nMOS stability faults can be detected and the fault-free design can still correctly function.

Table 11 shows the corresponding result of applying different write voltages to LVW-HVR. As the result shows, LVW-HVR cannot detect nMOS stability faults until the write voltage is reduced to 0.26 V. However, if we further lower the write voltage to 0.24 V, the minimum detectable resistance of pMOS and nMOS stability faults will be reduced to 2 and $45\ \mathrm{k}\Omega$. Such a low minimum detectable resistance kills almost all design margin for tolerating small detects during the test mode and in turn may result in an overtesting. Therefore, setting a proper write voltage is critical when applying LVW-HVR.

TABLE 11
Impact of Using Different Write Voltages during LVW-HVR for Type-C Designs

Transistor property	Transistor name	LVW-HVR with different write voltage (0.30v)	(0.28v)	(0.26v)	(0.24v)
pull-up pMOS	M_{C4}(S/D)	4MΩ	3MΩ	930kΩ	2kΩ
	M_{C6}(S/D)				
pull-down nMOS	M_{C5}(S/D)	∞	∞	16MΩ	45kΩ
	M_{C7}(S/D)				

TABLE 12
Impact of Using Different Backgrounds when Testing Fail-to-Read Open Defects in Type-C Designs

Transistor name	Same background	Opposite background
M_{C1}(G)	∞	310MΩ
M_{C1}(S/D)	78MΩ	7MΩ
M_{C3}(S/D)	∞	4MΩ

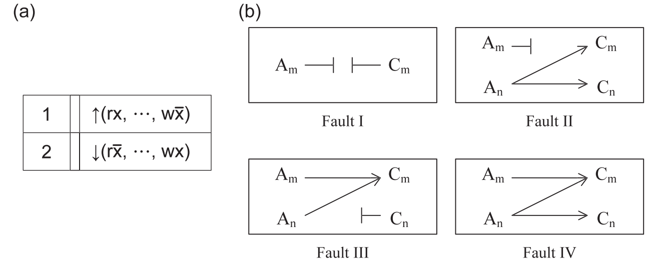

Fig. 9. (a) Conventional march sequence for detecting ADFs; (b) Types of address decoder faults.

Similar to Table 8, Table 12 reports the minimum detectable resistance obtained by applying the same background and the opposite background for all read-fail open defects in Type-C designs. The simulation is also conducted based on the FF corner at 75°C. As the result shows, the opposite data background can effectively help to detect those read-fail open defects (with an acceptable minimum detectable resistance) while the same data background may fail to detect a large open defect, which again shows the effectiveness of setting an opposite background for detecting a read-fail open defect.

7 Address Decoder Faults in Subthreshold SRAMs

Address decoder faults in memories have been studied in the past [22], [23], [24], and it is proven in [24] that all the gross ADFs (not including the faults with sequential behavior and the small timing defect in the address decoder) can be detected by a march algorithm as long as the two march elements in Fig. 9a are included. Fig. 9b shows the four gross ADFs defined in [24]. In Fig. 9b, A_m represents the word-line signal of the address m, and C_m represents the physical memory cell indexed by the address m. Also, both m and n represent addresses.

Note that the above march algorithm is derived based on the assumption that only one word-line is used for both read and write operations, which is the case of the

traditional 6T SRAM design. However, some subthreshold SRAM designs utilize multiple word-lines for read and write operations. Thus, the above march algorithm may not be able to detect all ADFs for all subthreshold SRAM designs. In the following sections, we will briefly discuss the impact of the ADFs for each type of the subthreshold SRAM designs. Also, only the single ADF model is considered.

7.1 Type-A Subthreshold SRAM

Type-A subthreshold SRAM designs use separate read word-line and write word-line (denoted as RWL and WWL in Figs. 2, 3, and 4) for read operations and write operations, respectively. Each ADF shown in Fig. 9 may occur on each of these two word-lines, and hence we need to consider total eight cases of ADFs (four types of ADFs on two word-lines). In the following paragraphs, the eight cases of ADFs would be discussed.

7.1.1 Fault-I

When Fault-I exists and occurs on the WWL, the cell C_m (refer Fig. 9b) would be unaccessible when it should be written, but accessible for reading. The sense amplifier, when reading C_m, would thus always output the same value as the prestored data in C_m. The SAF-like behavior can be easily tested by the march in Fig. 9a. In the other case of Fault-I occurring on the RWL, since the RWL of C_m will never be triggered, the voltage on RBL (refer Figs. 2, 3, and 4) when reading C_m will always keep high regardless of the value in C_m. The faulty behavior is just like SA1 and can also be tested by the Fig. 9a march.

7.1.2 Fault-II

When Fault-II occurs on the WWL, C_m could not be written by system operation "Write C_m" but by the "Write C_n." The faulty behavior can be tested by Fig. 9a march. It's because, in either $\Uparrow (rx, \ldots, w\bar{x})$ or $\Downarrow (r\bar{x}, \ldots, wx)$ where C_n is earlier accessed than C_m, the "Read C_m" will output the inverse value since the previous "Write C_n" operation changes the value stored in C_m. In the other case of occurring on the RWL, C_m is unaccessible for read operation and thus the SA output of operation "Read C_m" will always keep high as Fault-I on RWL. The SA1-like behavior is testable by the Fig. 9a march.

7.1.3 Fault-III

In the faulty behavior of Fault-III occurring on WWL, C_m would be written by operation "Write C_n" just like Fault-II on WWL. Thus, in either $\Uparrow (rx, \ldots, w\bar{x})$ or $\Downarrow (r\bar{x}, \ldots, wx)$ where C_n is earlier accessed than C_m, the SA output of "Read C_m" will be the inverse value written by operation "Write C_n." Fig. 9a march is still useful for Fault-III on WWL. For Fault-III on RWL, Fig. 9a is still useful but uses the different test element from on-WWL case. In the march element in which C_m is earlier accessed than C_n, the "Read C_n" will read the value in C_m, which is changed by previous operation "Write C_m," rather than unchanged value in C_n.

7.1.4 Fault-IV

Fault-IV on WWL is just like Fault-II/III on WWL which can be tested by the march element in which C_n is earlier accessed than C_m. The detail can be referred in previous paragraph. For Fault-IV occurring on RWL, its write operation works correctly but when reading cell n, both C_m and C_n will be read out at the same time. Assuming that $m > n$ in the ADF Fault-IV (i.e., $\Uparrow$ will visit n earlier than m), the march element $\Uparrow (rx, .., w\bar{x})$ cannot detect the ADF Fault-IV because both C_n and C_m store the same value x when reading C_n. Also, an address-decreasing march element $\Downarrow (rx, \ldots, w\bar{x})$ may not necessarily detect the ADF Fault-IV. For example, even though the march element $\Downarrow (r0, .., w1)$ can create the situation that C_n stores 0 and C_m stores 1 when reading C_n, the RBL remains the good value 0 because the read bit-line will not be pulled up by the value 1 of cell m for designs [10] and [11]. The read-1 mechanism in [10] and [11] is to turn off the pull-down path at the read bit-line and leave the read bit-line floating 1. Thus, only the march element $\Downarrow (r1, \ldots, w0)$ can detect the ADF Fault-IV in this case. Note that the above discussion is based on the assumption that $m > n$ in the ADF Fault-IV. To cover the case that that $m < n$, another march element $\Uparrow (r1, \ldots, w0)$ is also required.

7.1.5 Short Summary

After the analysis, most cases of ADFs can be detected by the march algorithm shown in Fig. 9a. However, the case of Fault-IV occurring on the RWL needs both $\Downarrow (r1, \ldots, w0)$ and $\Uparrow (r1, \ldots, w0)$. Therefore, a march algorithm which can cover four ADFs for Type-A SRAM designs needs to include three march elements. The two possible combinations of the three march elements are 1) $\Downarrow (r1, \ldots, w0)$, $\Uparrow (r1, \ldots, w0)$, and $\Downarrow (r0, \ldots, w1)$, and 2) $\Downarrow (r1, \ldots, w0)$, $\Uparrow (r1, \ldots, w0)$, and $\Uparrow (r0, \ldots, w1)$.

7.2 Type-B Subthreshold SRAM

Type-B subthreshold SRAM designs utilize WL and $\overline{WL}$ to access a bit-cell for both read and write operations. In general, these two signals (WL and $\overline{WL}$) come from the same address decoder but with the difference of an inverter. Thus, once an ADF falls in the address decoder, the signal at both WL and $\overline{WL}$ will be affected. As a result, the impact of an ADF fault in Type-B Subthreshold SRAM designs is exactly the same as that in a 6T SRAM design, and hence the march algorithm shown in Fig. 9a is sufficient to detect all the ADFs for Type-B Subthreshold SRAM designs.

7.3 Type C

The analysis of ADFs in Type-C subthreshold SRAM design [15] is more complicated than that in Type-A or Type-B designs since the Type-C design uses the combination of the values at $WL1$ and $WL2$ to determine the operation mode of a cell. Table 13 shows the value of $WL1$ and $WL2$ at its hold, read, and write mode, respectively.

TABLE 13
Setting of WL1 and WL2 for Type-C Design

operation	WL1	WL2
Hold	1	0
Read	0	1
Write	1	1

TABLE 14
Faulty Behavior of Address Decoder Faults on Type-C Designs (Fig. 8)

		Faulty-WL1						Faulty-WL2					
		C_m			C_n			C_m			C_n		
		WL1	WL2	Behavior	WL1	WL2	Behavior	WL1	WL2	Behavior	WL1	WL2	Behavior
Fault-I	Read C_m	1	1	FB1-USR	-	-	-	0	0	FB2-UA	-	-	-
	Write C_m	1	1	Write	-	-	-	1	0	FB2-UA	-	-	-
Fault-II	Read C_m	1	1	FB1-USR	1	0	Hold	0	0	FB2-UA	1	0	Hold
	Write C_m	1	1	Write	1	0	Hold	1	0	FB2-UA	1	0	Hold
	Read C_n	0	0	Hold	0	1	Read	1	1	FB3-AR	0	1	Read
	Write C_n	1	0	Hold	1	1	Write	1	1	FB4-AW	1	1	Write
Fault-III	Read C_m	0	1	Read	1	0	Hold	0	1	Read	1	0	Hold
	Write C_m	1	1	Write	1	0	Hold	1	1	Write	1	0	Hold
	Read C_n	0	0	Hold	1	1	FB1-USR	1	1	FB3-AR	0	0	FB2-UA
	Write C_n	1	0	Hold	1	1	Write	1	1	FB4-AW	1	0	FB2-UA
Fault-IV	Read C_m	0	1	Read	1	0	Hold	0	1	Read	1	0	Hold
	Write C_m	1	1	Write	1	0	Hold	1	1	Write	1	0	Hold
	Read C_n	0	0	Hold	0	1	Read	1	1	FB3-AR	0	1	Read
	Write C_n	1	0	Hold	1	1	Write	1	1	FB4-AW	1	1	Write

A full analysis of ADFs in the Type-C design should include the impact of each ADF on each word-line (total four ADFs for two word-lines). For each ADF on each word-line, we need to enumerate the value at each word-line caused by the ADF based on different operation modes of the two faulty cells, which includes four effective combinations: $C_m/C_n =$

1. Read/Hold,
2. Write/Hold,
3. Hold/Read, and
4. Hold/Write.

Note that we eliminate the cases of simultaneous Read and/or Write (i.e., Read/Read, Read/Write, Write/Read, and Write/Write) since the subthreshold SRAM is a single-port SRAM.

Table 14 lists the complete analysis results of $WL1$ and $WL2$ values of the Type-C design [15] under the four C_m/C_n operations when each of the ADFs in Fig. 9b occurs on $WL1$ and $WL2$ separately. According to the setting in Table 13, the values of $WL1$ and $WL2$ will lead to the corresponding behavior listed in the "Behavior" columns of Table 14. If the corresponding behavior is different from the supposed one, we highlight the faulty behavior with a gray background in Table 14. Note that we view the combination $WL1 = WL2 = 0$ as a Hold operation since this configuration also enables the Type-C design [15] to hold the data but just without the extra assistance of M_{C3} and M_{C9}.

The faulty behaviors in Table 14 are categorized into four groups (FB1-USR, FB2-UA, FB3-AR, and FB4-AW). In the paragraphs below, we will detail how each faulty behavior performs and give a short summary for testing ADFs in the Type-C design at the end.

7.3.1 FB1-USR (UnSafe Read)

The faulty behavior FB1-USR means that a cell is supposed to be read out, but its value may be attacked during the read operation. As shown in Table 13, only $WL2$ should be turned on during a read operation such that the turned off $WL1$ can protect the cross-coupled inverters from BL/BLB's direct accessing (as illustrated in Fig. 8). The cell with the faulty behavior FB1-USR would have both its word-lines turned on during a read operation, and thus the stored data (Q and QB) would be affected by the precharged BL/BLB just as the typical 6T SRAM would. In other words, the designed extra-read path in the Typc-C subthreshold SRAM is disabled and can no longer help the cell to avoid the potential read disturb. To detect the faulty behavior FB1-USR, we need to apply consecutive read operations to the same cells in the test sequence.

7.3.2 FB2-UA (UnAccessible)

The faulty behavior FB2-UA means that a cell is unaccessible by either a read or a write operation. This fault can already be detected by the conventional march sequence shown in Fig. 9a, and thus needs no further discussion.

7.3.3 FB3-AR (Attacked Read)

As shown as Table 14, the faulty behavior FB3-AR occurs when ADF II, III, or IV occurs on $WL2$, where C_m and C_n should originally be hold and read, respectively. However, both word-lines of C_m in this case are turned on instead. If C_m and C_n locate at different columns, C_m will be attacked by the unselected, precharged bit-lines just like the cell suffering FB1-USR, which can be detected by the consecutive read operations as discussed in Section 7.3.1. On the other hand, if C_m and C_n locate at the same column, the read operation on C_n will be affected by the value stored in C_m as well since both word-lines of C_m are turned on. To trigger this fault, we need C_m and C_n to store the inverse data when C_n is read. The march sequence shown in Fig. 9a satisfies this criterion. However, based on our simulation result, we found that the sensed output of this read fail with both BL and BLB pulled-down (one by C_m, and the other by C_n) is actually determined by the favored value of the sense amplifier in use. Thus, in order to cover different favored values of the sense amplifier, we should

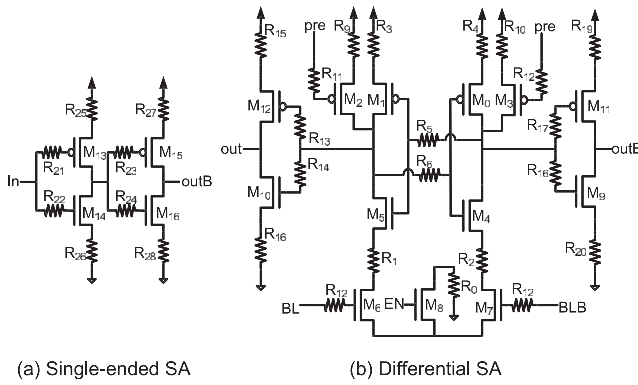

Fig. 10. Schematics of single-ended and differential sense amplifiers.

apply the march sequence shown in Fig. 9a twice, one with $x = 1$ and the other with $x = 0$. In other words, the march elements $\Downarrow (r1, \ldots, w0)$, $\Uparrow (r0, \ldots, w1)$, $\Uparrow (r1, \ldots, w0)$, and $\Downarrow (r0, \ldots, w1)$ should be included in the march algorithm.

7.3.4 FB4-AW (Attacked Write)

The faulty behavior FB4-AW is similar to FB3-AR, where C_m should originally be hold with $WL1/WL2 = 1/0$ but both its word-lines are unexpectedly turned on instead. The only difference is that a write operation (instead of a read operation) is applied to C_n for FB4-AW when both word-lines of C_m are unexpectedly turned on. If C_m and C_n are at the same column, our simulation result shows that the value stored in C_m will not be overwritten by the value writing into C_n since the VirGND of C_m still remain low (unlike a normal write operation keeping VirGND high). Also, the value of C_m will not prevent the original write operation to C_n from successfully performed even when their values are different. Thus, FB4-AW is more difficult to detect than FB3-AR. Fortunately, as shown in Table 14, an ADF causing FB4-AW must cause FB3-AR as well, meaning that FB4-AW can also be detected as long as FB3-AR can be detected through the methods described in Section 7.3.3. Therefore, we only need to focus on detecting FB3-AR when designing the test algorithm.

7.3.5 Short Summary

To detect the ADFs occurring on $WL1$, we need to use consecutive read operations to cover FB1-USR as shown in Section 7.3.1. As to the ADFs on $WL2$, Fault-I, Fault-II, and Fault-III all cause FB2-UA, such that conventional march sequence shown in Fig. 9a can already detect them. In the case that Fault-IV occurs on $WL2$, we can apply consecutive read operations and the march sequence $\{\Downarrow (r1, \ldots, w0); \Uparrow (r0, \ldots, w1); \Uparrow (r1, \ldots, w0); \Downarrow (r0, \ldots, w1)\}$ to detect FB3-AR.

7.4 Address-Decoder Faults with Sequential Behavior

Note that the march algorithm shown in Fig. 9a can detect all the ADFs for conventional 6T SRAM only under the assumption that no ADF has sequential behavior. If an ADF has sequential behavior, we need to apply the nonlinear test algorithm proposed by Sachdev [31], [32] to detect it in conventional 6T SRAM. However, the effect of ADFs with sequential behavior in subthreshold SRAMs still remains unclear, which could also be a potential research topic.

TABLE 15
Minimum Detectable Resistance for Open Defects on a Differential Sense Amplifier

Differential SA					
Open Defect	0.4 V	1.2 V	Open Defect	0.4 V	1.2 V
R0	280kΩ	10kΩ	R11	360MΩ	660kΩ
R1	890kΩ	10kΩ	R12	∞	130kΩ
R2	∞	10kΩ	R13	8.83MΩ	60kΩ
R3	∞	∞	R14	100MΩ	190kΩ
R4	∞	∞	R15	1.9MΩ	10kΩ
R5	30MΩ	0.1MΩ	R16	8.53GΩ	6.41GΩ
R6	∞	50kΩ	R17	∞	∞
R7	30MΩ	20kΩ	R18	∞	∞
R8	∞	30kΩ	R19	∞	∞
R9	290MΩ	390MΩ	R20	∞	∞
R10	300MΩ	90kΩ			

8 Fault Models for Sense Amplifier under Subthreshold Operations

8.1 Open Defects

In this section, we first attempt to observe the impact of a single open defect which falls on a single-ended or differential sense amplifier operating under the subthreshold operations, and then compare the results to that under the normal superthreshold operations. In the following experiment, we will inject a single open defect with different resistances to different terminals inside the sense amplifier and check whether the injected defect can cause a failure of a read-0 operation (denoted as R0) or a read-1 operation (denoted as R1). However, the result of this experiment may depend on the setting of the cycle time. In order to make fair comparison of sense amplifiers between the subthreshold operations and the superthreshold operations, we operate the same bit-cell design at both 0.4 and 1.2 V, and then set the cycle time by adding extra 20 percent to the minimum required cycle for both designs under subthreshold and superthreshold operations.

Figs. 10a and 10b illustrate the schematic of the single-ended and differential sense amplifiers used in our experiment. Also, we label the terminals where an open defect may be injected in Fig. 10. Table 15 first reports the minimum detectable resistance of each possible open defect based on the operating voltage of both 0.4 and 1.2 V, respectively, for the differential sense amplifier. As the result shows, the minimum detectable resistance of almost all open defects under 0.4 V operations is at least one order higher than that under 1.2 V operations. A similar result can also be observed from the single-ended sense amplifier, whose result is reported in Table 16. Therefore, we can conclude that the sense amplifiers under subthreshold operations is more immune to the open defects than that under superthreshold operations.

8.2 V_{th} Mismatch

The sensing ability of a sense amplifier can be significantly affected by the mismatch of device's V_{th} [25], [26], especially when the local process variation has continually increased in advanced process technologies [5], [6]. V_{th} mismatch may

TABLE 16
Minimum Detectable Resistance for Open Defects on a Single-Ended Sense Amplifier

Single-ended SA					
Open Defect	0.4 V	1.2 V	Open Defect	0.4 V	1.2 V
R21	50MΩ	1.1MΩ	R25	60MΩ	105kΩ
R22	520MΩ	1.8MΩ	R26	60MΩ	1.6MΩ
R23	360MΩ	∞	R27	110MΩ	10.8MΩ
R24	100MΩ	2MΩ	R28	22MΩ	500kΩ

result in a larger input offset voltage for a differential sense amplifier. Also, V_{th} mismatch may result in a higher input voltage to read 1 (or a lower input voltage to read 0) for a single-ended sense amplifier. In the following experiment, we attempt to observe the impact of different levels of V_{th} mismatch on differential and single-ended sense amplifiers operating at 1.2 and 0.4 V, respectively.

We first model the V_{th} of each device in an independent normal distribution and specify a 3-sigma value to the normal distributions to represent the level of V_{th} mismatch. Based on the specified V_{th} distributions for all devices, we then randomly sample 10,000 device configurations for a sense amplifier and collect the 99th percentile of its largest input voltage offset among the 10,000 configurations. Fig. 11 plots the 99 percent percentile of its largest input offset voltage versus the 3-sigma value of V_{th} distributions for the differential sense amplifier operating at both 0.4 and 1.2 V, respectively. Note that the 3-sigma value of V_{th} distributions in Fig. 11 is represented by its percentage to the mean value of V_{th}, i.e., 0.4 V in this technology. For example, a 10 percent 3-sigma value shown in Fig. 11 means 10 percent of 0.4 V, i.e., 40 mV.

For the result of 0.4 V operations in Fig. 11, the input offset voltage of the differential sense amplifier dramatically increases and exceeds its operating voltage 0.4 V when the 3-sigma value of V_{th} distributions is larger than 9 percent. On the other hand, the input offset voltage under 1.2 V operations increases more slowly based on the same level of V_{th} mismatch. This result shows that a differential sense amplifier under subthreshold operations is more vulnerable against V_{th} mismatch than that under superthreshold operations. In other words, the probability to have a faulty differential sense amplifier is higher in subthreshold SRAMs, compared to the traditional SRAMs under superthreshold operations.

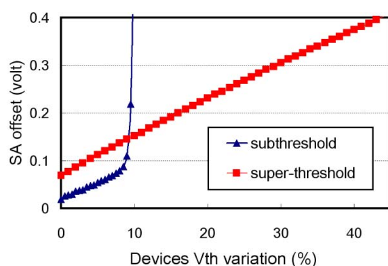

Fig. 11. 99th percentile of the largest input voltage offset versus V_{th} mismatch for a differential SA operating at 0.4 and 1.2 V, respectively.

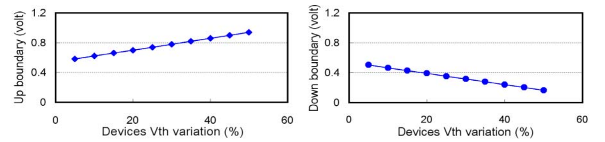

Fig. 12. 99th percentile of the largest (smallest) input voltage for read 1 (0) for a single-ended SA operating at 1.2 V.

Fig. 12a plots the 99th percentile of the largest input voltage to successfully read 1 from a single-ended sense amplifier under 1.2 V operations. Fig. 12b plots the 99th percentile of the smallest input voltage to successfully read 0 from a single-ended sense amplifier under 1.2 V operations. Fig. 13 plots the same result under 0.4 V operations. By comparing Figs. 12 and 13, we can find that the change in the largest input voltage for read 1 (or the smallest input voltage for read 0) under 1.2 V operations is similar to that under 0.4 V operations based on the same level of V_{th} mismatch, if we scale the result of 0.4 to 1.2 V. Also, under 0.4 V operations, the input-offset change of a single-ended sense amplifier increases more slowly than that of a differential sense amplifier when V_{th} mismatch increases. This result shows that a single-ended sense amplifier may tolerate a more significant process variation than a differential sense amplifier.

9 Impact of Temperature at Test

When operating at a superthreshold voltage (e.g., 1.2 V), the on-current of a transistor decreases along with the increase of temperature [27], meaning that the performance of a circuit also decreases. At the same time, the power consumption of a circuit increases along with the increase of temperature as well due to the lower V_{th} at a higher temperature [27], [28]. Therefore, we in general test a circuit (including logic and memory) more often at a high temperature than that at a low temperature since operating a circuit at a high temperature can exercise a worse corner of both the circuit's performance and power consumption, which in turn can examine the circuit's marginality and reliability. In addition, such a stressed condition at a high temperature can further speed up the aging of circuits and identify the infant mortality of circuits (such as burn-in).

However, the above property may not hold for subthreshold SRAMs (or general subthreshold logic circuits). Fig. 14a first plots the minimum required cycle time for a subthreshold SRAM array [9] (used in our previous experiment) at different temperatures. As the figure shows, the cycle time decreases when the temperature increases under 0.4 V operations, which is opposite to the case under 1.2 V operations. On the other hand, Fig. 14b plots the power consumption of the same subthreshold SRAM array at different temperatures and shows that the power

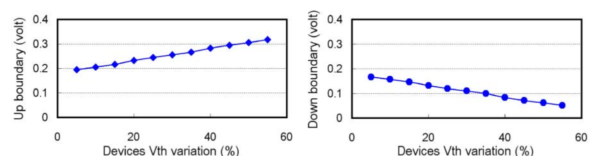

Fig. 13. 99th percentile of the largest (smallest) input voltage for read 1 (0) for a single-ended SA operating at 0.4 V.

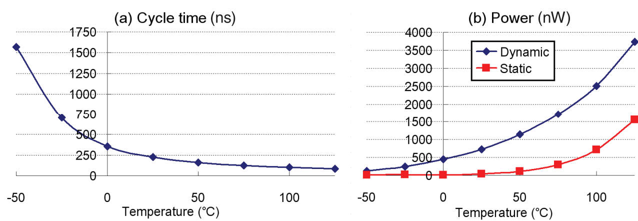

Fig. 14. (a) Cycle time versus temperature and (b) Power consumption versus temperature for a 128×32 subthreshold SRAM array.

consumption of a subthreshold SRAM array still increases when the temperature increases. The same trend about circuit performance and power consumption also holds for the subthreshold logic circuits [29], [30].

As a result, testing a subthreshold SRAM at a high temperature can exercise a worse corner only for its power consumption. To exercise a worse corner for its performance, testing the subthreshold SRAM at a low temperature is required. This result also implies that the effectiveness of the traditional burn-in test may need to be reevaluated for subthreshold circuits.

10 Conclusion

In this paper, we first validated the effectiveness of three different test methods on detecting stability faults through simulation and found that 1) only severe write can cover all stability faults for Type-A designs, 2) only read equivalent stress can cover all stability faults for Type-B designs, and 3) only low-V-write/high-V-read can cover all stability faults for Type-C designs. We also discussed the effectiveness of using opposite background for detecting a fail-to-read open defect for each type of designs and found that this background works for Type-B and Type-C designs. Next, we discussed the faulty behavior of address decoder faults for each type of designs and found that 1) the detection of ADFs in Type-A designs requires a different march sequence from the traditional one and 2) the detection of ADFs in Type-C designs requires consecutive read operations and a specialized march sequence. Next, we studied the impact of open defects and V_{th} mismatch on sense amplifiers and found that 1) sense amplifiers under 0.4 V operations are more immune to open defect and 2) differential sense amplifiers under 0.4 V operations are more vulnerable to V_{th} mismatch, when compared that under 1.2 V operations. At last, we discuss the impact of the test temperature under 0.4 V operations and how it differs from that under 1.2 V operations.

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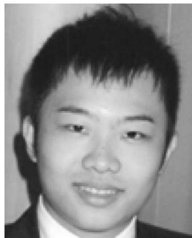

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