Wide Tunning Range 60 GHz VCO and 40 GHz DCO Using Single Variable Inductor

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Abstract—This paper presents a 60 GHz, 16% tuning range VCO, and a 40 GHz, 18 bits, 14% tuning range DCO incorporating variable inductor (VID) techniques. The variable inductor, consisting of a transformer and a variable resistor, is tunable by adjusting its resistor. By employing the proposed frequency tuning scheme, wide-tuning range as well as multi-band operation are achieved without sacrificing their operating frequencies. To verify the operation principles, the VCO and DCO are both fabricated in 90 nm CMOS technology. The tuning range of VCO is from 52.2 GHz to 61.3 GHz. The measured phase noise from a 61.3-GHz carrier is about -118.75 dBc/Hz at 10-MHz offset, and the output power is -6.6 dBm. It dissipates 8.7 mW from a 0.7-V supply, and the chip size is $0.28 \times 0.36 \text{ mm}^2$. On the other hand, the DCO is capable of covering frequency range from 37.6 GHz to 43.4 GHz. The measured phase noise from a 43 GHz carrier is about -109dBc/Hz at 10-MHz offset, and the output power is -11 dBm. The DCO core dissipates 19 mW from a 1.2-V supply. Chip size is $0.5 \times 0.15 \text{ mm}^2$.

Index Terms—Digital controlled oscillator (DCO), millimeterwave (MMW) band, ultra wide band (UWB), variable inductor (VID), voltage controlled oscillator (VCO).

I. INTRODUCTION

HORT RANGE multi-Gbps wireless interconnects have motivated marvelous research efforts recently [1]–[11]. At 60-GHz unlicensed frequency band, a 7-GHz wide spectrum is available for up to 6-Gbps UWB applications. With the rapid developments of the VLSI process, nano-meter CMOS are considered as promising technologies to make RFICs for the broadband wireless interconnects feasible and cost effective.

In the RF transceiver front-end, LC voltage-controlled oscillators (VCOs) are extensively used in frequency synthesizers to provide local carriers for up and down frequency conversion. Thus its performance is essential to the wireless transceiver. Major design issues of the VCO are focused on oscillating frequency, phase noise, output power level, and frequency tuning range. For portable devices, its power dissipation is also of special concern.

Conventionally, millimeter-wave (MMW) band LC-VCOs employ accumulation-mode MOS (A-MOS) varactors for

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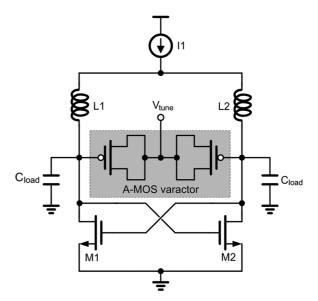


Fig. 1. The schematic of LC-VCO.

frequency tuning [12]–[17]. Fig. 1 shows a typical schematic of LC-VCO. The VCO oscillation frequency can be approximated as

$$f_{vco} = \frac{1}{2\pi\sqrt{L(C_{\text{var}} + C_p)}}\tag{1}$$

where L, C_{var} , and C_p respectively represent the inductance, varactor capacitance, and loading capacitance at the resonator. Here the loading capacitance also includes the parasitic capacitance contributed by the succeeding buffer stage. In order to achieve 60-GHz operating frequency, the varactor capacitance (C_{var}) and the corresponding tuning range are severely limited due to C_p . This issue becomes even more critical under low supply voltage, which is required for nanometer CMOS operation.

It is well known that the phase noise performance of a VCO degrades when the VCO gain, K_{VCO} , increases [19]. However, for a single band VCO, K_{VCO} is proportional to its oscillating frequency for the same frequency tuning percentage. Considering an oscillator with 10% frequency tuning range and 1-V tuning voltage, its K_{VCO} is 180 MHz/V at oscillating frequency of 1.8 GHz, but increases to 6 GHz/V if its output frequency is raised to 60 GHz. Therefore, for broadband MMW applications, multi-band VCO is necessary to degenerate VCO gain K_{VCO} and alleviate phase noise performance degradation. However, conventional capacitor bank for multi-band operation is hardly applicable in the 60-GHz case since the C_p in the capacitor bank is too large to be tolerable. Some magnetic tuning methods have been reported [20]–[25] to increase the frequency tuning ranges

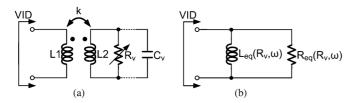


Fig. 2. (a) The proposed variable inductor. (b) Equivalent circuit model.

of LC-tank VCOs though, their oscillation frequencies are far less than 60 GHz.

In this paper, a 60-GHz varactor-less VCO and an 18 bit, 40 GHz DCO for multi-band operations employing a novel variable inductor (VID) are proposed [26]. Based on magnetic tuning scheme, they achieve multi-band as well as broad-band operations without sacrificing their oscillation frequencies. Measurement results show that the VCO's output frequency ranges from 52.2 GHz to 61.3 GHz. The corresponding tuning percentage is 16.07%. It manifests strong potential to be applied in the 60-GHz band UWB system. Also, the VCO is capable of operating under a supply voltage as low as 0.7 V, which is suitable for nano-meter CMOS technology. On the other hand, the measured output frequency of the 40 GHz DCO is distributed from 37.6 GHz to 43.4 GHz, corresponding to 14% tuning range. It can be applied in a dual-IF receiver for 60 GHz UWB system [27]–[29].

This paper is organized as follows. In Section II, the proposed VID and its tuning schemes are described. Section III presents the VCO and DCO design. The experimental results of the two oscillators are shown in Section IV. Finally, conclusion is drawn in Section V.

II. PRINCIPLE OF THE VARIABLE INDUCTOR (VID)

A. VID Schematic and Equivalent Circuit Model

Fig. 2(a) illustrates the schematic of the proposed VID, which consists of a transformer T_1 and a variable resistor R_v . L_1 and L_2 respectively represent the self inductance of the primary and secondary coils of T_1 , k is the coupling factor of the primary and secondary coils, and C_v is the parasitic capacitor at the secondary coil. The VID can be modeled as a variable inductor L_{eq} in parallel with a variable resistor R_{eq} ,, as is illustrated in Fig. 2(b). Both L_{eq} and R_{eq} are functions of R_v and the radian frequency ω . It can be derived that

$$L_{eq}(R_v, \omega) = \frac{R_v^2 L_1 \left[1 - \omega^2 C_v L_2 (1 - k^2)\right]^2 + \omega^2 L_1 L_2^2 (1 - k^2)^2}{R_v^2 (1 - \omega^2 C_v L_2) \left[1 - \omega^2 C_v L_2 (1 - k^2)\right] + \omega^2 L_2^2 (1 - k^2)}$$
(2)

and

$$R_{eq}(R_v, \omega) = \frac{R_v^2 L_1 \left[1 - \omega^2 C_v L_2 (1 - k^2) \right]^2 + \omega^2 L_1 L_2^2 (1 - k^2)^2}{R_v k^2 L_2}$$
(3)

If the self resonant frequencies of C_v and L_2 are larger than the operating frequency ω , i.e., $\omega^2 C_v L_2 < 1$, L_{eq} increases with

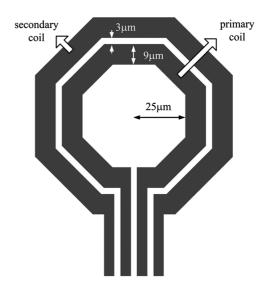


Fig. 3. 1:1 Transformer layout view.

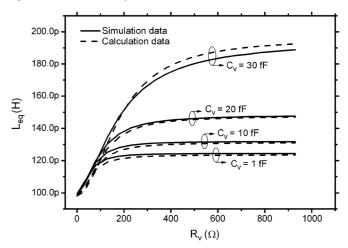


Fig. 4. Simulated and calculated L_{eq} at 60 GHz.

the increment in R_v . Thus, the minimum equivalent inductance L_{min} is equal to $L_{eq}(0,\omega)$, and can be calculated as

$$L_{eq}(0,\omega) = L_1(1-k^2). \tag{4}$$

Contrarily, the maximum equivalent inductance L_{max} is equal to $L_{eq}(\infty, \omega)$, and can be calculated as

$$L_{eq}(\infty,\omega) = L_1 \left(1 + \frac{\omega^2 L_2 C_v}{1 - \omega^2 L_2 C_v} k^2 \right). \tag{5}$$

From (4) and (5), it can be seen that only L_{max} depends on the parasitic capacitance C_v , and its lower bound is L_1 (i.e., $L_{max} > L_1$). Under this circumstance, the lower bound of the inductance tuning ratio α can be derived as

$$\alpha \equiv \frac{[L_{eq}(\infty,\omega) - L_{eq}(0,\omega)]}{L_{eq}(\infty,\omega)} = \frac{k^2}{1 - \omega^2 C_v L_2(1 - k^2)} > k^2$$
(6)

On the other hand, if $\omega^2 C_v L_2 > 1$, L_{eq} may become non-monotonic against R_v , and even become negative if R_v is too large. When the VCO's tuning characteristic is not monotonic, it will result in false locking of a PLL.

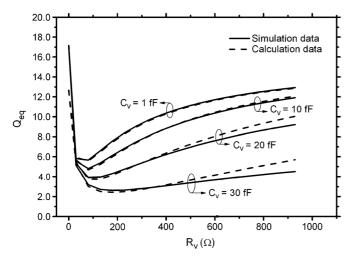


Fig. 5. Simulated and calculated Q_{eq} at 60 GHz.

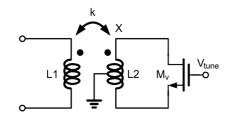


Fig. 6. VID implementation.

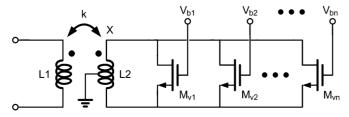


Fig. 7. Multi-band variable inductor.

Fig. 3 shows the layout of the transformer used in the simulations. The inner radius of the primary (secondary) coil is 25 μm (37 μm); the metal width is 9 μm ; and the space between the first and second coils is 3 μm . By EM simulation, the self-resonant frequency of the transformer is about 194 GHz. The self inductance of the primary (secondary) coil is about 123 pH (175 pH), and the coupling factor is about 0.45 at 60 GHz.

Fig. 4 shows the EM simulation results of L_{eq} against R_v under different C_v at 60 GHz. The L_{eq} derived in (2) is also shown for comparison. It can be seen that L_{eq} increases along with the increment in R_v . And the inductance tuning ratio α is larger than or equal to k^2 (i.e., 0.2) in all cases. Also, only L_{max} depends on C_v as predicted by (5). The proposed lumped circuit model in Fig. 2(a) can accurately represent VID's inductance. In Fig. 4, it can also be seen that L_{eq} is proportional to R_v when

 R_v is less than 100 Ω . The linear range of R_v can be derived from (2) and approximated as R_{lin} , where

$$R_{lin}^2 = \omega^2 L_2^2 (1 - k^2) [6k^2 - 1]$$
 when $\omega^2 C_v L_2 < 1$ (7)

Under this circumstance, the tunable inductor within the linear region can be described as

$$L_{eq-lin}(R_v, \omega) = L_1 \left[\frac{\sqrt{(6k^2 - 1)}}{6\sqrt{\omega^2 L_2^2 (1 - k^2)}} R_v + (1 - k^2) \right],$$
(8)

which is also independent of C_v at the secondary coil.

The other important parameter of the proposed VID is its quality factor Q_{eq} . By taking the parasitic resistors into account, the Q_{eq} can be calculated as shown in the equation at the bottom of the page, where R_1 is the equivalent parasitic resistor of the primary coil. The detail derivation of (9) is shown in Appendix. When $\omega^2 C_v L_2 < 1$ and at around 60 GHz, the EM simulated and calculated Q_{eq} under different C_v are plotted against R_v , as is shown in Fig. 5. The frequency response of the quality factor has a V shape, which reveals that the VID has a better quality factor in the extreme cases where R_v is nearly short or open circuit. In either case the magnetic energy dissipated in the passive R_v can be minimized.

When the VID is integrated in an LC oscillator, its oscillation frequency can be approximated as

$$\omega_{osc}(\Delta L) \approx \omega_{center} \left(1 - \frac{1}{2} \frac{\Delta L}{L_{center}} \right) \text{ when } \frac{\Delta L}{L_{center}} \ll 1$$
(10)

where ω_{center} is the center frequency of the VCO, L_{center} is the inductance at ω_{center} , and ΔL is the inductance tuning range. According to (10), the frequency tuning characteristic of an LC-VCO can be linearized by a linear control of VID.

B. VID Tuning by MOSFET Resistors (VID-I)

The proposed VID can be modified to achieve multi-band operation. Here M_v in Fig. 6 is decomposed into several smaller devices $M_{v1} \dots M_{vn}$ in parallel, as is shown in Fig. 7. Each smaller device is separately controlled by voltages $V_{b1} \dots V_{bn}$. As the device size of M_v is equal to those of $M_{v1} \dots M_{vn}$ in total, the parasitic capacitance at node X in Fig. 7 is almost the same as that in Fig. 6. Thus, multi-band operation can be achieved without severely affecting the inductance and the tuning percentage of the VID. This is a major advantage in contrast to conventional capacitor-bank structure, where the parasitic capacitor in general contributes significantly to the total capacitance at the oscillating node, and thus limits the tuning range. Also, the variable resistors occupy smaller silicon area compared to varactors or metal-insulator-metal capacitors, thus a small form factor can be benefited.

$$Q_{eq} = \omega \cdot \frac{R_v^2 L_1 (1 - \omega^2 C_v L_2)^2 + \omega^2 L_1 L_2^2 (1 - k^2) + \omega^2 k^2 R_v^2 C_v L_1 L_2 (1 - \omega^2 L_2 C_v)}{R_1 R_v^2 (1 - \omega^2 C_v L_2)^2 + \omega^2 L_2 (k^2 L_1 R_v - R_1 L_2)}$$
(9)

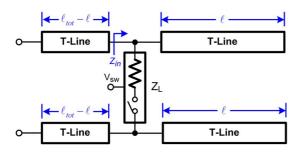


Fig. 8. A reconfigurable transmission line.

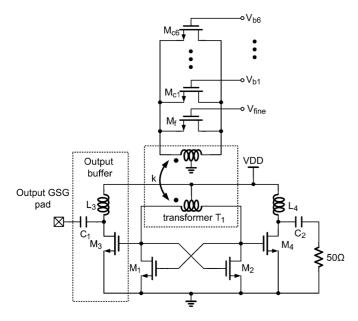


Fig. 9. VCO schematic.

C. VID Tuning by Reconfigurable Transmission Line (VID-II)

As is revealed in Fig. 4 and (8), a linear tuning of L_{eq} depends on a linear control of R_v . For high resolution frequency tuning, it is difficult to be realized using parallel MOSFETs resistors. Although it can be achieved by adopting predistortion DAC to provide adequate dc bias for the switchable MOSFETs, a sophisticated design may be required. Another potential solution is to reconfigure the switchable MOSFETs resistors in a series way, but large devices are required as is imposed by R_{lin} . It turns out that the self resonant frequency of the VID is severaly limited. In order to develop a linear tuning scheme for VID to facilitate all digital PLL application, a VID tuning by reconfigurable transmission line is proposed.

Fig. 8 illustrates the schematic of tunable resistor, which is composed of a switch controlled by V_{sw} in parallel with an open stub transmission line ℓ . Assuming that the turn on resistance of the switch is Z_L , it can be shown that the input impedance (Z_{in}) looking into the open stub can be derived as

$$Z_{in}(\ell) = Z_L \| \left[\frac{Z_0}{j \tan(\beta \ell)} \right] \approx Z_0 \frac{1}{Z_0/Z_L + j \tan(\beta \ell)} \quad (11)$$

where Z_o and β respectively represent the characteristic impedance and phase velocity of the transmission line. If

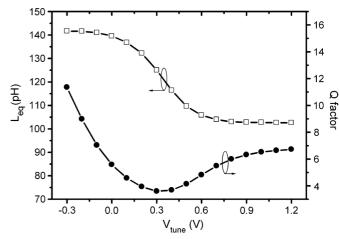


Fig. 10. The simulated L_{eq} and Q_{eq} of VID-I based on EM simulation.

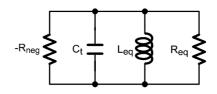


Fig. 11. VCO small-signal model.

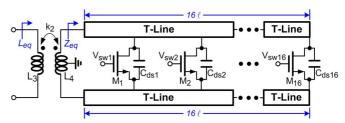


Fig. 12. The 4 bits linear VID.

 $Z_0 \approx Z_L$, the real part of Z_{in} can be approximated as

$$\operatorname{Re} \left[Z_{in}(\ell) \right] \approx Z_0 \frac{1}{1 + \tan^2(\beta \ell)}$$

$$= 0.5 Z_0 \left[1 + \sin(\pi/2 - 2\beta \ell) \right]$$

$$\approx 0.5 Z_0 (1 + \pi/2 - 2\beta \ell), \tag{12}$$

which is proportional to ℓ . Thus the real part of $Z_{\rm in}$ is tunable by positioning the switches to reconfigure the effective length of transmission line.

III. CIRCUIT DESIGN

To verify the operation principle of the proposed VIDs, two experimental prototypes are implemented and demonstrated. In Section III-A, a 60 GHz VCO using a VID with MOSFET variable resistors is described. It features broadband as well as multi-band operations, and can be integrated in a PLL to degenerate VCO gain for lower phase noise performance. On the other hand, a 40 GHz DCO using a VID with reconfigurable transmission line is introduced in Section III-B. It shows higher resolution in frequency tuning and also facilitates integration in an all digital phase locked loop (ADPLL).

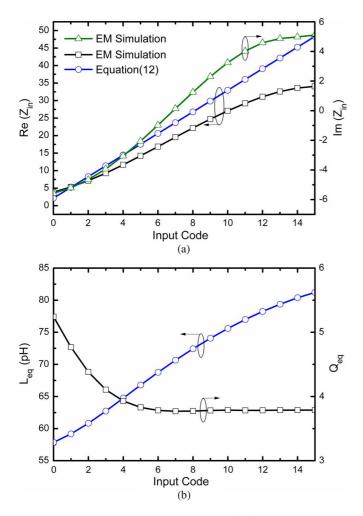


Fig. 13. (a) The EM simulated and calculated $Re(Z_{\rm eq})$. (b) Equivalent inductance and quality factor of 4-bits VID-II based on EM simulation.

A. 60 GHz Multi-Band VCO

The detail schematic for 60 GHz, multi-band VCO is show in Fig. 9. In order to reduce the parasitic capacitance at the resonator, the negative impedance converter is composed of M_1 and M_2 cross-coupled pair. M_3 is an output buffer to drive the 50- Ω load for measurement, and M_4 is a dummy buffer to balance the parasitic capacitance at the resonator.

The variable resistors consists of six binary-weighted NMOSFETs $(M_{c1}-M_{c6})$ controlled by digital codes $(V_{b1}-V_{b6})$ for band switching, and an NMOS M_f controlled by V_{fine} for fine frequency tuning. Thus R_v and L_{eq} are tunable by adjusting V_{fine} or $[V_{b1},\ldots,V_{b6}]$. The second coil is center tapped to ground, so as to diminish dc power dissipation. For a better quality factor, the self resonant frequency at the secondary port caused by L_2 and the parasitic capacitance of MOSFETs should be designed to be higher than the operating frequency of the VID.

In the experimental prototype, a single-turn 1:1 transformer is adopted in the VID, as is shown in Fig. 3. To illustrate L_{eq} and Q_{eq} across different band of operations, $(V_{b1}-V_{b6})$ and V_{fine} are wired together and controlled by V_{tune} . The simulated L_{eq} and Q_{eq} of VID (VID-I) at 60-GHz are illustrated in Fig. 10. When V_{tune} changes from -0.3 to 1.2 V, the L_{eq} is tunable

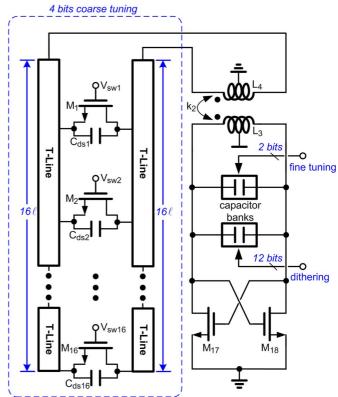


Fig. 14. The schematic of DCO.

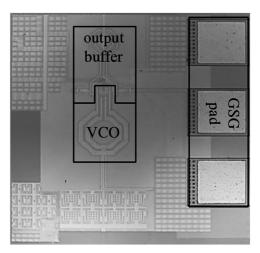


Fig. 15. VCO chip micrograph.

from 142 to 103 pH (i.e., $\alpha = 27.5\%$), and the quality factor is changed from 11.35 to 3.6. The VID has a better quality factor when MOSFET resistors are nearly fully turned on or off, i.e., R_v is minimum or maximum. This agrees pretty well with the calculated results shown in (9) and Fig. 5.

The equivalent small-signal model of the VCO is shown in Fig. 11. Here C_t represents the total capacitance at the resonator, including the parasitic capacitances of the cross-coupled pair M_1/M_2 , the output buffer M_3/M_4 , and the parasitic capacitance of the transformer T_1 . R_{eq} is the equivalent resistance looking into the primary coil of the VID, as is derived in (3). The negative resistance provided by the cross-coupled pair M1 and M2 is denoted as $-R_{neg}$, which is approximately equal to $-2/g_m$, and g_m is the small-signal transconductance

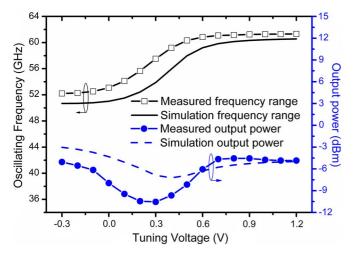


Fig. 16. Measured/simulated frequency tuning characteristic and output power of 60 GHz VCO.

of M_1/M_2 . R_{neg} must be smaller than R_{eq} to guarantee oscillation start-up. In this design, R_{neg} is chosen to be smaller than $R_{eq}/2.5$ within the entire frequency range. The oscillating frequency ω of the VCO can be derived as

$$\omega = \frac{1}{\sqrt{C_t L_{eq}(R_v, \omega)}}$$

$$= \sqrt{\frac{R_v^2 (1 - \omega^2 C_v L_2) \left[1 - \omega^2 C_v L_2 (1 - k^2)\right] + \omega^2 L_2^2 (1 - k^2)}{C_t R_v^2 L_1 \left[1 - \omega^2 C_v L_2 (1 - k^2)\right]^2 + \omega^2 C_t L_1 L_2^2 (1 - k^2)^2}}$$
(13)

, and the upper (ω_{max}) and lower (ω_{min}) bound of output frequencies are

$$\omega_{\text{max}} = \frac{1}{\sqrt{C_t L_{eq}(0, \omega_{\text{max}})}} = \frac{1}{\sqrt{C_t L_1 (1 - k^2)}}$$
(14)

and

$$\omega_{\min} = \frac{1}{\sqrt{C_t L_{eq}(\infty, \omega_{\min})}} < \frac{1}{\sqrt{C_t L_1}}$$
 (15)

Based on (14) and (15), the VCO frequency tuning percentage can be derived and is approximated by $k^2/2$, which is determined by the coupling factor (k) of the transformer. Therefore, for a VCO with a given transformer to implement the VID, its frequency tuning range can be quickly estimated. In this design, the coupling factor of the transformer is around 0.45, it turns out that the frequency tuning range of the VCO is at least 10%.

B. A 40 GHz DCO With Linear Frequency Tuning

To further linearize the frequency tuning characteristic of VID, a 40 GHz DCO with reconfigurable transmission line is implemented. Fig. 12 shows the detail schematic of a 4-bits linearly controlled VID (VID-II) for coarse tuning. The transmission line is divided equally into 16 segments with 16 MOS switches attched on it. Thus the effective length of the open stub is programable by the switches, and the parasitic capacitance associated with the MOS switches can be absorbed along the transmission line. Based on (7) and (8), the frequency tuning

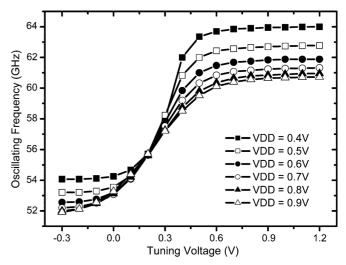


Fig. 17. Measured VCO tuning characteristics under different supply voltages.

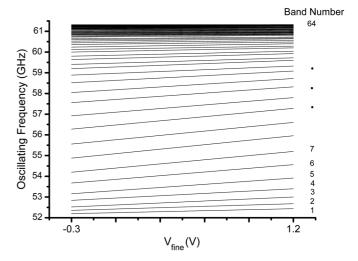


Fig. 18. Measured frequency tuning characteristics of all bands of the $60~\mathrm{GHz}$ VCO.

range (β_{DCO}) of the DCO with linear frequency tuning can be derived as

$$\beta_{DCO} > \frac{2(1 - 1.1\sqrt{1 - k^2})}{1 + 1.1\sqrt{1 - k^2}} \tag{16}$$

The physical length of the transmission line is 15 $\mu m/\ell$. By EM simulation, L_3 , L_4 and k_2 of the transformer are 100 pH, 129 pH and 0.6, while Z_L (Z_0) and β are 46 Ω and 0.08 rad/ ℓ respectively. It turns out that the corresponing frequency tuning range is at least 13% according to (16).

Fig. 13(a) shows the EM simulated $Z_{\rm eq}$ and that derived by (12). Both illustrate linear characteristic along the tuning range. Fig. 13(b) shows the equivalent inductance and quality factor of the linearly controlled VID by EM simulation. The corresponding inductance is distributed from 58 pH to 82 pH, while Q is varied between 5.5 to 3.8 due to the change of real part of $Z_{\rm eq}$.

Fig. 14 shows the detail schematic of the 40 GHz digitally controlled oscillator (DCO). The DCO has 4 bits for coarse tuning with VID-II, 2 bits for fine tuning with varactors, and 12 bits dithering though varactor controlled by a 2nd order $\Delta\Sigma$

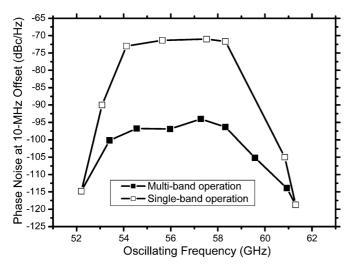


Fig. 19. Measured phase noise at 10-MHz offset in single-band and multi-band operation of the 60 GHz VCO.

modulator at 400 MHz. The corresponding minimum gain of the DCO is about 24 kHz/step.

IV. MEASUREMENT RESULTS

A. 60 GHz Single and Multi-Band VCO

Fig. 15 shows the chip micrograph of the 60 GHz VCO. The core size is $0.28 \times 0.36 \text{ mm}^2$. The chip is measured on a high-frequency probe station. With VDD = 0.7 V, the measured and simulated frequency tuning characteristics are shown in Fig. 16. If the tuning voltages of $V_{b1} - V_{b6}$ and V_{fine} in Fig. 9 are tied together and varied from -0.3 to 1.2 V, the single band VCO frequency is changed from 52.2 to 61.32 GHz. The corresponding tuning percentage is 16.07%. With a reduced tuning range of 0 V to 0.7 V, the tuning percentage becomes 13.98%. After the loss from the output buffer, probes, cables, adapters, and external mixer is deembedded, the measured single-ended output power are also shown in Fig. 16. Here the simulation results are also shown for comparison. From the measurement results, the VCO output power varies from -10 dBm to -4 dBm within the entire frequency tuning range.

The VCO can start oscillation as VDD is larger than $0.37~\rm V$. The measured frequency tuning ranges for VDD from $0.4~\rm V$ to $0.9~\rm V$ are shown in Fig. 17. When VDD = $0.4~\rm V$, the VCO has the maximum frequency tuning range from $54.07~\rm to~64~\rm GHz$ (i.e., 16.8% at $59~\rm GHz$). Under this circumstance, the parasitic capacitance introduced by negative impedance converter is minimized.

Multi-band operation is achieved by digitally controlling V_{b1} – V_{b6} and fine-tuning V_{fine} separately. By the mixed-mode frequency tuning scheme, the VCO manifests 64 frequency bands incorporating binary weighted transistors $\rm M_{c1}$ – $\rm M_{c6}$, as is shown in Fig. 18. The maximum K_{VCO} is 720 MHz/V at band 8, which is reduced by 10 fold compared to that of a single-band operation. The uniformity of multi-band operations can be improved by more sophisticated transistor sizing instead of employing binary-weighted transistors.

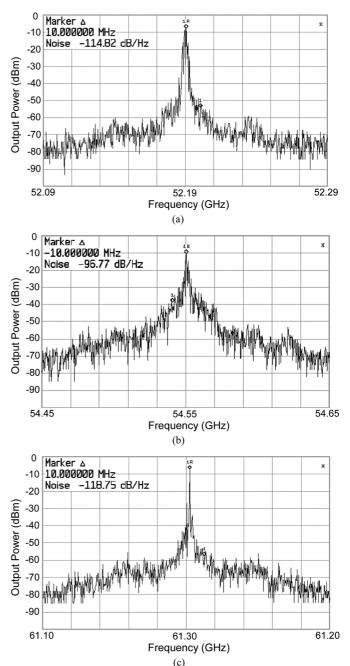


Fig. 20. Measured output spectrums of the 60 GHz VCO at (a) 52.19 GHz (b) 54.55 GHz (c) 61.3 GHz.

The measured phase noise performance at 10-MHz offset within the entire frequency tuning range is plotted in Fig. 19. By multi-band operation, the phase noise performance ranges from -94 to -118.75 dBc/Hz, and the average phase noise is -102.44 dBc/Hz. If V_{b1} – V_{b6} and V_{fine} are tied together for a single-band frequency tuning, the measured phase noise is also shown for comparison. It can be observed that phase noise performance can be significantly improved by 10 to 30 dB employing the proposed multi-band operation scheme.

Fig. 20(a)–(c) show the measured VCO output spectrums at different frequencies. When VDD = 0.7 V, the measured average power consumptions of the VCO core within the frequency tuning range is 8.7 mW. The buffer stage dissipates 5.6 mW.

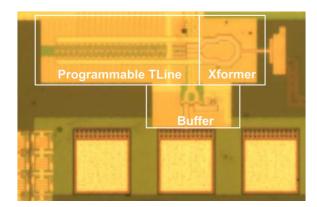


Fig. 21. DCO chip microphotograph.

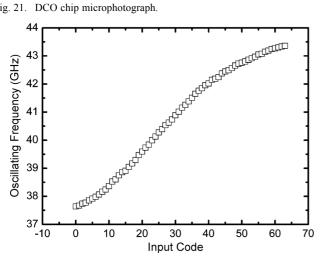


Fig. 22. Measured frequency tuning range of the DCO.

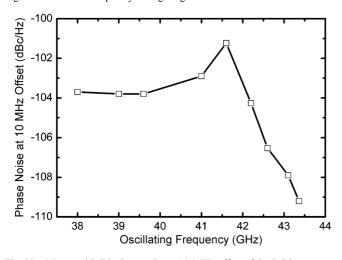
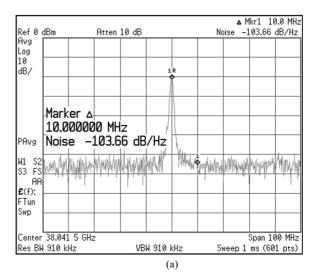
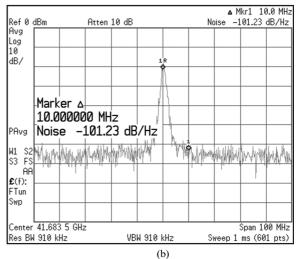


Fig. 23. Measured DCO phase noise at 10-MHz offset of the DCO.

B. A 40 GHz DCO With Linear Frequency Tuning

The chip micrograph of 40 GHz DCO is shown in Fig. 21. The core size is $0.5 \times 0.15 \text{ mm}^2$. The DCO consumes 20 mA under a 1.2 V power supply. Two on-chip DCO buffers are adopted to drive testing equipment and succeeding divider in a PLL respectively. They contribute a total capacitance of 90 fF. As the DCO has 4 bits for coarse tuning with VID-II, 2 bits for fine tuning with varactors, and 12 bits dithering though varactor controlled by $\Delta\Sigma$ modulator, the measured output frequency versus digital control codes (coarse + fine) is shown in Fig. 22. The output





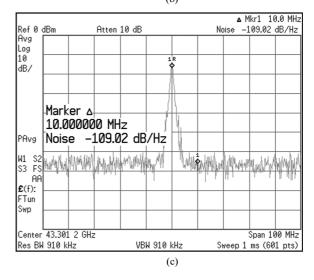


Fig. 24. Measured output spectrums of the 40 GHz DCO at: (a) 38 GHz; (b) 41.6 GHz; (c) 43.3 GHz.

frequency covers from 37.6 GHz to 43.4 GHz, which can be applied in a dual-IF 60 GHz UWB system (38.8 GHz to 43.2 GHz). The proposed DCO has 14% tuning percentage. The measured fine tuning step using varactor bank is about 100 MHz/step. By dithering unit varactor through a 12 bit, 2nd order $\Delta\Sigma$ modulator at 400 MHz, the corresponding minimum resolution is

Reference	[15]	[16]	[17]	[18]	[31]	[30]	This work	
Technology	90 nm	90 nm	130 nm	130 nm	90 nm	90 nm	90 nm	90 nm
Multi-band operation	without	without	without	without	DCO	DCO	with	DCO
$VDD/\Delta V_t$	1/N.A.	0.7/1.1	1/1	0.6/1	1.2/N.A.	1.2/N.A.	0.7/1.5	1.2/N.A.
Frequency range (GHz)	59.9-	73.8-	55-	66.7-	51.3-	58.27-	52.2-	37.6-
	60	79.3	61.5	69.8	53.3	63.83	61.3	43.4
Tuning percentage	0.2%	7.2%	10%	4.5%	4%	9.3%	16.07%	14%
Resolution	VCO	VCO	VCO	VCO	10 bits	2.3 bits	VCO	18 bits
PN at Δf	-100 at	-110 at	-95 at	-115.2 at	-116.5 at	-90.1 at	-118.75 at	-109 at
	1MHz	10MHz	1 MHz	10 MHz	10MHz	1MHz	10 MHz	10MHz
Power consumption	1.9 mW	13.58 mW	3.9 mW	4.32 mW	2.34 mW	10.6 mW	8.7 mW	19 mW
FOM	-192.8	-176.3	-184.4	-184	-187.2	-175.5	-184.3	-168.9
FOM_T	-158.8	-173.5	-184.4	-177	-179.2	-174.9	-187.4	-171.9
$FOM_{T/V}$	N.A.	-172.7	-184.4	-177	N.A	N.A	-185.8	N.A

TABLE I PERFORMANCE BENCHMARK

about 24 kHz/step by simulation. Taking signal loss caused by experimental setup into account (including the loss of probes, cables and adapters), the output power varies from -15 dBm to -11 dBm due to the variation of quality factor within the entire frequency tuning range. The measured phase noise performance at 10-MHz offset within the entire frequency tuning range is plotted in Fig. 23. Fig. 24 shows the measured VCO output spectrums at different frequencies.

The performance benchmark of the proposed oscillators and the prior art in the literature are summarized in Table I. Three different figures of merits are illustrated to investigate their advantages. They are

$$FOM = PN - 20 \log \left(\frac{f_o}{\Delta f}\right) + 10 \log \left(\frac{P_{cons}}{1 \text{ mW}}\right)$$
(17)

$$FOM_T = PN - 20 \log \left(\frac{f_o}{\Delta f} \frac{TP}{10\%}\right) + 10 \log \left(\frac{P_{cons}}{1 \text{ mW}}\right)$$
(18)

$$FOM_{T/V} = PN - 20 \log \left(\frac{f_o}{\Delta f} \frac{TP}{10\%} \frac{1 \text{ V}}{\Delta V_t}\right)$$

$$+10 \log \left(\frac{P_{cons}}{1 \text{ mW}}\right)$$
(19)

where PN is the phase noise at the offset frequency Δf , f_o is the oscillating frequency, P_{cons} is the power consumption, TP is the frequency tuning percentage, and ΔV_t is tuning voltage range. For over 50-GHz operating frequency, the proposed VCO has the widest frequency tuning range, the best FOM_T and $FOM_{T/V}$. On the other hand, the proposed DCO has the widest tuning range for over 40 GHz operation frequency, while also manifests the finest frequency resolution of 24 kHz. Compared to the FoM of VCO, it suggests that the Q-factor of DCO tank is compromised with resolution and tuning range.

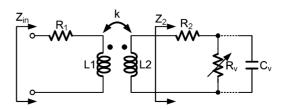


Fig. 25. The modified lump model of the VID.

V. CONCLUSION

Novel variable inductors for VCO and DCO are proposed in this paper. By using the proposed frequency tuning scheme, both VCO and DCO are capable of operating at MMW frequency band while manifesting wider tuning range than those VCOs with varactors for frequency tuning. In addition, multiband operation can be achieved without sacrificing its oscillating frequency or consuming large chip area. Both the VCO and DCO are capable of operating at supply voltage as low as 0.7 V. They manifest strong potential to be applied in the 60-GHz UWB system.

APPENDIX

Fig. 25 shows the modified lumped model of the VID to analyze its equivalent quality factor Q_{eq} . R_1 and R_2 respectively represent the parasitic resistors at the primary and secondary coils. The input impedance $Z_{\rm in}$ can be calculated as

$$Z_{in} = R_1 + j\omega L_1 + \frac{\omega^2 k^2 L_1 L_2}{j\omega L_2 + Z_2}$$
 (20)

$$Q_{eq} = \frac{\operatorname{Im}(Z_{in})}{\operatorname{Re}(Z_{in})}$$

$$= \omega \cdot \frac{R_v^2 L_1 (1 - \omega^2 C_v L_2)^2 + \omega^2 L_1 L_2^2 (1 - k^2) + \omega^2 k^2 R_v^2 C_v L_1 L_2 (1 - \omega^2 L_2 C_v)}{R_1 R_v^2 (1 - \omega^2 C_v L_2)^2 + \omega^2 L_2 (k^2 L_1 R_v - R_1 L_2)}$$
(23)

where

$$Z_{2} = \frac{R_{2} + R_{v} + j\omega C_{v} R_{2} R_{v}}{1 + j\omega C_{v} R_{v}}$$
(21)

In general, R_2 is much smaller than R_v . Thus, when $\omega \ll 1/C_v R_2$, Z_2 can be simplified as

$$Z_2 = \frac{R_v}{1 + j\omega C_v R_v} \tag{22}$$

The equivalent quality factor Q_{eq} of the VID can be calculated as shown in the equation at the top of the page.

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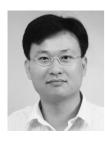
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