A 2.4-GHz Low-Flicker-Noise CMOS Sub-Harmonic Receiver

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***Abstract*—A 2.4-GHz low-noise sub-harmonic direct-conversion receiver (SH-DCR) is demonstrated using standard 0.18-μm CMOS technology. Deep-n-well vertical-NPN (V-NPN) bipolar junction transistors (BJTs) are employed to solve the flicker noise problem in CMOS process. Design optimization of a power-constrained noise-impedance-matched low-noise amplifier (LNA) with the effect of lossy on-chip inductors is fully discussed in this paper. A multi-stage octet-phase polyphase filter is analyzed in detail and implemented to generate well balanced octet-phase LO signals. As a result, the demonstrated receiver achieves 51-dB voltage gain and 3-dB noise figure with flicker noise corner less than 30 kHz when RF $= 2.4$ GHz. The I/Q amplitude/phase mismatch is below ± 0.2 dB/$\pm 1°$, respectively, covering from 2.35 to 2.6 GHz. The dc current consumption is 5 mA at a 1.8-V supply.**

***Index Terms*—Direct-conversion receiver (DCR), low-noise amplifier (LNA), sub-harmonic mixer (SHM), vertical-NPN (V-NPN), octet-phase.**

I. Introduction

RECENTLY, DIRECT-CONVERSION RECEIVERs (DCRs) have been widely researched and implemented for their high integration level and low power consumption when compared with the heterodyne receivers [1]–[3]. The discrete RF image-rejection filter and the IF high-Q channel select filters of a heterodyne receiver are the two fundamental hindrances for the monolithic integration. On the contrary, the RF image-rejection filter can be eliminated in a DCR because there is no image channel. Besides, the entire CMOS DCR can be implemented alongside the baseband DSP in a single inexpensive chip. Since the DCR down-converts the RF signal directly to baseband $(\mathrm{IF} = 0)$, the power dissipation of the high-order channel-selection active filter in a DCR is lower than that in a heterodyne receiver with a higher IF frequency for the same selectivity.

However, a CMOS DCR has inherently serious flicker noise, IIP_2 and dc offset problems because the MOS device itself has very large flicker noise and mismatch [4]. A deep-n-well vertical-NPN (V-NPN) bipolar junction transistor (BJT), available in a standard low-cost 0.18-μm CMOS process, has low flicker noise and good device matching (beneficial for low IM_2 and dc offset) and thus is especially suitable for a DCR [5], [6]. Further, a sub-harmonic mixer (SHM) topology is chosen in this work to achieve a low dc offset because of its additional LO rejection (LOR) [7]–[9].

For a single-quadrature I/Q DCR, either RF or LO should be in quadrature. As a result, there are two main types of I/Q SHM topologies to achieve an I/Q SH-DCR. For the corresponding SHMs, an equivalent differential switching operation at 2LO frequency requires that the LO signal should be in quadrature as shown in Fig. 1(a) while a quadrature 2LO operation straightforwardly requires octet-phase LO signals as shown in Fig. 1(b). Thus, Fig. 1(a) consists of both quadrature RF and LO signals [9] while Fig. 1(b) consists of differential RF but octet-phase LO signals [7], [10], [11]. The IF quadrature phase accuracy is determined by the RF quadrature generator while the quadrature LO signals are only used to perform a 2LO differential switching operation in the former topology. Thus, the former topology has lower loss in the LO signal generation. However, the loss of the RF quadrature generator is especially undesirable in a high-gain low-noise receiver. On the other hand, an octet-phase LO topology can be employed to avoid the additional RF loss through the gain path as long as the LO power is sufficient and balanced octet-phase LO signals can be generated. A BJT switching core requires a smaller LO power than an MOS switching core and the use of V-NPN BJT with its low cut-off frequency (f_{T}) of 2 GHz does not cause performance degradation because the LO frequency ($\sim$1.2 GHz) is only half the RF frequency for a sub-harmonic mixing operation. Thus, in this work, the latter topology incorporating a multi-stage octet-phase polyphase filter (PPF) [12] is chosen to generate well balanced octet-phase LO signals. A thorough analysis of the octet-phase polyphase filter is also described in this paper.

This paper describes the design, analysis and implementation of a low-power low-noise RF receiver for 2.4-GHz-band IEEE 802.15.4 standard. Because the applications of this standard are commercial, home automation, industrial, consumer electronics, personal health care, and game, these electric devices should operate from several months to a year on one battery without changing. Thus, low cost and low power are key issues.

The block diagram of the proposed SH-DCR is shown in Fig. 1(b), including a single-ended-input LNA, I/Q SHMs with BJT switching core, I/Q variable-gain amplifiers (VGAs) and an LO octet-phase PPF. Circuit design optimizations are deeply described in Section II while Section III reports the measurement

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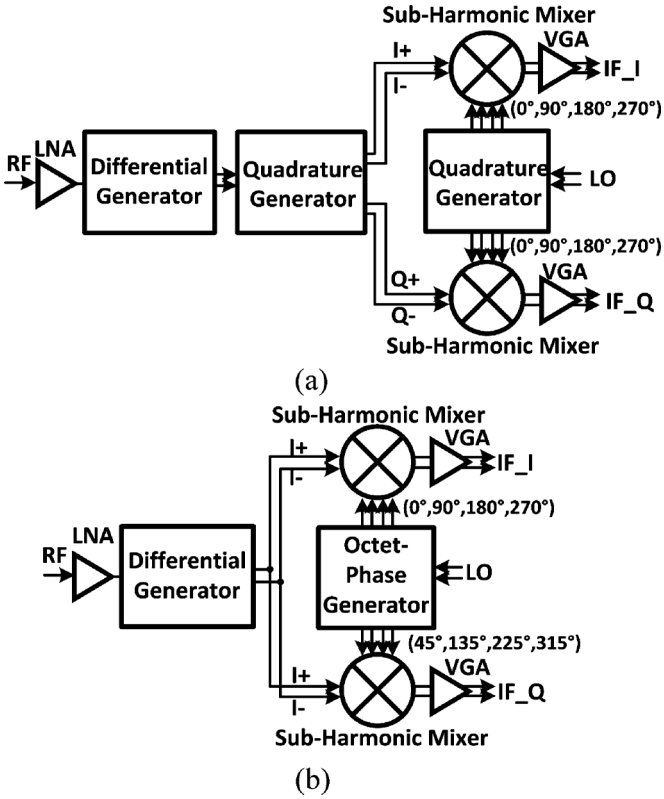

Fig. 1. Block diagram of an I/Q sub-harmonic direct-conversion receiver with (a) both quadrature RF and LO signals (b) differential RF and octet-phase LO signals.

results and compares with simulation results. Conclusions are given in Section IV. After detailed analysis and design optimization in each function block, the proposed SH-DCR achieves 51-dB voltage gain and 3-dB NF at 2.4 GHz, while the total current consumption is only 5 mA. The performance is comparable and even better than that of other 2.4 GHz receivers based on fundamental mixing or using advanced technology.

II. Circuit Design and Implementation

A. Low-Power LNA Design Optimization With On-Chip Low-Q Inductors at a Fixed Power Consumption

A low-noise amplifier (LNA) plays an important role in a receiver and its power consumption usually dominates the whole receiver. The optimization of an LNA is urgently required. The schematic of a widely used cascode LNA with a source degeneration inductor ($L_{\rm s}$) is shown in Fig. 2. The $L_{\rm s}$ is used to make the optimal noise impedance and input impedance almost equal. The cascode structure provide good reverse isolation to avoid the LO leakage leaking back to the RF input and even to the antenna.

1) Input Matching With the Effect of Low-Q Inductors: The input impedance of a cascode LNA, shown in Fig. 2, can be expressed as

$$Z'_{in} = (sL_g + R_{Lg}) + (sL_s + R_{Ls}) + 1/(sC_t) + g_m(sL_s + R_{Ls})/(sC_t) \quad (1)$$

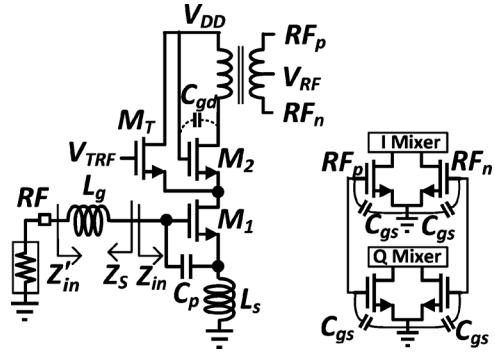

Fig. 2. Schematic of a cascode LNA with a single-to-differential transformer connecting to the transconductance stage of the following I/Q Gilbert mixers.

where R_{Lg}/R_{Ls} represent the series resistance of the inductance $L_{\rm g}/L_{\rm s}$. Typically, R_{Ls} is much smaller than R_{Lg} and can be neglected. $C_t = C_{\rm gs} + C_p$ when a parallel capacitance C_p is applied.

Since an on-chip planar inductor can be modeled as an inductor L in series with a resistor R when the operating frequency is lower than $f_{\rm Qmax}$. Here, Q_L of an inductor is defined as $\omega_0 L/R$. Generally speaking, the series resistance is proportional to the geometric length and thus proportional to the series inductance. That is, $R = (\omega_0/Q)L \equiv \alpha_0 L$, where α_0 is close to a constant, only relating to the geometrical shape (including metal width, spacing and metal thickness). Thus, the $Z'_{\rm in}$ in (1) can be modified as

$$Z'_{\rm in} = \alpha_0(L_g + L_s) + g_m L_s/C_t + s(L_g + L_s) + (1 + g_m\alpha_0 L_s)/(sC_t). \quad (2)$$

To achieve impedance matching at a target resonance frequency (ω_0) and the target matching impedance $R_S = 50\ \Omega$ when the device size ($\rm C_{gs}$) (or $\rm C_t$) and bias ($\rm g_m$) are decided,

$$\begin{cases} R'_{\rm in} = \alpha_0(L_g + L_s) + g_m L_s/C_t = R_S \\ \dfrac{1 + g_m\alpha_0 L_s}{(L_g + L_s)C_t} = \omega_0^2 \end{cases}. \quad (3)$$

Thus

$$L_s = \frac{R_S C_t}{g_m}\left(1 - \frac{\alpha_0}{\omega_0^2 C_t R_S}\right) \Big/ \left[1 + \left(\frac{\alpha_0}{\omega_0}\right)^2\right] \quad (4)$$

and

$$L_g = \frac{1 + g_m\alpha_0 L_s}{\omega_0^2 C_t} - L_s. \quad (5)$$

Note that, if no series resistance R_{Lg} is considered (i.e., $\alpha_0 = 0$), the well-known results for impedance matching are $L_s = R_S C_t/g_m$ and $L_g = 1/(\omega_0^2 C_t) - L_s$.

Besides, the transconductance gain of the input transistor $\rm M_1$ at resonance can be expressed as

$$|G_m(\omega_0)| = \frac{1}{R_S}\frac{g_m}{\omega_0 C_t} = \frac{g_m Q_S}{1 + g_m R_{Ls}} \approx g_m Q_S \quad (6)$$

where $Q_S = \omega_0(L_g + L_s)/R_S = (1 + g_m R_{Ls})/(\omega_0 C_t R_S)$ is the quality factor of the input impedance.

2) PCSNIM Method With the Effect of Low-Q Inductors: Conventionally, for the power-constraint simultaneous noise

impedance matching (PCSNIM) method proposed in [13], a C_p is applied to modify the $\mathrm{Re}\{Z_{\mathrm{opt}}\}$ without changing the $\mathrm{NF}_{\mathrm{min}}$ and makes the noise and impedance matching achieved at the same time for every transistor size at a fixed I_{D} when R_{Lg} is negligible. However, when considering the extrinsic R_{Lg} (i.e., $\alpha_0 \neq 0$), the noise factor (F) has one additional term of $(R_{Lg}+R_{Ls})/R_{\mathrm{S}}$ when compared to the $F(\alpha_0=0)$ [14], i.e.,

$$F \approx 1+\frac{R_{Lg}+R_{Ls}}{R_S}+\gamma g_{d0}R_S\left(\frac{\omega_0}{\omega_T}\right)^2\left[1+\frac{\delta\alpha^2}{5\gamma}\right] +2|c|\left(\frac{\omega_0}{\omega_T}\right)\sqrt{\frac{\delta\gamma}{5}}+\frac{\delta}{5g_{d0}R_S} \quad (7)$$

where $\alpha=\mathrm{g_m}/\mathrm{g_{d0}}$, γ is a constant for the channel thermal noise current, δ is a constant for the gate induced noise current, and c is a correlation coefficient of the gate-induced noise current and the channel noise current.

Therefore, the series resistances of on-chip low-Q inductors make the NF increase dramatically and even dominate the overall NF. Instead of complicated mathematical NF derivations [15], a clearer and more useful graphical method based on simulation is proposed in this paper for the NF optimization with the effect of low-Q inductors.

Here, a cascode LNA with a parallel RLC resonance load ($=400\ \Omega$ at resonance) as shown in Fig. 2 is simulated for different transistor size $(\mathrm{W_1})$ of $\mathrm{M_1}$, series inductance L_g/L_s and C_p, while the gate width $(\mathrm{W_2})$ of $\mathrm{M_2}$ is 240 μm and the RLC tank is resonated at 2.4 GHz. All of the device gate lengths are kept at 0.18 μm. The device model is BSIM3v3.24 provided by the foundry. Here, $\alpha_0=0$, 1, and 2 Ω/nH are simulated for both L_g and L_s and the corresponding $Q_L=\omega_0/\alpha_0=\infty$, 15, and 7.5 at 2.4 GHz. $\alpha_0=2$ Ω/nH is especially addressed because it is the typical value of an on-chip spiral inductor using ultra-thick metal (UTM) and metal width is 6 μm while the f_{Qmax} is still higher than the operating frequency.

Fig. 3 shows the simulation results of the cascode LNA w/ C_p following a PCSNIM method while $I_{\mathrm{D}}=2.5$ mA. The C_p chosen for optimal noise performance and the $C_t=C_{\mathrm{gs}}+C_p$ are drawn in Fig. 3(a). However, no C_p is required to achieve noise matching when $\mathrm{W_1}$ is larger than 600 μm. The corresponding L_{s} and L_{g} are drawn in Fig. 3(b). Fig. 3(c) and (d) show the corresponding achievable NF and $\mathrm{A_V}$ (voltage gain), respectively. The line with square symbols in Fig. 3(c) clearly shows the results using PCSNIM but without R_{Lg}. When considering low-Q (high-α_0) inductors, a higher α_0 of an inductor requires a larger C_p to reduce the required L_g and the corresponding R_{Lg} for an optimal overall NF, as shown in Figs. 3(a) and (b). This advantage is much more significant than the reduction of the device noise. As a result, when considering the R_{Lg}, the minimum achievable NF w/ C_p [in Fig. 3(c)] is lower than the NF w/o C_p [in Fig. 4(b)] for a given α_0. Note that, when $\alpha_0\neq 0$, the $\mathrm{A_V}$ using PCNO decreases progressively when $\mathrm{W_1}$ increases as shown in Fig. 4(c). However, when using PCSNIM with low-Q inductors, the applied C_p degrades the overall G_m of the LNA as shown in (6) while the device $\mathrm{NF}_{\mathrm{min}}$ remains the same especially for a small transistor size. Thus, not only the NF but also $\mathrm{A_V}$ has an optimal device size when R_{Lg} is considered. Besides, the optimal width increases if a larger α_0 is applied as

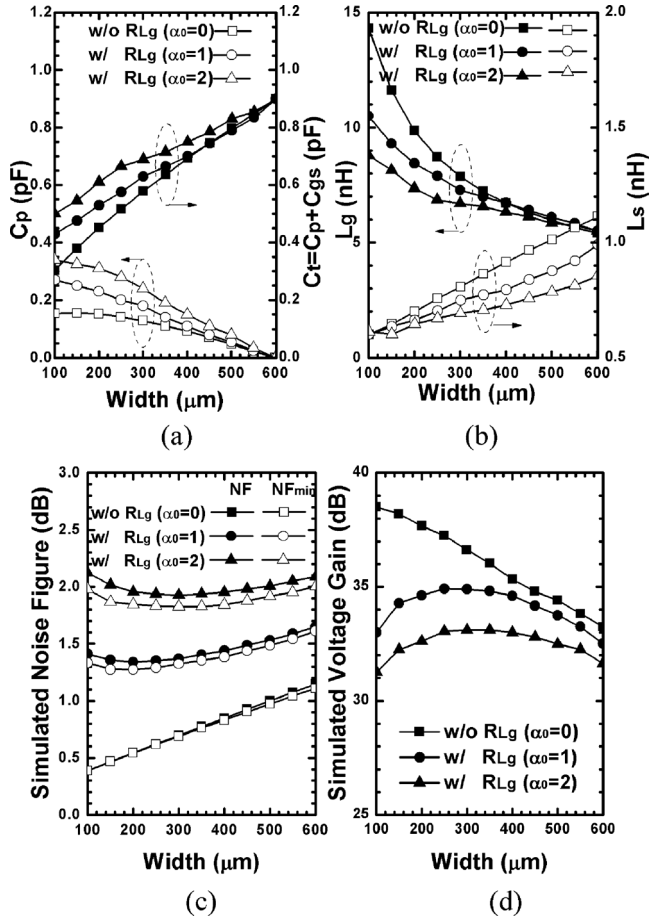

Fig. 3. (a) C_p and $C_t(=C_p+C_{gs}$ (b) L_g and L_s for power-constrained simultaneous noise and impedance matching at 2.4 GHz and the corresponding (c) simulated noise figure and (d) simulated voltage gain of the cascode LNA with C_p while the supply current is 2.5 mA. The unit for α_0 is Ω/nH.

shown in Fig. 3(c) and (d). As a result, the C_p for minimum achievable NF is around 0.2–0.3 pF when $\alpha_0=2$ Ω/nH. The corresponding L_g is around 6–7 nH, which is implementable and occupies a small die area. The minimum NF is below 2 dB and $\mathrm{A_V}$ is above 33 dB when $\mathrm{W_1}$ ranges from 200 to 400 μm ($J_{\mathrm{D}}=6.5$–12.5 μA/μm).

Further, if the matching condition is not limited to a perfect 50 Ω, i.e., a smaller matching impedance R_{S} is selected, the $\mathrm{A_V}$ also increases, as predicted in (6) and NF slightly decreases due to the smaller R_{Lg} at the cost of the matching bandwidth. Thus, changing the matched impedance to around 35–40 Ω by decreasing the L_s results in a higher $\mathrm{A_V}$, a lower NF and allowable matching bandwidth. Finally, the $\mathrm{W_1}=240$ μm (4-μm unit width $\times$ 60 fingers) is chosen to achieve both optimal NF and $\mathrm{A_V}$.

As shown in Fig. 2, a transformer is used as the load of the cascode LNA, instead of the parallel LC resonance load, to transform the single-ended LNA current into differential voltage output for I/Q mixers. Thus, a 5:4 transformer is used. The line width, line spacing and the outer diameter of the implemented transformer are 9 μm, 2 μm and 290 μm, respectively. In addition, a tuning transistor $(\mathrm{M_T})$ is used to achieve the gain reduction by drawing out the RF current if the gate bias of $\mathrm{M_T}$ increases when a large RF signal is applied.

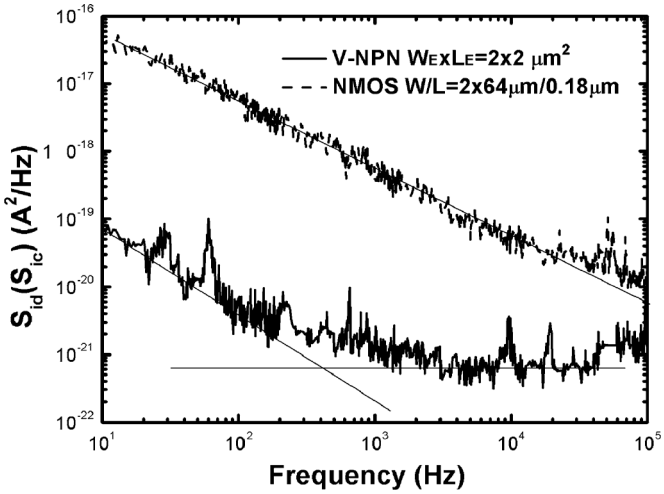

Fig. 4. Measured output noise current spectral density of the V-NPN BJT and 0.18-μm NMOS device. $\mathrm{I_{dc}} = 250\ \mu\mathrm{A}$.

B. I/Q Sub-Harmonic Mixer Using V-NPN BJTs

The output noise current spectral density for V-NPN BJT (with $\mathrm{W_E} \times \mathrm{L_E} = 2 \times 2\ \mu\mathrm{m}^2$) and NMOS (with $\mathrm{W/L} = 2 \times 64\ \mu\mathrm{m}/\ 0.18\ \mu\mathrm{m}$) devices is measured using an Agilent 35670A dynamic signal analyzer as shown in Fig. 4. The V-NPN BJT has roughly 400-Hz flicker noise corner at $I_C = 250\ \mu$A while the NMOS device has the flicker noise corner beyond MHz at the same dc current. V-NPN BJTs can be obtained without extra cost in a deep-n-well CMOS technology [5], [6]. The source-drain diffusion functions as the emitter, the p-well as the base, and the deep-n-well as the collector.

The flicker noise of the LO switching core directly leaks to the output at the zero-crossing, while the flicker noise of the RF stage is upconverted to the odd harmonics of the LO frequency [16]. Thus, a CMOS active Gilbert mixer has a several MHz flicker noise corner and becomes an unacceptable weakness for a DCR, especially in a narrow IF band application. As a result, V-NPN BJTs are used to replace the LO core devices, directly eliminating the device flicker noise source of the LO switching core [5]. In addition, the f_{T} of the V-NPN BJT are around 2 GHz, which is enough for a 2.4-GHz SHM because the LO frequency is only 1.2 GHz.

As shown in Fig. 5, there are three main kinds of SHMs, including stacked-LO [7], top-LO [9], [10], [17], and bottom-LO [18] topologies. A 1.8-V supply voltage, compatible to digital circuits, is not sufficient for the stacked-LO topology consisting of the cascode LO core, RF g_m stage and IF resistive or PMOS load as shown in Fig. 5(a). Besides, if the V-NPN BJTs are applied to the LO cores in a bottom-LO SHM, as shown in Fig. 5(b), it still has severe flicker noise problem because the flicker noise of the RF transistors directly leaks to the output. However, the V-NPN BJT is not suitable for an RF g_m stage because of the low f_T and high parasitic resistance (R_E, R_B, and R_C). On the other hand, the top-LO SHM has better 2LO-to-RF isolation than the others because the four transistors fed by the quadrature phases LO signals are connected at the emitter node, $\mathrm{V_{E1}}$ or $\mathrm{V_{E2}}$, and thus the 2LO frequency component is inherently cancelled, as shown in Fig. 5(c) [19].

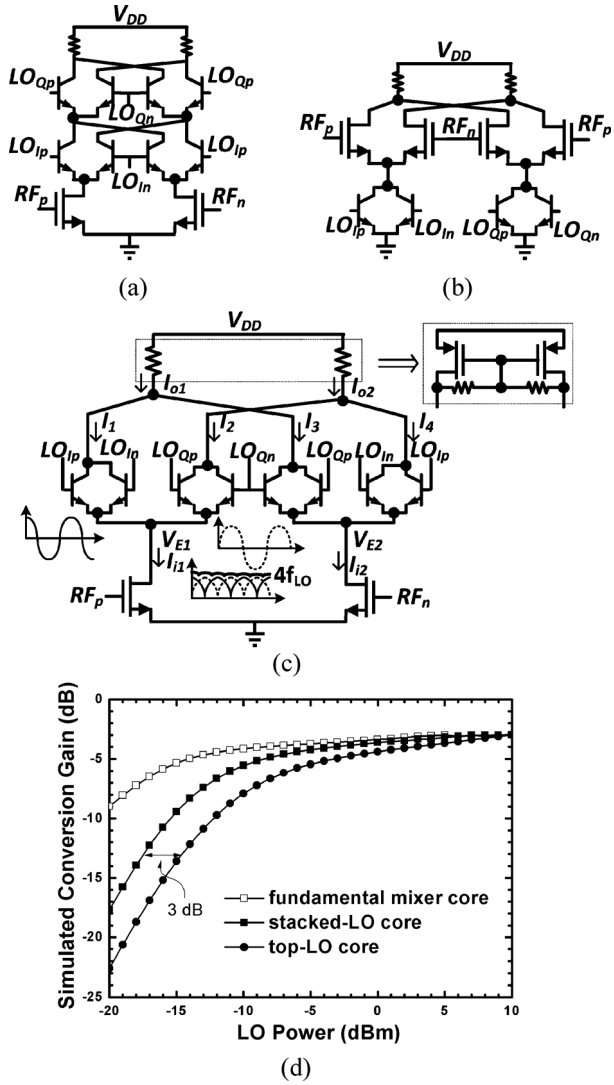

Fig. 5. (a) Stacked-LO sub-harmonic mixer (SHM) (b) bottom-LO SHM (c) top-LO SHM with V-NPN BJTs in LO core (d) simulated current conversion gain of the switching core for a fundamental mixer, a stacked-LO mixer and a top-LO mixer core.

As a result, the top-LO SHM as shown in Fig. 5(c) is chosen in this work to simultaneously fulfill both the supply-voltage requirement and the gain/noise performance. Active PMOS loads with a 2 μm gate length to guarantee the flicker noise less than 10 kHz are applied in this work. The top-LO SHM requires a 3-dB larger LO power than a stacked-LO one, which is derived in Appendix B and the simulation results at $\mathrm{RF} = 2.4$ GHz are drawn in Fig. 5(d) and compared to a fundamental mixer. Thus, the LO octet-phase generator should be carefully chosen and designed to reduce the unwanted LO loss. Although an SHM requires larger LO power than a fundamental mixer, there is still a flat-gain region to a certain extent and can tolerate the amplitude imbalance of the LO signals.

C. LO Multi-Stage Octet-Phase Polyphase Filter

A well-known multi-stage PPF is widely employed as a differential-quadrature generator [20]. However, an octet-phase PPF should be applied to generate the eight vectors required by the top-LO I/Q SHMs. As shown in Fig. 6, a single stage PPF

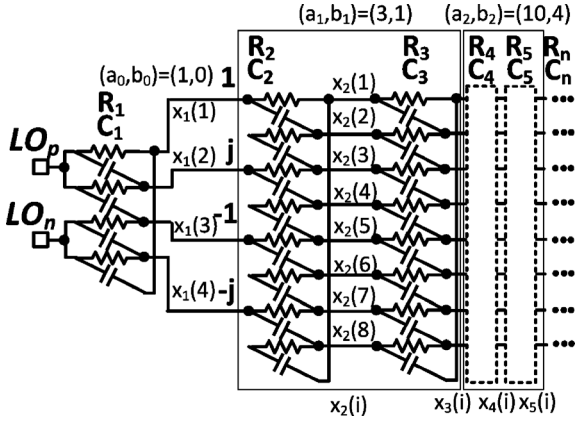

Fig. 6. Schematic of a multi-stage octet-phase polyphase filter.

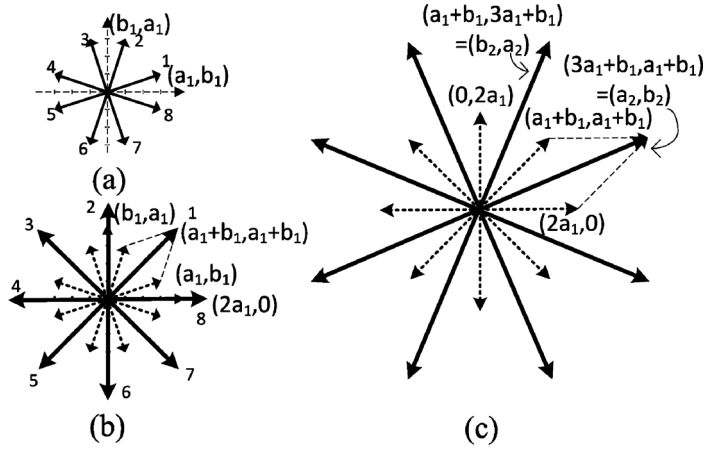

Fig. 7. Phasor diagram at (a) second (b) third stage and (c) fourth stage.

is applied at the first stage to generate differential-quadrature outputs (i.e., $[x_1(1), x_1(2), x_1(3), x_1(4)] = [1, j, -1, -j]$) at the center frequency (ω_0) in spite of loadings [20]. The four vectors are further split into eight vectors $x_2(i), i \in \{1, 2, \ldots, 8\}$ by (8), shown at the bottom of the page, and $x_2(k+2) = jx_2(k), k \in \{1, 2, \ldots, 6\}$.

Fig. 7(a) shows the vector diagram at the second-stage output. Here, the common denominator is neglected because it only affects the absolute (not relative) gain and phase. Here, we define two variables to quantify the octet-phase signal accuracy

$$\mathrm{AD(amplitude\ difference)} = \frac{|V(k)|}{|V(l)|} \tag{9}$$

and

$$\mathrm{PE(phase\ error)} = |\phi(k) - \phi(l) - 45^\circ| \tag{10}$$

where $|k-l| = 1$, and $k, l \in \{1, 2, \ldots, 8\}$.

As a result, all $|x_2(k)|$ are the same (i.e., $\mathrm{AD} = 1$) but the PE is $|\arctan(3) - \arctan(1/3) - 45^\circ)| = 8.13^\circ$, which is not acceptable in a real application.

From the third stage, the gain of each stage follows:

$$\begin{aligned} x_n(k) &= \frac{j\omega/\omega_0 x_{n-1}(k-1) + x_{n-1}(k)}{1 + j\omega/\omega_0} \\ &= \frac{jx_{n-1}(k-1) + x_{n-1}(k)}{1+j} \\ &= \frac{x_{n-1}(k+1) + x_{n-1}(k)}{1+j} \end{aligned} \tag{11}$$

where $k \in \{1, 2, \ldots, 8\}$ and define $x_{n-1}(0) = x_{n-1}(8)$.

Here, $x_{n-1}(k+1) = jx_{n-1}(k-1)$ holds if the quadrature signal at the first stage is perfect. The output vectors at the third stage are shown in Fig. 7(b). Thus, perfect 45° phase difference is obtained (i.e., $\mathrm{PE} = 0^\circ$) but $\mathrm{AD} = 3/(2\sqrt{2}) = 0.51$ dB.

If we extend the analysis to more stages, the results are summarized as follows.

1) At the even $(2n_{\mathrm{th}})$ stage, the eight vectors are $(\pm a_{\mathrm{n}}, \pm b_{\mathrm{n}})$, and $(\pm b_{\mathrm{n}}, \pm a_{\mathrm{n}})$ where $a_n \geq b_n$ is assumed. As a result, we get (12), shown at the bottom of the page.
2) At the odd $[(2n+1)_{\mathrm{th}}]$ stage, the eight vectors are $(\pm 2a_{\mathrm{n}}, 0), (0, \pm 2a_{\mathrm{n}})$, and $(\pm(a_{\mathrm{n}} + b_{\mathrm{n}}), \pm(a_{\mathrm{n}} + b_{\mathrm{n}}))$. Thus

$$\begin{cases} \mathrm{AD} = \dfrac{\sqrt{2}a_n}{(a_n + b_n)} \\ \mathrm{PE} = 0^\circ \end{cases}. \tag{13}$$

Note that, following Fig. 7(a)–(c), the recursive formula can be directly obtained

$$\begin{bmatrix} a_{n+1} \\ b_{n+1} \end{bmatrix} = X \begin{bmatrix} a_n \\ b_n \end{bmatrix} = \begin{bmatrix} 3 & 1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} a_n \\ b_n \end{bmatrix} \tag{14}$$

and $(a_1, b_1) = (3, 1)$.

It is interesting that, after more stages are cascaded, perfect octet outputs with balanced amplitude/phase are achieved eventually at either the even or odd stage. The detailed derivations are summarized in Appendix A. However, the voltage

$$\begin{cases} x_2(1) = \dfrac{-jR + 2/(sC) + R}{2[R + 1/(sC)]} = \dfrac{(2 + \omega/\omega_0) + j(\omega/\omega_0)}{2(1 + j\omega/\omega_0)} \overset{(\omega=\omega_0)}{=} \dfrac{3+j}{2(1+j)} \\ x_2(2) = \dfrac{2R + 1/(sC) + j/sC}{2[R + 1/(sC)]} = \dfrac{1 + j(1 + 2\omega/\omega_0)}{2(1 + j\omega/\omega_0)} \overset{(\omega=\omega_0)}{=} \dfrac{1+3j}{2(1+j)} \end{cases} \tag{8}$$

$$\begin{cases} \mathrm{AD} = 1 \\ \mathrm{PE} = \left| \arctan\left(\dfrac{a_n}{b_n}\right) - \arctan\left(\dfrac{b_n}{a_n}\right) - 45^\circ \right| = \arctan\left| \dfrac{a_n^2 - b_n^2 - 2a_n b_n}{a_n^2 - b_n^2 + 2a_n b_n} \right| \end{cases}. \tag{12}$$

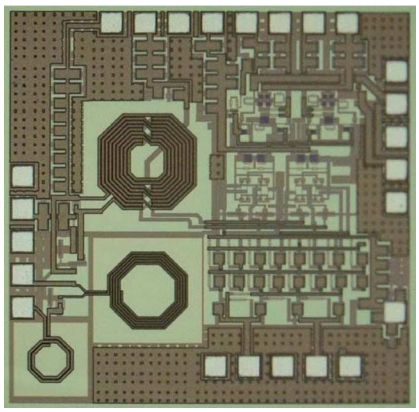

Fig. 8. Die photo of the proposed 2.4-GHz sub-harmonic receiver.

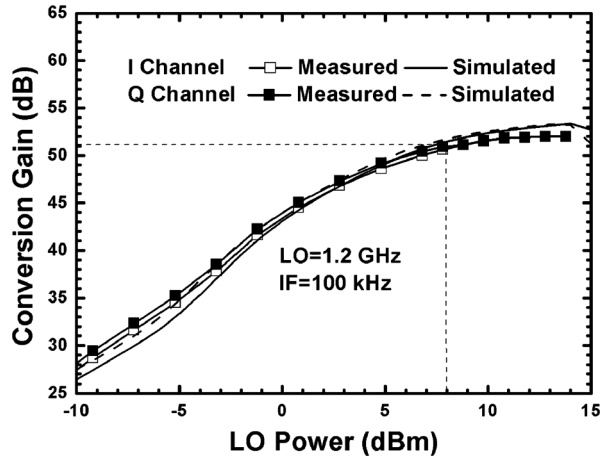

Fig. 9. Conversion gain with respect to LO power of the proposed 2.4-GHz sub-harmonic receiver.

loss when cascading many stages is unacceptably large. As a result, a three-stage octet-phase PPF is employed in consideration of both voltage loss and signal accuracy. A 0.51-dB LO amplitude imbalance is tolerable because when the LO signal is large enough for an active mixer, the mixer output amplitude imbalance is even smaller, as shown in Fig. 9(d).

Finally, an IF VGA with around 20-dB linear-in-dB tuning range is implemented using an R-r attenuation method [21], [22]. In addition, the V-NPN BJTs are used at the input g_m stage because of the ultra-low flicker noise and the larger $g_{\rm m}$ under the same dc current consumption than NMOS transistors.

III. Measurement Results

The die photo of the 2.4-GHz SH-DCR is shown in Fig. 8, and the die size is 1.15×1.05 mm^2. On-wafer measurement facilitates the RF performance. Fig. 9 shows the conversion gain of each I/Q channel with respect to the LO power when $\mathrm{RF} = 2.4001$ GHz and $\mathrm{LO} = 1.2$ GHz. The CG of I/Q channel has around 0.7-dB gain difference at low LO power. When the LO power exceeds 8 dBm, the CG of both channels is almost the same, as discussed in Section II.B. A maximum CG is 52 dB when LO power exceeds 10 dBm. However, an 8-dBm LO power is applied for all the following measurements. Note that, the simulated power loss of the LO octet-phase generator is around 8 dB.

Fig. 10(a) shows the CG and NF as a function of RF frequency. The peak CG is 51.2 dB at 2.35 GHz with a 1-dB bandwidth ranging from 2.25 to 2.45 GHz while the minimum NF is 3 dB and less than 3.5 dB within 2.3–2.55 GHz. In addition, the input return loss is better than -10 dB from 2.0 to 2.6 GHz as shown in Fig. 10(b). Fig. 11 shows the NF with respect to IF frequency when $\mathrm{LO} = 1.2$ GHz. The NF is 3 dB at the highest gain while NF is 5 or 8 dB when the LNA gain is reduced by 5 or 10 dB, respectively. Further, the NF remains around 3 dB when the IF VGA is reduced by 10 dB. The flicker corner is much less than 30 kHz, which is limited by the noise source and dc block in NF measurement.

The I/Q output waveforms are shown in Fig. 12(a) with 0.04 dB gain difference and 0.04° phase error when $\mathrm{RF} = 2.4001$ GHz and $\mathrm{LO} = 1.2$ GHz. Fig. 12(b) shows the gain difference <0.2 dB and I/Q phase error $<1°$ when LO frequency ranges from 2.35 to 2.6 GHz. However, the phase error increases when

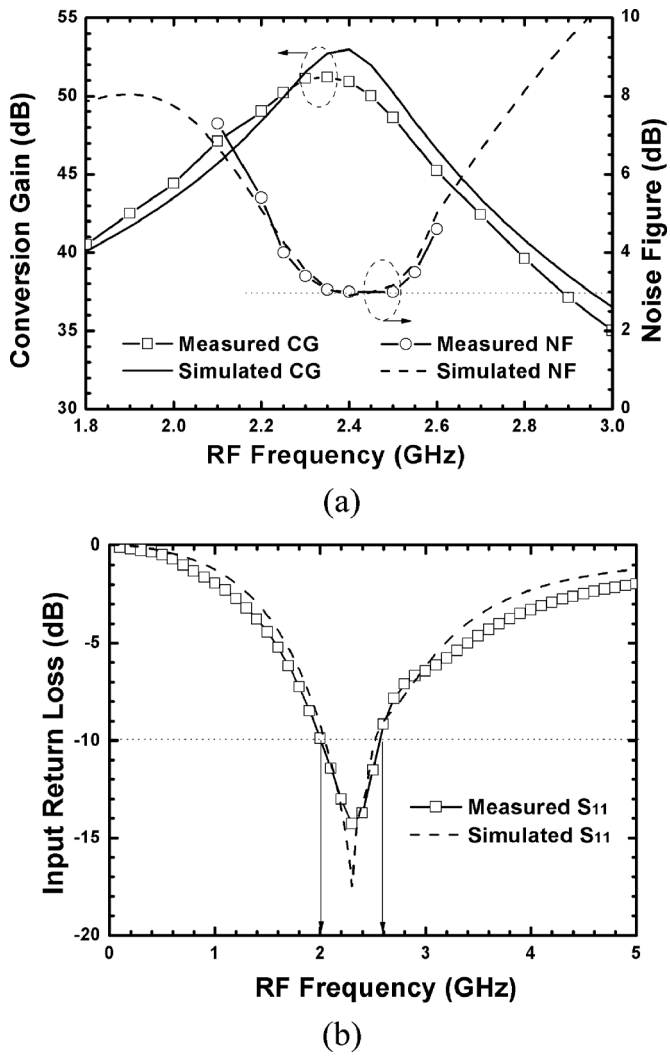

Fig. 10. (a) Conversion gain/noise figure (b) input return loss with respect to RF frequency of the proposed 2.4-GHz sub-harmonic receiver.

LO frequency is away from the designed center frequency of 1.2 GHz. Fig. 13(a) shows the CG as a function of the LNA RF tuning voltage ($\mathrm{V_{TRF}}$) while Fig. 13(b) indicates the CG

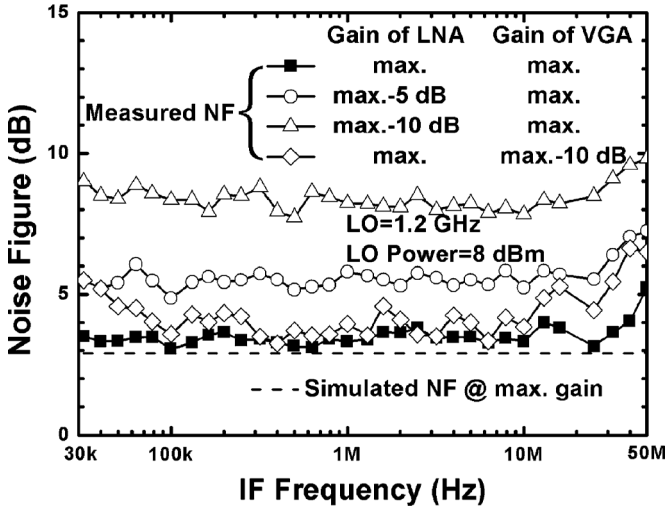

Fig. 11. Noise figure with respect to IF frequency of the proposed 2.4-GHz sub-harmonic receiver.

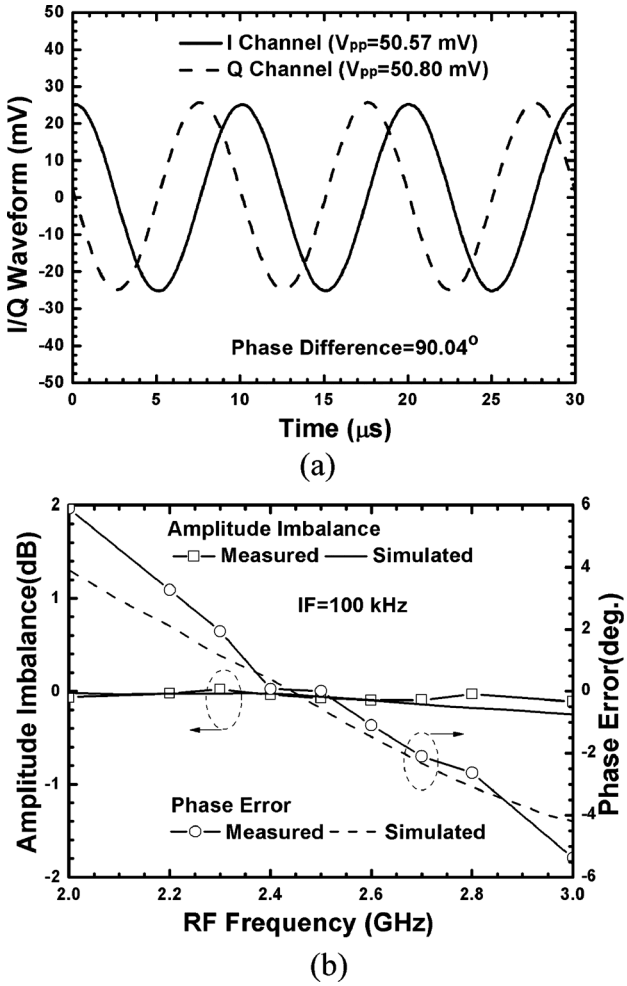

Fig. 12. (a) I/Q waveform at $\mathrm{RF} = 2.4001$ GHz, $\mathrm{LO} = 1.2$ GHz (b) amplitude imbalance and phase error of the proposed 2.4-GHz sub-harmonic receiver.

with respect to the VGA IF tuning voltage ($\mathrm{V_{TIF}}$). A tuning range of around 20 dB is achieved by each RF/IF tuning scheme. Fig. 14(a) shows the $\mathrm{IP_{1dB}}$ and $\mathrm{IIP_3}$ at different gain conditions by RF gain tuning while $\mathrm{IIP_2}$ of five random chips are measured and plotted in Fig. 14(b) individually since the $\mathrm{IIP_2}$ is related to the process variations and mismatches. Thus, the mean value of the $\mathrm{IIP_2}$ is 25 dBm at highest gain with at most 2 dB variation. The LO/2LO-to-RF leakage is defined as the LO/2LO power measured at the RF input port while the receiver is normally functioning with 8-dBm LO input power. Thus, the LO/2LO-to-RF leakage is less than $-77/-105$ dBm when the LO frequency ranges from 1.1 to 1.3 GHz, as shown in Fig. 15(a). The worst-case dc offset due to LO/2LO self-mixing is calculated following [11]

$$\begin{cases} V_{\mathrm{DC-offset}}(\text{due to LO}) = V_{\mathrm{LO-LEA}} \times \mathrm{CG_{LO}} \\ V_{\mathrm{DC-offset}}(\text{due to 2LO}) = V_{\mathrm{2LO-LEA}} \times \mathrm{CG_{2LO}} \end{cases}. \quad (14)$$

where $\mathrm{V_{LO-LEA}}/V_{\mathrm{2LO-LEA}}$ represents the observed LO/2LO leakage at the RF port and $\mathrm{CG_{LO}}/\mathrm{CG_{2LO}}$ stands for the conversion gain of a mixer when input signal at LO/2LO frequency is applied. Here, $\mathrm{CG_{2LO}} = \mathrm{CG}$ for an SH-DCR. Thus, the dc offset due to self-mixing is strongly reduced for an SHM and 50 dB LOR at $\mathrm{LO} = 1.2$ GHz is obtained, as shown in Fig. 15(a). The dc offset due to LO/2LO is drawn in Fig. 15(b). That is, an overall worst-case dc offset of 0.44 mV appears at the output. The circuit performance is summarized and compared with state-of-the-art DCRs in Table I [7], [9], [10], [23]. A MOS active mixer has typically over 1-MHz flicker noise corner [9]. Besides, even though only quadrature LO signals are required, the LO power is still high because of the MOS switching core. A separate bias of the mixer core and the RF g_{m} stage is applied in [10]. PMOS devices with lower flicker noise property and a lower dc current flowing into the mixer core result in a lower flicker noise leaking to IF output [10]. On the contrary, a g_{m} stage biased at a higher current can maintain sufficient linearity and noise figure of the active mixer. Passive mixer realization is an alternative for low flicker noise performance [23], [24] but the conversion loss of the passive mixer raises the NF floor if the preceding LNA does not have sufficient gain. The flicker noise problem can be avoided using SiGe HBT technology [7] or using V-NPN BJTs in low-cost CMOS process because of the device nature. However, the LO power requirement of this work is 4-dB lower than that in [7], even though the top-LO SHM in this work inherently requires 3-dB more LO power than the stacked-LO SHM in [7]. That is, the passive loss of the proposed octet-phase generator is very low. Table II compares the demonstrated 2.4-GHz BJT-based sub-harmonic receiver with the state-of-the-art 2.4-GHz low-power receivers based on fundamental mixing [1]–[3], [22], [25], [26] to further manifest the excellent performance of this work.

IV. Conclusion

A 2.4-GHz low-noise SH-DCR is demonstrated using parasitic V-NPN BJTs in a standard 0.18-μm CMOS process. The design optimization of the LNA with the trade-offs between extrinsic R_{Lg} thermal noise of low-Q inductors and intrinsic device $\mathrm{NF_{min}}$ at a fixed power dissipation is fully analyzed. An octet-phase PPF is used to generate balanced octet outputs for I/Q SHMs. As a result, the maximum CG is 51 dB and minimum NF is 3 dB with the flicker noise corner less than 30 kHz when $\mathrm{LO} = 1.2$ GHz.

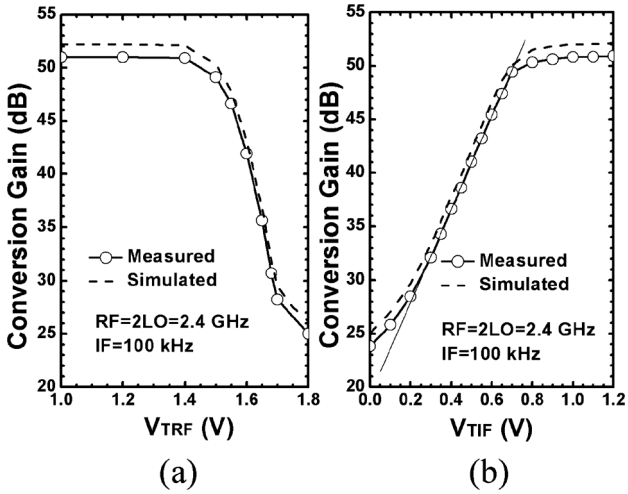

Fig. 13. Conversion gain with respect to (a) RF tuning voltage ($\mathrm{V_{TRF}}$) (b) IF tuning voltage ($\mathrm{V_{TIF}}$) of the proposed 2.4-GHz sub-harmonic receiver.

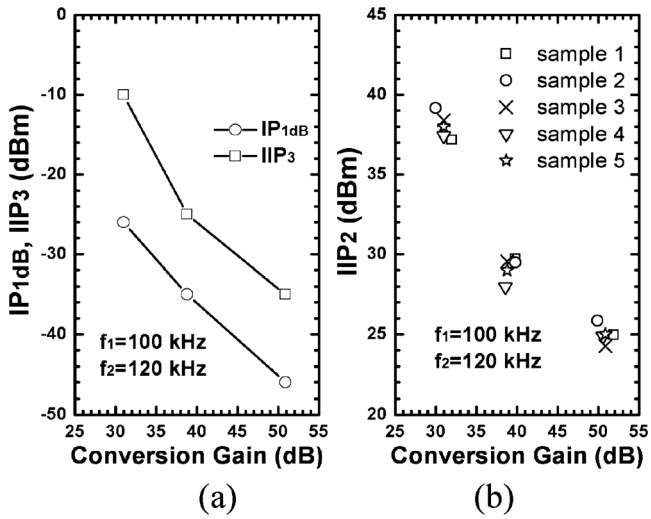

Fig. 14. (a) $\mathrm{IP_{1\,dB}}$ and $\mathrm{IIP_3}$ (b) $\mathrm{IIP_2}$ of the proposed 2.4-GHz sub-harmonic receiver.

Appendix A
Derivation of Amplitude/Phase Relations of a Multi-Stage Octet-Phase Polyphase Filter

For additional stages, the vector $[a_{\mathrm{n}}, b_{\mathrm{n}}]$ should be obtained first because both AD and PE can be formulated using it by (12) and (13). As mentioned in Section II.C,

$$\begin{bmatrix} a_{n+1} \\ b_{n+1} \end{bmatrix} = X \begin{bmatrix} a_n \\ b_n \end{bmatrix} = \begin{bmatrix} 3 & 1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} a_n \\ b_n \end{bmatrix} \tag{A1}$$

where $n \geq 1$.

The matrix X can be eigendecomposed to $X = VEV^{-1}$ where

$$V = \begin{bmatrix} v_1 & v_2 \\ -v_2 & v_1 \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{2}-1}{\sqrt{4-2\sqrt{2}}} & \frac{1}{\sqrt{4-2\sqrt{2}}} \\ \frac{-1}{\sqrt{4-2\sqrt{2}}} & \frac{\sqrt{2}-1}{\sqrt{4-2\sqrt{2}}} \end{bmatrix},$$

$$V^{-1} = \begin{bmatrix} v_1 & -v_2 \\ v_2 & v_1 \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{2}-1}{\sqrt{4-2\sqrt{2}}} & \frac{-1}{\sqrt{4-2\sqrt{2}}} \\ \frac{1}{\sqrt{4-2\sqrt{2}}} & \frac{\sqrt{2}-1}{\sqrt{4-2\sqrt{2}}} \end{bmatrix},$$

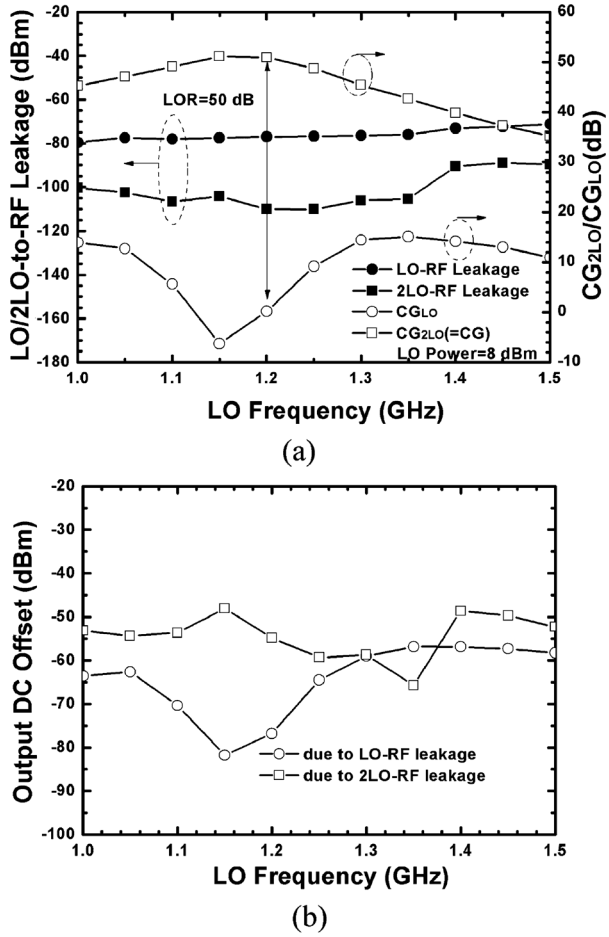

Fig. 15. (a) LO/2LO-to-RF leakage (b) equivalent output dc offset of the proposed 2.4-GHz sub-harmonic receiver while the LO power is 8 dBm.

and

$$E = \begin{bmatrix} E_1 & 0 \\ 0 & E_2 \end{bmatrix} = \begin{bmatrix} 2-\sqrt{2} & 0 \\ 0 & 2+\sqrt{2} \end{bmatrix}.$$

Thus,

$$\begin{aligned} \begin{bmatrix} a_{n+1} \\ b_{n+1} \end{bmatrix} &= X^n \begin{bmatrix} a_1 \\ b_1 \end{bmatrix} \\ &= \begin{bmatrix} v_1 & v_2 \\ -v_2 & v_1 \end{bmatrix} \begin{bmatrix} E_1^n & 0 \\ 0 & E_2^n \end{bmatrix} \begin{bmatrix} v_1 & -v_2 \\ v_2 & v_1 \end{bmatrix} \begin{bmatrix} a_1 \\ b_1 \end{bmatrix} \\ &= E_2^n \begin{bmatrix} (K^n v_1^2 + v_2^2) & (1-K^n) v_1 v_2 \\ (1-K^n) v_1 v_2 & (K^n v_2^2 + v_1^2) \end{bmatrix} \begin{bmatrix} a_1 \\ b_1 \end{bmatrix} \end{aligned} \tag{A2}$$

where $K = (2-\sqrt{2})/(2+\sqrt{2}) = 3 - 2\sqrt{2} < 1$.

When n reaches infinity,

$$\frac{b_\infty}{a_\infty} = \lim_{n\to\infty} \left[\frac{b_{n+1}}{a_{n+1}}\right] = \frac{v_1 v_2 a_1 + v_1^2 b_1}{v_2^2 a_1 + v_1 v_2 b_1} = \frac{v_1}{v_2} = \sqrt{2} - 1. \tag{A3}$$

Consequently, at the $2n_{\mathrm{th}}$ stage, $\mathrm{AD} = 1$ remains but

$$\begin{aligned} \mathrm{PE}_\infty &= \arctan \left| \frac{a_\infty^2 - b_\infty^2 - 2a_\infty b_\infty}{a_\infty^2 - b_\infty^2 + 2a_\infty b_\infty} \right| \\ &= \arctan \left| \frac{a_\infty^2 - (3-2\sqrt{2})a_\infty^2 - 2(\sqrt{2}-1)a_\infty^2}{a_\infty^2 - (3-2\sqrt{2})a_\infty^2 + 2(\sqrt{2}-1)a_\infty^2} \right| = 0. \end{aligned} \tag{A4}$$

TABLE I
PERFORMANCE COMPARISONS OF SUB-HARMONIC DIRECT-CONVERSION RECEIVERS

Reference	[7]	[10]	[23]	[9]	This Work
Topology (**A**:Active; **P**: Passive) (I) quadrature RF and LO (II) differential RF octet-phase LO	**A** Stacked-LO (II)	**A** Top-LO (II)	**P** Parallel Stacked-LO (No Q-path output)	**A** Top-LO (I)	**A** (Top-LO w/ BJT core) (II)
RF Frequency (GHz)	2	2	2.2	5-6	2.4
Conversion Gain (dB) LG=low gain mode	19.2	20 (1 MΩ load)	4.5	26.2	51(1 MΩ load) 31 @LG
LO Power (dBm)	>12[a]	3[a]	−18[a]	15.5	8
Noise Figure (dB)	7.8	8.5	11	7.2/5.2[b]	3
Flicker Noise Corner (kHz)	N/R	100	100	3000	<30
IIP_3 (dBm)	−3	4 (50 Ω load)	0	−12.5	−30 (1 MΩ load) −10 @ LG
IIP_2 (dBm)	35	41 (50 Ω load)	35	N/R	25 (1 MΩ load) 38 @ LG
DC offset (mV)	N/R	9	0.7	0.002	0.44
Supply Voltage (V)	3.3	1.8	1.2	1	1.8
Power Dissipation (mW) (excluding LO generator)	18.5	13.32 (LO octet-phase generator:10.8)	7.2 (LO buffer:5.5)	45.5	9
Technology	0.5μm SiGe HBT	0.18μm CMOS	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS

[a] LO buffer is employed
[b] After inductively coupled plasma (ICP) post process

TABLE II
PERFORMANCE COMPARISONS OF 2.4-GHZ LOW-POWER RECEIVERS

Reference	[1]	[2]	[3]	[22]	[25]	[26]	This Work
Topology (A: Active; P: Passive)	**P** DCR	**P** DCR	**A** DCR	**A** DCR	**A**(switch g_m mixer) DCR/Low-IF	Mixer1: **A** (switch g_m mixer) Mixer2: **P** Dual-Conversion Sliding IF	**A** (w/ BJT core) SHM, DCR
RF Frequency (GHz)	2	2.3	2.4	2.5	2.4	2.4	2.4
Conversion Gain (dB) LG=low gain mode	29	35.6	52	43	67	30	51(1 MΩ load) 31 @LG
Noise Figure (dB)	3.9	8.8[a]	24.5	5	16	18	3
Flicker Noise Corner (kHz)	70	N/R	N/R	N/R	N/R	N/R	<30
LO Power (dBm)	N/R	N/R	>−10[b]	−10[b]	N/R	N/R	8
IIP_3 (dBm)	−1	−31	−21	−37	−10.5	−22	−30 (1 MΩ load) −10 @ LG
IIP_2 (dBm)	35	N/R	18	N/R	20.6	N/R	25 (1 MΩ load) 38 @LG
Supply Voltage (V)	1.8	1.8	1.2	1.2	0.6	0.5	1.8
Power Dissipation (mW) (excluding LO generator)	15	9	1.86 (LO buffer: 1.44)	1.4 (LO generator: 1.2)	10 (LO generator: 22.5)	5.2 (LO buffer: 3.3)	9
Technology	0.18-μm CMOS	0.18-μm CMOS	0.13-μm CMOS	0.18-μm CMOS	90-nm CMOS	90-nm CMOS	0.18μm CMOS

[a] SSB NF
[b] LO buffer is employed

Further, at the $(2n+1)_{\text{th}}$ stage, $\text{PE} = 0°$ remains but

$$\text{AD} = \frac{\sqrt{2}a_n}{(a_n + b_n)} = \frac{\sqrt{2}a_n}{a_n + (\sqrt{2}-1)a_n} = 1. \tag{A5}$$

Therefore, perfect octet-phase accuracy can be obtained under any arbitrary initial condition of a_1 and b_1. However, choosing closer a_1 and b_1 results in less necessary stages for a tolerable criterion.

APPENDIX B
DERIVATION OF SWITCHING FUNCTION OF THE TOP-LO/STACKED-LO SUB-HARMONIC MIXERS

The schematic of a BJT-based top-LO SHM is shown in Fig. 5(c). The current relationship is summarized as below while the input/output differential current are $(I_{\text{i1}} - I_{\text{i2}})$ and $(I_{\text{o1}} - I_{\text{o2}})$, respectively.

$$\begin{cases} I_1 = I_S e^{(V_{\text{LO}Ip} - V_{S1})/V_T} + I_S e^{(V_{\text{LO}In} - V_{S1})/V_T} \\ \quad = I_S e^{(V_{CM} - V_{S1})/V_T} \times (e^X + e^{-X}) \\ I_2 = I_S e^{(V_{CM} - V_{S1})/V_T} \times (e^Y + e^{-Y}) \\ I_3 = I_S e^{(V_{CM} - V_{S2})/V_T} \times (e^Y + e^{-Y}) \\ I_4 = I_S e^{(V_{CM} - V_{S2})/V_T} \times (e^X + e^{-X}) \end{cases} \tag{B1}$$

where $X = A\cos\omega_{\text{LO}}t, Y = A\sin\omega_{\text{LO}}t$, $A = V_{\text{LO}}/(2V_T)$ and V_{CM} is the dc bias of the LO base node.

As a result, the current switching function $s_{\mathrm{TOP}}(\mathrm{t})$ can be expressed as

$$\begin{aligned} s_{\mathrm{TOP}}(t) &= \frac{I_{o1}-I_{o2}}{I_{i1}-I_{i2}} = \frac{I_1+I_3-I_2-I_4}{I_1+I_2-I_3-I_4} \\ &= \frac{\cosh(X)-\cosh(Y)}{\cosh(X)+\cosh(Y)} \\ &= \tanh\left(\frac{X-Y}{2}\right) \times \tanh\left(\frac{X+Y}{2}\right). \end{aligned} \quad \text{(B2)}$$

On the other hand, a stacked-LO SHM consisting of two Gilbert mixing cells in cascode configuration with differential quadrature phase inputs is shown in Fig. 5(a). The switching function of a Gilbert cell is $\tanh(X)$ if the LO input voltage is $V_{\mathrm{LO}}\cos\omega_{\mathrm{LO}}\mathrm{t}$ [27]. Thus, the stacked-LO SHM has a switching function of

$$\begin{aligned} s_{\mathrm{STACKED}}(t) &= \tanh(X) \times \tanh(Y) \\ &= \tanh(A\cos(\omega_{\mathrm{LO}}t)) \\ &\quad \times \tanh(A(\sin(\omega_{\mathrm{LO}}t)). \end{aligned} \quad \text{(B3)}$$

When compared to the switching function of a stacked-LO SHM, an additional 3-dB LO power is required for a top-LO SHM to reach the same gain level, because

$$\begin{cases} (X+Y)/2 = A\cos(\omega_{\mathrm{LO}}t-\pi/4)/\sqrt{2} \\ (X-Y)/2 = A\sin(\omega_{\mathrm{LO}}t-\pi/4)/\sqrt{2} \end{cases}, \quad \text{(B4)}$$

and the common phase delay $\pi/4$ has no influence on the conversion gain. In addition, the mathematical expression fits the simulated results shown in Fig. 5(d) well.

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