Triple Loop Modulation (TLM) for High Reliability and Efficiency in a Power Factor Correction (PFC) System

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***Abstract*—The proposed triple loop modulation (TLM) can ensure reliability of the power factor correction (PFC) system due to the improvement of transient response. In conventional design, low bandwidth of less than 20 Hz that rejects ac source of 60/120 Hz coupling deteriorates system reliability in case of output load variation. Contrarily, the proposed TLM can automatically adjust bandwidth to rapidly increase or decrease inductor current to shorten transient response time. Besides, in the steady state, system stability can be guaranteed by low-frequency compensation pole without being affected by the TLM. The test circuit fabricated in a VIS 500 V UHV laterally diffused metal–oxide–semiconductor transistor process demonstrates that the highly integrated PFC controller with the proposed TLM has high power factor of 99%, high efficiency of 95%, and high power driving capability of about 90 W. The improvement in transient response is twofold faster than in conventional PFC design with output load variation from 90 to 20 W and vice versa.**

***Index Terms*—Fast transient response, power factor correction (PFC), triple loop modulation (TLM).**

I. Introduction

DUE to the lack of energy, high reliability and efficiency become the focus of current green power systems. Power factor correction (PFC) can shape the input current of offline power supplies in phase with the input ac voltage in order to increase the real power available from the ac source [1]. Generally speaking, active PFC with constant on-time control technique is used to improve the power factor (PF) value to about 0.99 [2]–[12]. The conventional PFC architecture uses a constant on-time control technique in boundary conduction mode (BCM), as shown in Fig. 1(a). In the conventional constant on-time control architecture, the error amplifier (EA) is used to set up the output power level through the error signal $V_{\rm EAO}$. The comparator compares the saw-tooth signal with the $V_{\rm EAO}$ to determine the on-time period. On the other hand, the off-time period is determined by the detection of the zero inductor current. Thus, the off time varies with the line voltage level and the output power. It results in the switching frequency of the constant on-time control that is variable. There are many different variable switching frequency control methods as shown in Table I. These control methods are usually used to improve PF and total harmonic distortion (THD) but the transient response time is not improved obviously.

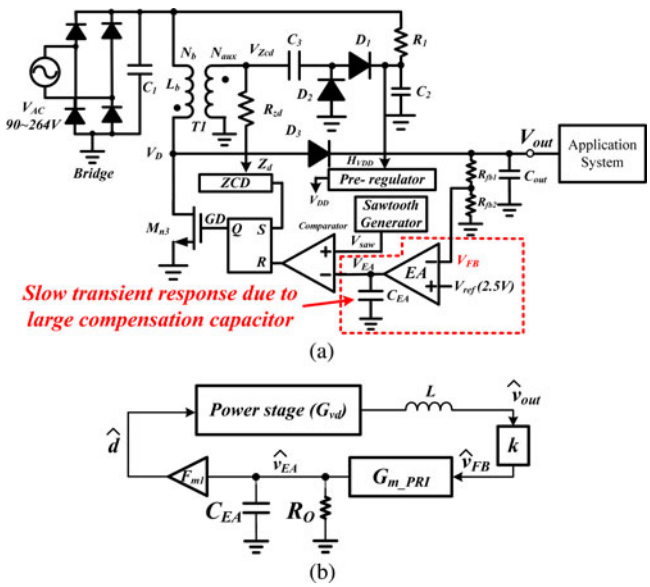

Fig. 1. (a) Conventional PFC architecture uses constant on-time control technique in BCM. (b) Small-signal analysis reveals low bandwidth contributed by the large compensation capacitor $C_{\rm EA}$.

Here, system bandwidth of the active PFC controller needs to be low enough to filter out noise from the ac line revealed by small-signal analysis, as shown in Fig. 1(b). Therefore, a large compensation capacitor $C_{\rm EA}$ is connected to the output EA [13]–[16]. Resulting large over-/under-voltage may seriously affect the reliability of the next stage or the application system (see Fig. 2). The overshoot problem will cause two serious issues throughout the duration of the next IC stage: 1) hot carrier injection and 2) high voltage stress on core gate oxide. Hot carrier injection will be affected by drain-to-source voltage, shortening lifetime and affecting external power MOSFET. Higher output voltage will increase response internal power voltage, while higher power supply voltage will shorten the lifetime of core gate oxide. As shown in (1), lifetime is inversely related to power supply voltage, which is provided by the output of the

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TABLE I
COMPARISON TABLE WITH DIFFERENT VARIABLE SWITCHING FREQUENCY CONTROL

	This work	[13]	[14]
Input inductor	400 μH	600 μH	80 μH/180μH
Output Capacitor	68 μF	100 μF	220 μF
Input line voltage	90-264 V_{ac}	265 V_{ac}	90-264 V_{ac}
Output voltage	400 V	400 V	400 V
Control mechanism	Constant-on time With TLM	Variable on-time	Proposed variable-duty-cycle control
THD (minimum)	10%	6.1%	N/A
Power factor	0.994	N/A	~0.999
Improve transient response time	Yes	N/A	N/A

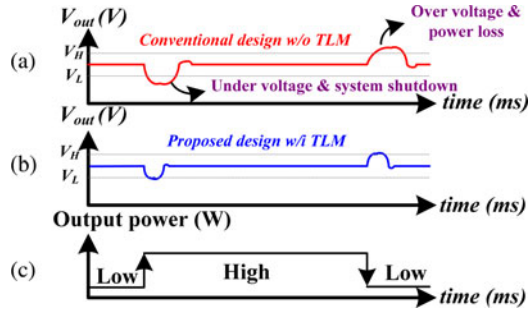

Fig. 2. (a) Large transient over-/under-voltage reduces system reliability. (b) TLM prevents over-/under-voltage. (c) Output power variation.

PFC system

$$\text{Time to failure } \propto (V_{CC})^{-n} * \exp\left(E_a/(KT)\right) * (A_{\rm OX})^{-1/\beta} \quad (1)$$

where $A_{\rm OX}$ is the total gate oxide area on silicon, T is the absolute junction temperature, V_{CC} is the gate voltage, n is the power law exponent for core thin gate oxide, E_a is the thermal activation energy, k is Boltzmann's constant, and b is Weibull shape factor.

On the other hand, the undershoot problem may cause shutdown and deteriorate system stability of the next stage. Therefore, the proposed PFC architecture needs to carefully consider the reliability and the transient response time in order to improve lifetime of electronics. To improve reliability and transient response time, the PFC with the triple loop modulation (TLM) technique is proposed. The comparison waveform of modified ripple is shown in Fig. 2. The output ripple will be detected to trigger the TLM technique. With the hysteresis window defined by the lower bond voltage V_L and the upper bond voltage V_H, the TLM technique will restrain output ripple in the design specifications. Once output ripple is restrained, extension of reliability follows naturally. The TLM technique not only prolongs reliability, but also promotes stability in the steady state. The operating frequency needs to be larger than 35 kHz for avoiding audio noise. Owing to the usage of electromagnetic interference (EMI) filter, the upper limit of the operating frequency is around 217 kHz at 220 $V_{\rm ac}$.

The organization of this paper is as follows. Section II introduces the circuit implementation of the TLM technique. The small-signal analysis of the proposed PFC technique with the TLM is shown in Section III. Section IV introduces the design of the components for the controller. Experimental results are presented in Section V. Finally, conclusions are made in Section VI.

II. CIRCUIT IMPLEMENTATION

As shown in Fig. 1(b), the EA is compensated by a very low frequency pole, which is generated by a large compensation capacitor $C_{\rm EA}$. The $C_{\rm EA}$ can remove noise from the ac power line but may deteriorate the transient response in case of large output load step variation. To facilitate immediate reaction to load transient response, the TLM was introduced and triggered during the load transient period in order to rapidly settle the output of EA even under low bandwidth. Fig. 3 shows the proposed PFC architecture with the TLM, which involves two additional feedbacks from the output node $V_{\rm out}$.

The flow diagram of the TLM technique is shown in Fig. 4. Normally, the steady-state operation controlled by the primary modulator is similar to that of original PFC controller. The allowable output variation is in the range of 10% of the nominal output voltage, 400 V. That is to say, the output voltage is limited within the range from 360 to 440 V. Thus, V_H and V_L are selected as 2.75 and 2.25 V, respectively, because the feedback factor is 2.5 V/400 V, which is determined by the ratio of feedback resistors. When the output power has a light-to-heavy load step and simultaneously the feedback voltage $V_{\rm FB}$ is smaller than the threshold voltage V_L, the secondary modulation is triggered to help transient response. That is, the slowly increased $V_{\rm EA}$ by the primary modulator will be modulated by the secondary modulator to speed up the response time, and thus, the undershoot voltage can be reduced. Once the $V_{\rm FB}$ voltage is pulled back to be larger than the V_L, the system will automatically switch to the primary modulation.

On the other hand, when the output power has a heavy-to-light load step and the feedback voltage $V_{\rm FB}$ is larger than the threshold voltage V_H at the same time, the third modulation starts to help transient response. The third modulator can rapidly pull low the $V_{\rm EAO}$ not the $V_{\rm EA}$ so as to decrease the overshoot voltage without decreasing the system stability since the $V_{\rm EA}$ is still controlled by the primary modulator. The TLM circuit can effectively reduce overshoot and undershoot voltages to decrease power loss and increase system reliability. That is, in case of load variation, the variation of the $V_{\rm out}$ is kept within the allowable transient voltage variation range, as depicted in Fig. 2.

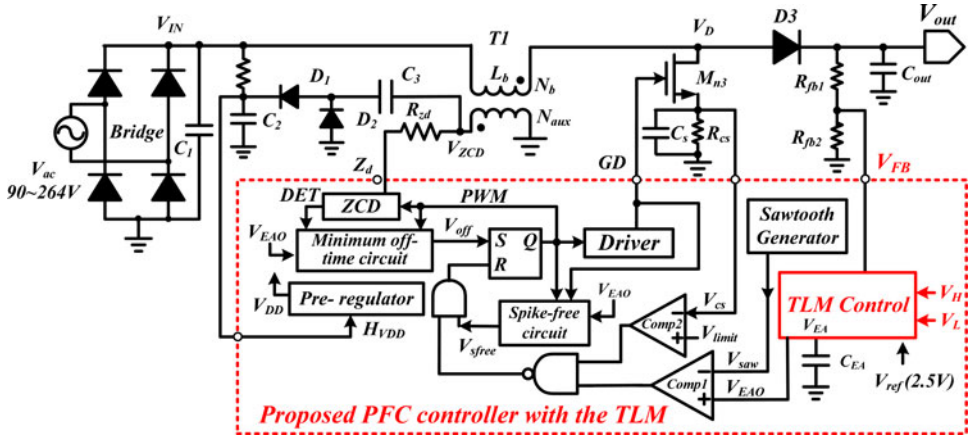

Fig. 3. Proposed PFC architecture with the TLM.

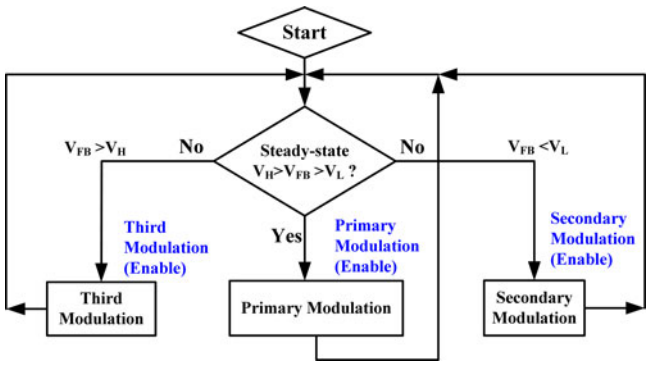

Fig. 4. Flowchart of the TLM system.

A. Primary Modulator

As shown in Fig. 5(a), the primary loop modulation circuit contains the EA, which is shown in Fig. 5(b). The differential inputs of the EA are composed of two high-voltage (HV) devices M_{p5} and M_{p6} to avoid a high voltage stress that may damage the input devices from the feedback node. The EA works as a transconductance amplifier to convert the voltage difference between $V_{\rm ref}$ and $V_{\rm FB}$ to a difference current with an output conductance of 120 μA/V. Thus, the bandwidth will be around 20 Hz determined by the compensation capacitor of 1 μF. Meanwhile, the inverting input of the EA is connected to the $V_{\rm FB}$. The EA's output is compensated by a large compensation capacitor $C_{\rm EA}$ and filtered by a unity-gain buffer OP2, which is composed of a two-stage operational amplifier, to yield the signal $V_{\rm EAO}$. The value of $V_{\rm EAO}$ can determine on-time value through the peak current control method. The on-time value is nearly constant to guarantee that the PF is sufficiently high to satisfy the requirements of the European Norm EN61000-3-2. In case of light-to-heavy load changes, rapid increase at the $V_{\rm EA}$ can effectively improve the transient response due to the instant extension of bandwidth. On the other hand, rapid decrease at the $V_{\rm EA}$ will cause the ringing effect as shown in Fig. 5(c) when the load changes from heavy to light or the system in the startup

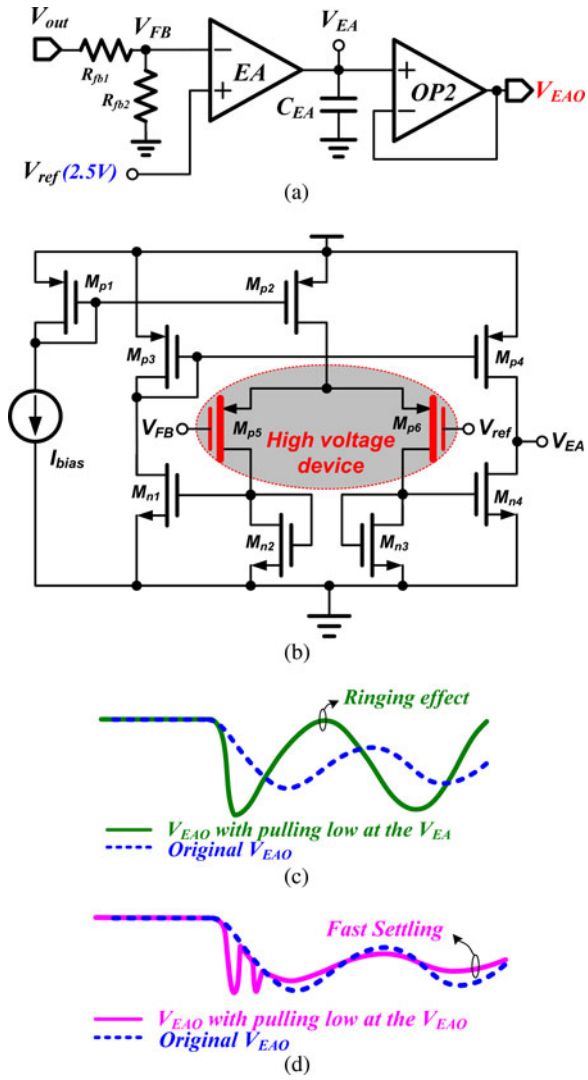

Fig. 5. (a) Primary modulator. (b) Schematic of the EA circuit (c) Ringing effect due to the fast pulling down at the $V_{\rm EA}$ when load changes from heavy to light. (d) Fast settling owing to the adequate pulling down at the $V_{\rm EAO}$ when load changes from heavy to light.

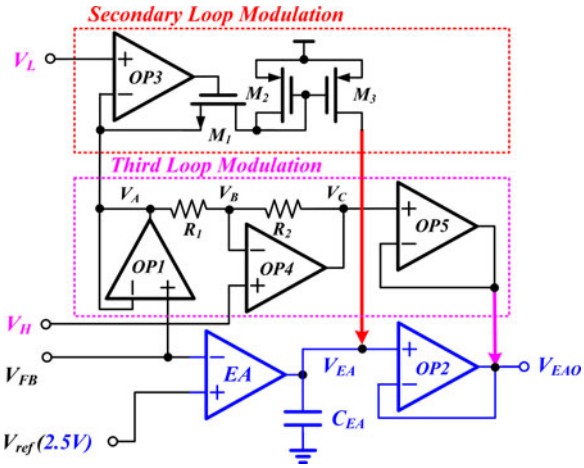

Fig. 6. TLM technique comprises of secondary and third modulators to improve transient response for high reliability.

period. Therefore, the suitable control node locates at the $V_{\rm EAO}$, which is the buffer output of the EA. As shown in Fig. 5(d), the system can be smoothly and rapidly settled down to its regulated voltage.

B. Secondary and Third Modulators

TLM (see Fig. 6) can improve transient response and reduce over-/under-shoot voltage due to the two additional insertion loops. Bandwidth will be instantly increased for a while to reduce transient response time.

In case of a large increasing load step, the scaled signal $V_{\rm FB}$, which is feedback from the output, is filtered by a unity-gain buffer OP1 to remove large switching noise. The circuit diagram of the OP1 is depicted in Fig. 7(a). The differential input pairs M_{p4} and M_{p5} are HV N-MOSFET devices to endure a 30 V high voltage across its gate–source voltage $V_{\rm gs}$. The decrease in $V_{\rm FB}$ with a large step will reveal output power. $V_{\rm FB}$ is compared with V_L, which defines allowable undershoot voltage at the output, to determine current injection to $V_{\rm EA}$, which is connected to a large compensation capacitor. In other words, there is an extra current to speed up the response time at the $V_{\rm EA}$. As a result, bandwidth will be extended to improve transient response and decrease undershoot voltage. Once $V_{\rm FB}$ is higher than V_L, current injection will cease. Meanwhile, the system bandwidth is recovered to less than 20 Hz, as defined by the primary modulator.

On the other hand, if output power is suddenly decreased, the low bandwidth in conventional design does not have the ability to suppress overshoot voltage. Thus, the third modulation loop is inserted to pull down the value of $V_{\rm EAO}$ through a unity-gain buffer OP5. The circuit of amplifier OP5, a two-stage op-amp and as shown in Fig. 7(b), only provides current sinking capability to rapidly pull down the voltage level at the $V_{\rm EAO}$. Here, the current sinking capability is determined by the transistor M_{n3}.

Lower values of $V_{\rm EAO}$ result in smaller on-time values to effectively clamp input power, thereby suppressing overshoot voltage. The third modulator will release domination of $V_{\rm EAO}$ due to suppression of output voltage although $V_{\rm EA}$ value has not been settled because of low bandwidth. Thus, the controller is reverted to heavy-to-light conditions and the third modulation loop is triggered again. After several switching cycles, $V_{\rm EA}$ will be successfully settled and the third modulator will no longer be activated. In other words, the control authority is changed between the primary modulator and the third modulator for small overshoot voltage during the recovery time of the output voltage. Importantly, the third modulator is not connected to $V_{\rm EA}$, since the instant pull-down will trigger the ringing effect as shown in Fig. 5(c), which depicts that the system experiences oscillation between the secondary and the third modulators. The third modulator that connects to the $V_{\rm EAO}$ can effectively improve the stability. Finally, the third modulator is turned off and control authority is returned to the primary modulator in the steady state.

C. On-Time and Off-Time Controlling Circuits

The on-time period is determined by the comparison of the saw-tooth signal $V_{\rm saw}$ and the $V_{\rm EAO}$. Fig. 8 shows the saw-tooth generator circuit, which uses a constant current to charge the capacitor to get a ramp-up signal. Besides, the max-on-time limiter is also implemented to limit the maximum on-time value for avoiding the overloading and audio noise through the comparison of a higher voltage of 3 V.

On the other hand, the off-time period is determined by the zero current detection (ZCD) circuit in Fig. 9. In other words, the ZCD circuit decides the begging of the next switching. The Z_d pin is used to detect the zero inductor current through the auxiliary winding in the BCM operation. The signal $V_{\rm ZCD}$ varies within the expression shown as

$$-\left(\frac{N_{\rm aux}}{N_b}\right)V_{\rm IN} \le V_{\rm ZCD} \le \left(\frac{N_{\rm aux}}{N_b}\right)\cdot\left(V_{\rm out}-V_{\rm IN}\right). \quad (2)$$

A negative voltage is not allowable for the integrated circuit fabricated in a standard CMOS process due to the latch-up problem. Thus, the ZCD circuit can protect the PFC controller from being damaged by latch-up caused by the negative voltage. If the voltage at the Z_d pin is gradually smaller than zero, the transistor M_2 will form a negative feedback to clamp the voltage still higher than 0 V. The operational amplifier OP1 can force the $V_{\rm ZR1}$ to be approximately equal to the $V_{\rm REF2}$. As a result, the voltage of the $V_{\rm ZR1}$ is expressed as

$$V_{\rm ZR1} = V_{\rm REF2} + \left(V_{\rm GS4} - V_{\rm GS3}\right). \quad (3)$$

When the pulsewidth modulation (PWM) signal is equal to zero, the stored energy in the inductor starts to release to the output. The $V_{\rm ZCD}$ starts to decrease since the energy in the inductor dries out. Once the signal Z_d voltage is lower than $V_{\rm REF}$, the GD signal will be set high, again. The power MOSFET will be turned ON to trigger one new switching cycle.

As we know, the switching noise will degrade the stability. The spike-free circuit in Fig. 10 is utilized to avoid high switching noise when the power MOSFET is turned ON. Simultaneously, the current limiting mechanism will be disabled during the operation of the spike-free circuit in order not to shut

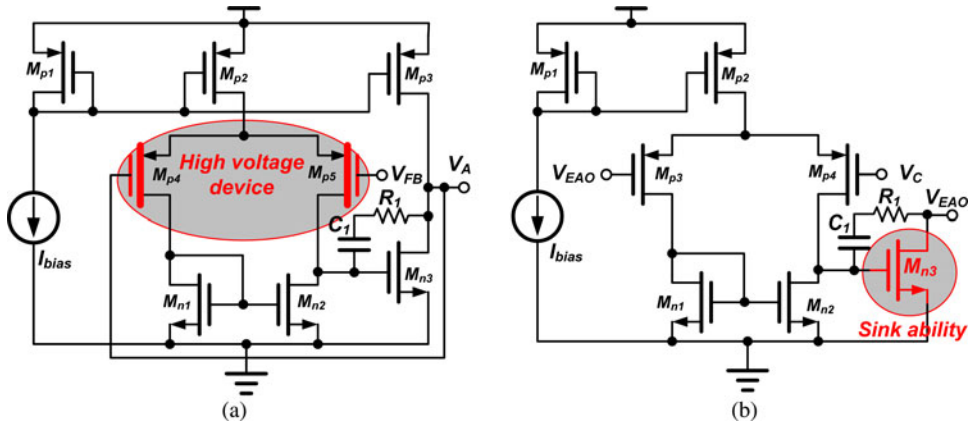

Fig. 7. Operational amplifiers. (a) OP1 circuit is a two-stage architecture with two HV differential input devices. (b) OP5 circuit simply provides the current sinking capability.

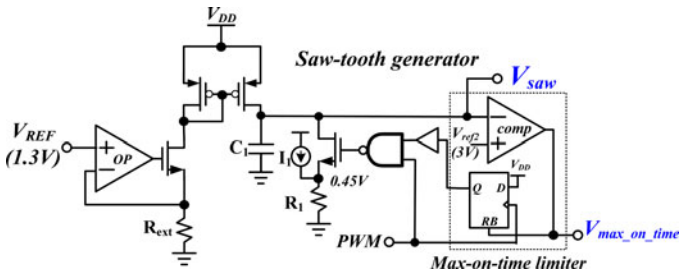

Fig. 8. Schematic of the saw-tooth circuit.

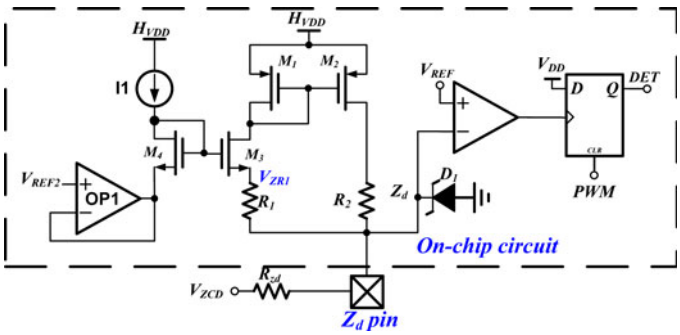

Fig. 9. Schematic of the ZCD circuit.

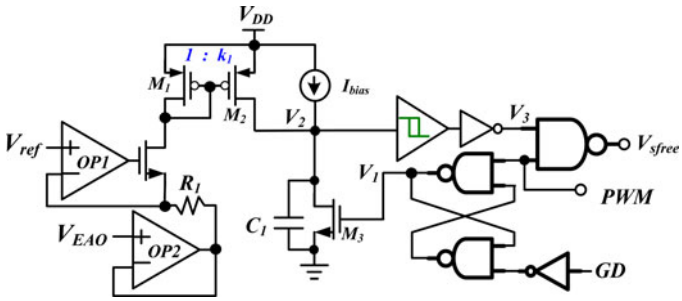

Fig. 10. Schematic of the spike-free circuit.

down the overall operation. The spike-free circuit gets rid of the switching noise without any external low-pass filters. Besides, the spike-free time varies according to the loading condition, indicated by the signal $V_{\rm EAO}$ in Fig. 3. That is, the voltage

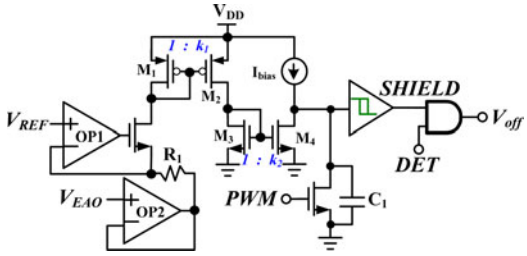

Fig. 11. Schematic of the minimum off-time circuit.

across the resistor R_1 defines the current flowing through the transistor M_3 in Fig. 10. Lower $V_{\rm EAO}$ leads to higher current flowing through M_3.

The power MOSFET can be turned OFF to deliver energy to the output; the minimum off-time circuit is shown in Fig. 11. The minimum off-time also needs to be adjusted according to the loading indication signal $V_{\rm EAO}$, which is generated by the EA in Fig. 3. In Fig. 11, the voltage across the resistor R_1 defines the current flowing through the transistor M_4. Lower $V_{\rm EAO}$ leads to higher current flowing through M_4. As a result, the charging current as expressed in (4) for the capacitor C_1 is drastically decreased to generate a longer minimum off-time

$$I_{\rm C1} = I_{\rm bias} - k_1 \cdot k_2 \cdot \frac{V_{\rm REF} - V_{\rm EAO}}{R_1}. \tag{4}$$

D. Preregulator and Driver

Two circuits in the PFC controllers that need to face high voltage are the preregulator and the driver. The preregulator that supplies internal voltage for the PFC controller is depicted in Fig. 12. The feedback is composed of diode-connected low-voltage (LV) P-type MOSFETs. The HV devices including N-type and P-type can endure a 20 V high voltage across their drain–source voltage. Furthermore, the preregulator is stabilized by an MOSFET capacitance M_{nc1}. Besides, the Zener diodes are used to clamp the maximum supply voltage to protect internal devices from being damaged by high voltage.

The HV driver circuit in Fig. 13 can be used to drive external power MOSFETs for minimizing conduction loss. The driver

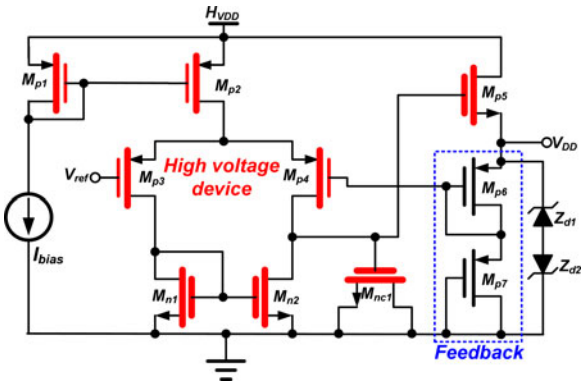

Fig. 12. Schematic of the preregulator circuit.

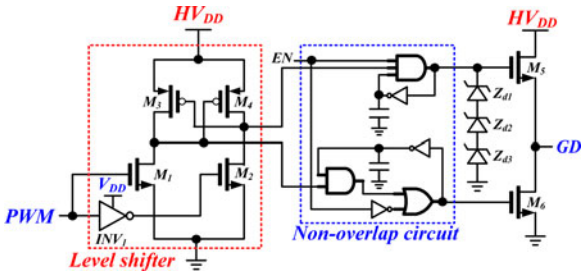

Fig. 13. Schematic of the driver circuit.

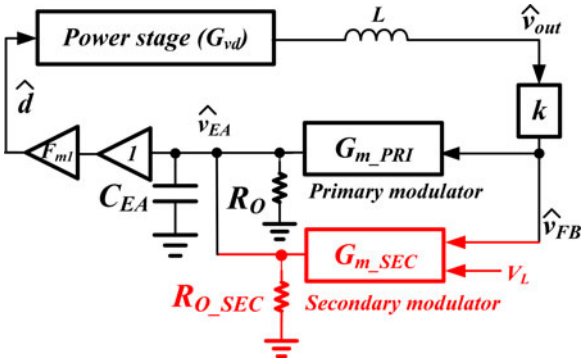

Fig. 14. Small-signal model of the TLM technique when the secondary loop modulation is activated.

circuit is composed of level shifter and nonoverlap circuit. The level shifter, composed of M_1, M_2, M_3, M_4, and INV_1, can boost the internal reference voltage to a high input voltage H_{vdd}. The nonoverlap circuit can avoid the shoot-through current from M_5 to M_6. Besides, the output voltage will be clamped by internal Zener diodes Z_{d1}, Z_{d2}, and Z_{d3}, and the source follower M_5.

III. Small-Signal Analysis of the TLM

These two additional feedbacks can help in the recovery of EA output under different load conditions. Small-signal model of the proposed TLM can be represented as in Figs. 14 and 15 if output load has light-to-heavy and heavy-to-light changes, respectively. The output-to-duty transfer function is formed by the combination of three feedback transfer functions under different load conditions.

The primary modulator resembles conventional design with the characteristic low bandwidth. The secondary modulator can adapt to load variation in order to adjust bandwidth for fast transient response when the output has an instantly increasing power. On the other hand, the third modulator can prevent overshooting of the output in case of rapidly decreasing power.

A. Analysis of Primary Loop Modulation

The primary modulator consists of an EA with a large compensation capacitor C_{EA}, as shown in Fig. 1(b). The transfer function of the primary modulator can be derived as

$$\frac{\hat{v}_{\mathrm{EA}}}{\hat{v}_{\mathrm{FB}}} = -G_{m\_\mathrm{PRI}} R_o \frac{1}{1+\frac{s}{\omega_{P(\mathrm{dominant})}}}$$

$$\text{where} \quad \omega_{P(\mathrm{dominant})} = \frac{1}{R_o C_{\mathrm{EA}}} \tag{5}$$

$$\mathrm{BW} = G_{m\_\mathrm{PRI}} R_o \cdot \frac{1}{R_o C_{\mathrm{EA}}} = \frac{G_{m\_\mathrm{PRI}}}{C_{\mathrm{EA}}}. \tag{6}$$

DC gain is the product of EA's transconductance (G_{m_PRI}) and output resistance R_o. The low-frequency pole $\omega_{P(\mathrm{dominant})}$ produced by the primary modulator significantly decreases bandwidth (BW) as shown in (6) due to the large C_{EA}.

B. Analysis of Secondary Loop Modulation

In case of increasing output power, the TLM will activate the secondary modulator to extend bandwidth if the V_{FB} is lower than the low threshold voltage V_L. In other words, the secondary modulator can avoid undervoltage and get high reliability. As illustrated in Fig. 14, the secondary modulator contributes another transconductance (G_{m_SEC}) so that the transfer function from V_{FB} to V_{EA} can be modified as

$$\frac{\hat{v}_{\mathrm{EA}}}{\hat{v}_{\mathrm{FB}}} = -(G_{m\_\mathrm{PRI}} + G_{m\_\mathrm{SEC}})(R_o \| R_{o\_\mathrm{SEC}}) \cdot \frac{1}{1+\frac{s}{\omega_{P(\mathrm{dominant})}}}$$

$$\text{where} \quad \omega_{P(\mathrm{dominant})} = \frac{1}{(R_o \| R_{o\_\mathrm{SEC}}) C_{\mathrm{EA}}} \tag{7}$$

$$\mathrm{BW} = (G_{m\_\mathrm{PRI}} + G_{m\_\mathrm{SEC}})(R_o \| R_{o\_\mathrm{SEC}}) \cdot \frac{1}{(R_o \| R_{o\_\mathrm{SEC}}) C_{\mathrm{EA}}} = \frac{G_{m\_\mathrm{PRI}} + G_{m\_\mathrm{SEC}}}{C_{\mathrm{EA}}}. \tag{8}$$

Due to the insertion of G_{m_SEC}, the combination of primary modulator and secondary modulator in (7) can enhance the equivalent transconductance from G_{m_PRI} to the sum of G_{m_PRI} and G_{m_SEC}. The equivalent resistance changes from R_o to a parallel resistance R_o in parallel with R_{o_SEC}. The reduced equivalent resistance pushes the dominant pole to higher frequencies. As a result, bandwidth as shown in (8) becomes higher than that in the steady state. Higher bandwidth means transient response can be greatly improved. Fig. 15(a) shows the Bode plot of the primary modulation only. As the load steps from light to heavy, the Bode plot of the secondary modulation is shown in Fig. 15(b). Obviously, the bandwidth is effectively extended and the gain is also improved.

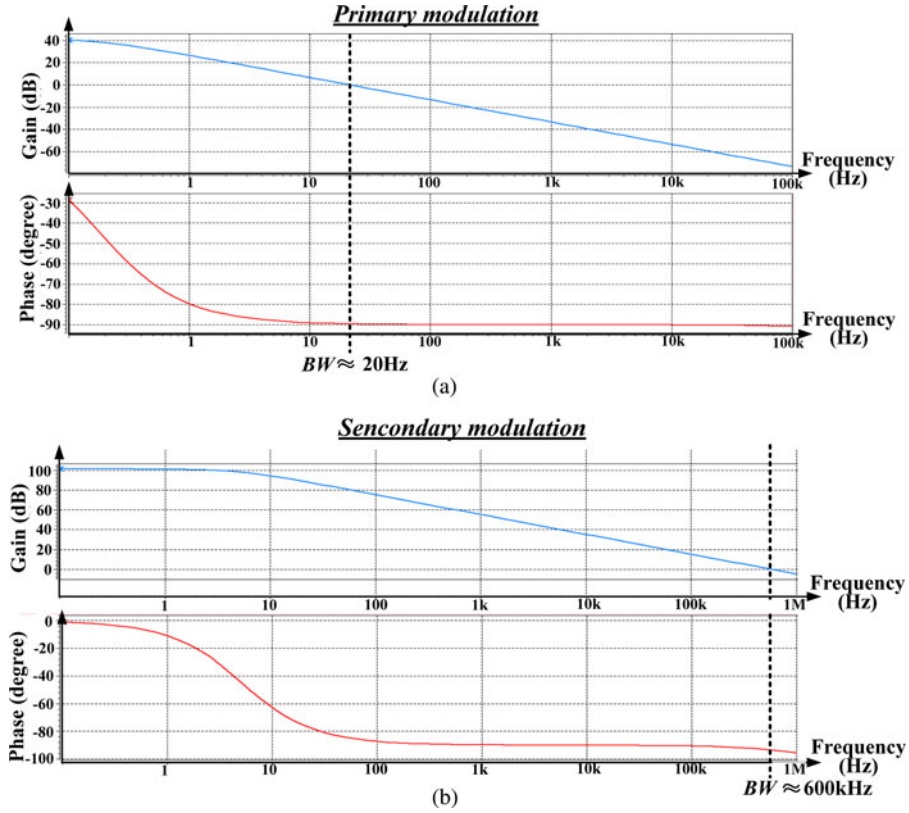

Fig. 15. Bode plot (a) with the primary modulation or (b) with the secondary modulation.

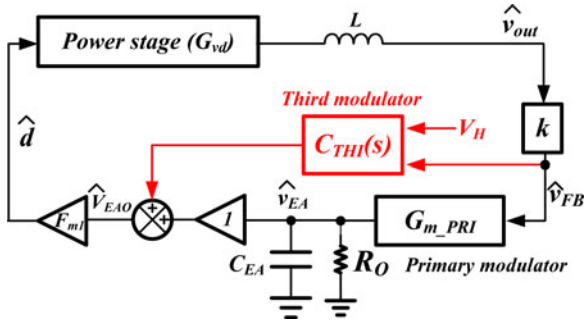

Fig. 16. Small-signal model of the TLM technique when the third loop modulation is activated.

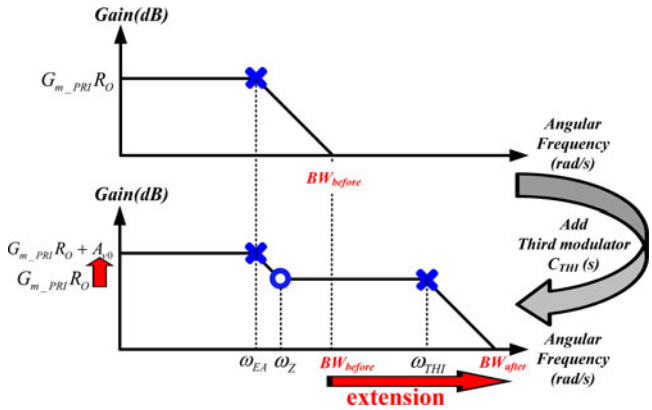

Fig. 17. Bode plot with and without the third modulator.

C. Third Loop Modulation Technique

In case of output power change from heavy to light, the third modulator $C_{\mathrm{THI}}(s)$, as shown in Fig. 16, will be activated once the V_{FB} is higher than the higher threshold voltage V_H. The transfer function is derived as (9). Therefore, the transfer function from V_{FB} to V_{EA} is modified to (10)

$$C_{\mathrm{THI}}(s) = A_{v0} \cdot \frac{1}{1+\frac{s}{\omega_{\mathrm{THI}}}} \tag{9}$$

$$\frac{\hat{v}_{\mathrm{EAO}}}{\hat{v}_{\mathrm{FB}}} = \left((-G_{m\_\mathrm{PRI}}R_O)\cdot\frac{1}{1+\frac{s}{\omega_{\mathrm{EA}}}}\cdot\frac{1}{1+\frac{s}{\omega_{\mathrm{THI}}}}\right)$$

$$+\left(A_{v0}\cdot\frac{1}{1+\frac{s}{\omega_{\mathrm{THI}}}}\right) = \frac{(-G_{m\_\mathrm{PRI}}R_O + A_{v0})\cdot\left(1+\frac{s}{\omega_Z}\right)}{\left(1+\frac{s}{\omega_{\mathrm{EA}}}\right)\cdot\left(1+\frac{s}{\omega_{\mathrm{THI}}}\right)}$$

and $A_{v0} = -\dfrac{R_2}{R_1}; \omega_{\mathrm{EA}} = \dfrac{1}{R_O C_{\mathrm{EA}}}; \omega_{\mathrm{THI}} = \dfrac{1}{R_{\mathrm{EAO}}\cdot C_{\mathrm{EAO}}}$

$$\omega_Z = \left(\frac{G_{m\_\mathrm{PRI}}R_O - A_{v0}}{A_{v0}}\right)\cdot\frac{1}{R_O C_{\mathrm{EA}}}. \tag{10}$$

Two poles and one zero appear in (10). The first pole ω_{EA} composed of R_O and C_{EA} is the low-frequency pole of the primary modulator. The second pole ω_{THI} composed of the equivalent resistance R_{EAO} and capacitor C_{EAO} at the V_{EAO} is a high-frequency pole. The zero ω_Z produced by the parallel path can almost cancel the effect of ω_{EA}, as shown in Fig. 17. The whole system can be seen as a one-pole system with an extended bandwidth

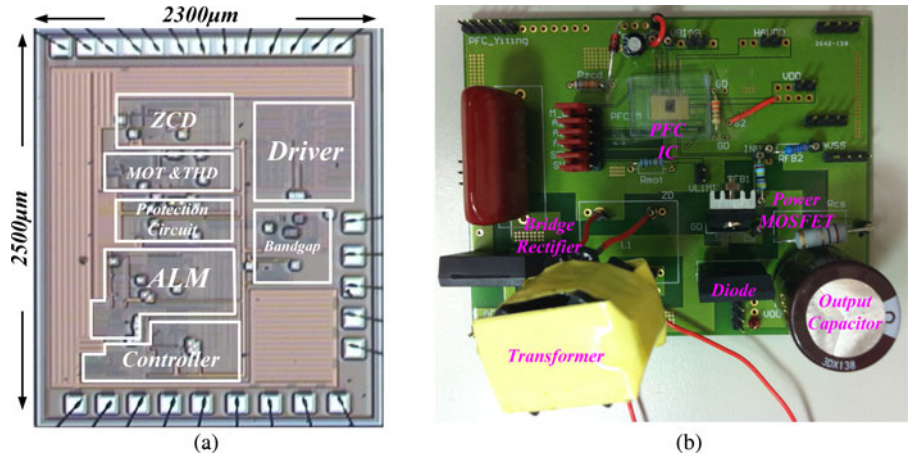

Fig. 18. (a) Chip micrograph. (b) Prototype of the PFC converter with the TLM technique.

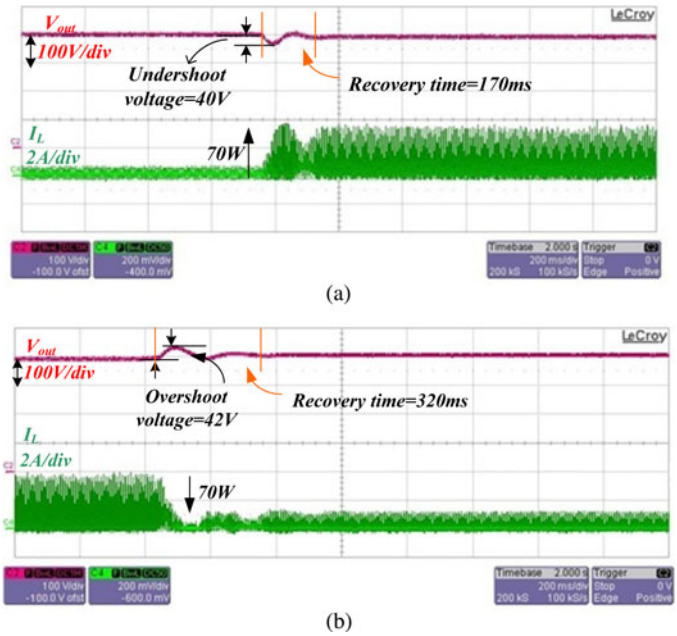

Fig. 19. Waveforms of a conventional PFC controller when (a) output load changes from 20 to 90 W and (b) from 90 to 20 W.

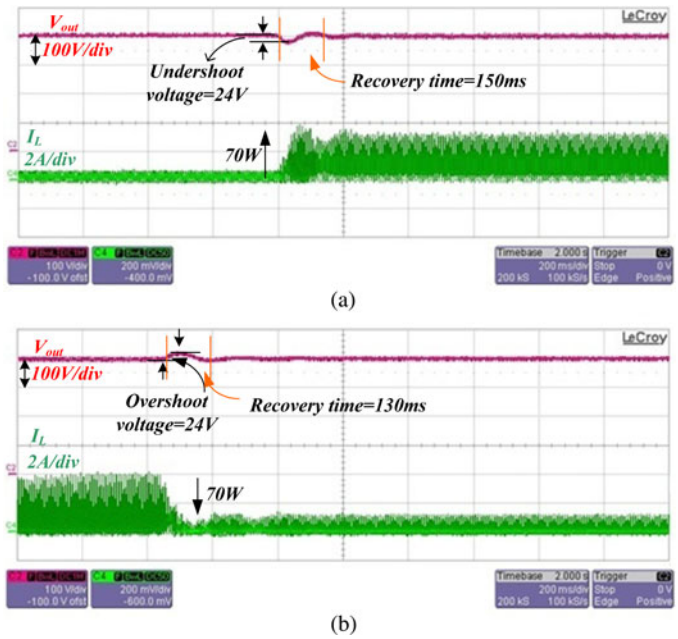

Fig. 20. Waveforms of the proposed PFC with TLM when (a) output load changes from 20 to 90 W and (b) from 90 to 20 W.

A_{v0} is the low-frequency gain of the transfer function of the third modulator, which can provide high-bandwidth response to rapidly pull down the $V_{\rm EAO}$ level through the OP5, as shown in Fig. 6. As $V_{\rm FB}$ exceeds V_H, $C_{\rm THI}$(s) will provide a high-bandwidth path to reflect the variation of output voltage. However, this rapidly pulling-down operation disappears if $V_{\rm FB}$ is lower than V_H, again. In the meanwhile, $C_{\rm THI}$(s) will be bypassed and the system automatically returns to the control of primary modulator. In the steady state, the primary modulator takes over control authority.

IV. Design of the Components for the Controller

Some design values of the components are described in this section to show the design specifications.

A. Design of Inductor Value

To avoid the switching frequency below the audio frequency, the minimum switching frequency $f_{s,\min}$, which happens at maximum ac line input voltage, is needed to be defined as 35 kHz. According to the law of energy conservation, the appropriate inductor value of the proposed PFC controller can be designed by

$$L_b = \frac{V_{\rm ac,peak}^2 \times (V_{\rm out} - V_{\rm AC,peak}) \times \eta}{4 \times P_{\rm out} \times V_{\rm out} \times f_{s,\min}} \tag{11}$$

where $V_{\rm ac,peak}$ is the peak value of the input ac voltage, $P_{\rm out}$ is the output power, and η is the conversion efficiency.

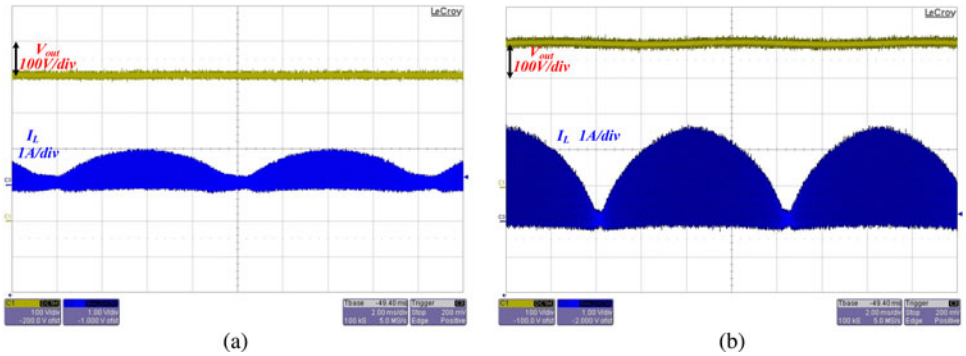

Fig. 21. Waveforms in the steady state when the output loads are (a) 20 W and (b) 90 W, respectively.

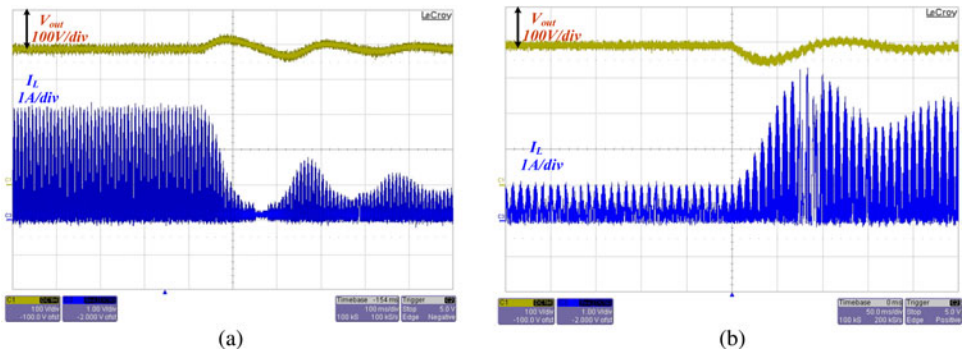

Fig. 22. Zoom-in waveforms of the conventional PFC controller when the output load step changes from 90 to 20 W in (a) and vice versa in (b).

B. Design of Primary Winding

The peak inductor current $I_{L,\text{peak}}$ may affect the primary winding design. Thus, according to Faraday's law, the turns of primary winding can be obtained by

$$N_b = \frac{L_b \times I_{L,\text{peak}}}{B_{\max} \times A_e} \text{ where } I_{L,\text{peak}} = 2\sqrt{2}\frac{P_{\text{out}}}{V_{\text{AC,rms}} \times \eta} \quad (12)$$

where A_e is the effective area of the core section and $B_{\max}$ is the saturation magnetic flux density.

C. Design of Auxiliary Winding

The ZCD needs to sense the voltage information of the auxiliary winding. When Z_d is lower than the threshold voltage in the ZCD circuit, the signal PWM is set high again to initiate a new switching cycle. Nevertheless, there is a prerequisite. Z_d must exceed V_{REF} to ensure the ZCD function when the power MOSFET is turned OFF. Therefore, the turns of auxiliary winding can be design by

$$N_{\text{aux}} = \frac{K_{\text{safe}} \times V_{\text{REF}}}{V_{\text{out}} - \sqrt{2}V_{\text{AC,rms(max)}}} \times N_b \quad (13)$$

where K_{safe} is a constant to ensure that the system contains a safe operation margin.

D. Design of Output Capacitor

The output capacitor C_{out} is used to guarantee the output voltage well-regulated voltage for the next stage. C_{out} is determined by the requirement of sufficient hold-up time t_{hold}, which is the measured time from the general output voltage to the minimum operating voltage of following stage. The output capacitor can be derived as

$$C_{\text{out}} = \frac{2 \times P_{\text{out}} \times t_{\text{hold}}}{(V_{\text{out}}^2 - V_{\text{out,min}}^2)}. \quad (14)$$

TABLE II
DESIGN SPECIFICATIONS

Technology	VIS 0.5μm 500V LDMOS
Die area (with test pads)	2500 μm × 2300 μm
Ac input voltage range V_{ac}	90~264Vac
Output voltage (V_{OUT})	400V
Minimum Switching frequency (f_{SW})	>35 KHz
Output power	90 W
Primary inductor (L_b)	400μH
Primary winding turns (N_b)	58T
Auxiliary winding turns (N_{aux})	5T
Output capacitor (C_{out})	68μF/450V
Compensation capacitor (C_c)	1μF
Output ripple (ΔV_{out})	9.6V
Controller voltage	5V&20V

V. EXPERIMENT RESULTS

The PFC controller with the TLM control technique was fabricated in the VIS 0.5 μm 500 V laterally diffused metal–oxide–semiconductor transistor (LDMOS) process. The chip micrograph and the prototype are shown in Fig. 18(a) and (b), respectively. The design specifications are shown in Table II. The operating voltages of the controller and the driver are 5 and 20 V, respectively. The off-chip input transformer and the output

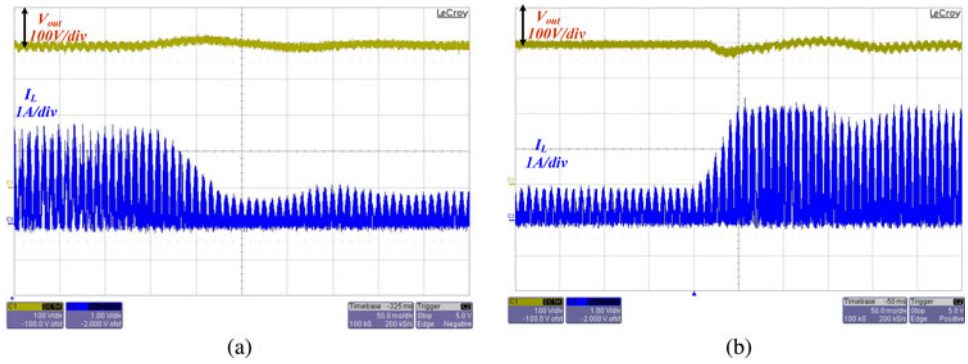

Fig. 23. Zoom-in waveforms of the proposed PFC controller with the TLM technique when the output load step changes from 90 to 20 W in (a) and vice versa in (b).

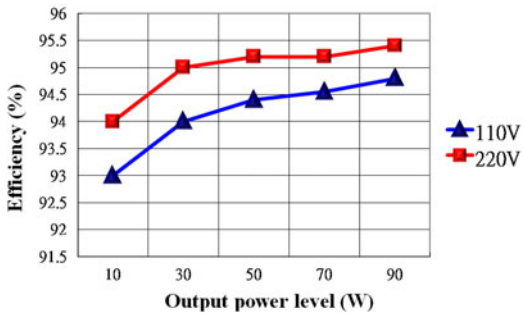

Fig. 24. Measured efficiency results at $V_{\rm ac} = 110$ V and $V_{\rm ac} = 220$ V.

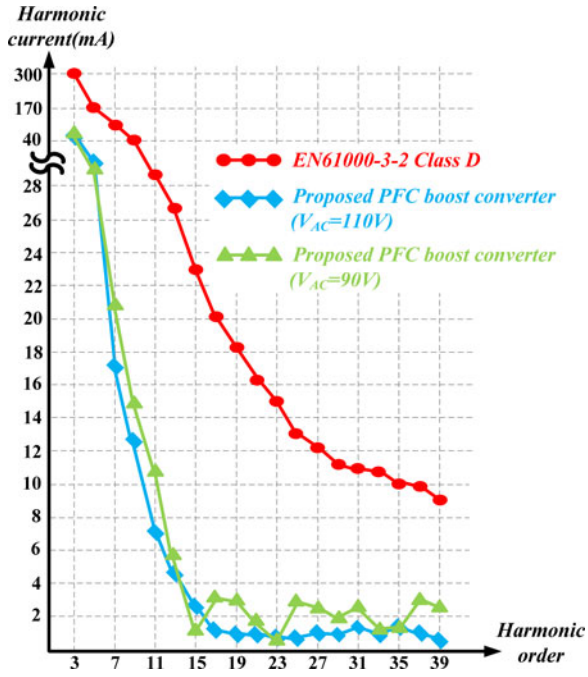

Fig. 25. Spectrum of the input current.

cap are 400 μH and 68 μF, respectively. Output voltage of the PFC controller is 400 V for the next-stage PWM converter.

Input ac voltage is 90 $V_{\rm ac}$. Experimental results of conventional design show that load power consumption changes from 20 to 90 W [see Fig. 19(a)] or vice versa [see Fig. 19(b)]. Overshoot and undershoot voltages are 42 and 40 V, respectively. Recovery times are 320 and 170 ms when load current changes from heavy to light and vice versa. Bandwidth is limited by the large compensation capacitor, so that low-bandwidth transient response of conventional design cannot be sped up.

Fig. 20 illustrates the experimental waveforms of the proposed PFC controller with the TLM. Overshoot and undershoot voltages are kept smaller than 24 V. Recovery times are 150 and 130 ms when load changes from heavy to light and vice versa. Transient response in the proposed PFC controller with the TLM is twofold faster than that of conventional design when output power is changed from heavy to light or vice versa. The improved overshoot and undershoot voltages can effectively enhance the reliability of the power system. Fig. 21(a) and (b) shows the measurement results in the steady state when the load changes from 20 to 90 W and vice versa, respectively. Furthermore, Figs. 22 and 23 show the zoom-in transient waveforms without and with the TLM technique, respectively.

Fig. 24 shows the measured efficiency with the proposed TLM at $V_{\rm ac} = 110$ V and $V_{\rm ac} = 220$ V. The output power varies from 10 to 90 W. As the input voltage is equal to 220 V, the input current is smaller than that with the input voltage of 110 V. Thus, the conduction loss can be decreased so that the efficiency can be increased effectively. The efficiency still can be kept larger than 93% at output power of 10 W without being affected by the power consumption of the TLM since the TLM only consumes 2.65 mW. Besides, Fig. 25 illustrates the spectrum of the input current, which fits the requirements of EN61000-3-2 Class D. The comparison with the prior arts is shown in Table III. The TLM technique can have fast transient response and low undershoot/overshoot voltage. Simultaneously, high PF and low THD also are guaranteed because the TLM only works during the duration of load variation. Furthermore, the operating frequency needs to be larger than 35 kHz to avoid audio noise. Based on the EMI filter, the upper limit of the operating frequency is around 217 kHz at 220 $V_{\rm ac}$. Moreover, the input ac current $I_{\rm ac}$ as shown in Fig. 26 is shaped to be a sinusoidal waveform and in-phase with the input ac voltage $V_{\rm ac}$. Thus, PF is improved by the proposed PFC controller.

TABLE III
COMPARISON OF THE PROPOSED METHOD AND THE PRIOR ARTS

	This work	[17]	[18]	[19]	[20]
Input inductor (μH)	400	227	N/A	200	400
Output Capacitor	68 μF	235 μF	300 μF	440 μF	470 μF
Input line voltage	90-264 V_{ac}	120 V_{ac}	85-267 V_{ac}	106 V_{ac}	110 V_{ac}
Output voltage	400 V	380 V	420 V	215 V	200 V
Switching frequency	> 35 kHz	40KHz	N/A	20 kHz	40 kHz
Control mechanism	TLM technique	DCM	Mixed-signal control	CCM	Adaptive control method
Load step response time (Heavy to light)	(90W to 20W) ~130ms	(90W to 55W) ~125ms	N/A	(400W to 200W) ~300ms	(200W to 50W) ~500ms
Load step response time (light to heavy)	(20W to 90W) ~150ms	(55W to 90W) ~125ms	(10% to 90%) 150ms (with notch filter) 50ms	(200W to 400W) ~300ms	(50W to 200W) ~280ms
Efficiency	95%	N/A	N/A	N/A	N/A
Advantages	TLM modulation with an integrated controller	High PF but discontinuous boost rectifiers	Mixed-signal realization with fast dynamic response	A simple low-cost modulating controller	Adaptive and fast-response technique
Disadvantages	Only need external power MOSFETs	Implemented by discrete circuits	System level implementation	Implemented by discrete circuits	Implemented by discrete circuits

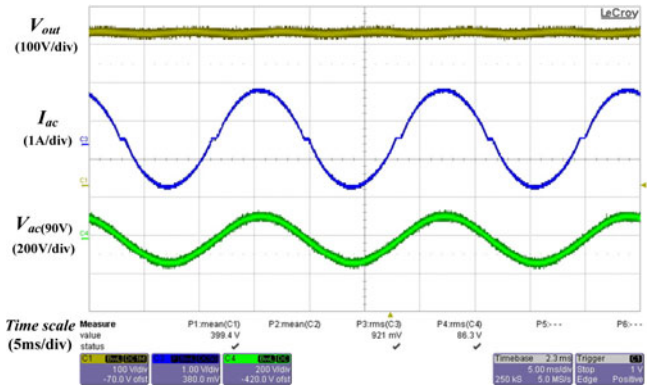

Fig. 26. Measured waveforms of the output voltage and the input ac current at the input ac voltage of 90 V.

VI. CONCLUSION

The PFC controller with the TLM technique can ensure high reliability and high efficiency of 95% at output power of 90 W. In addition, the PFC controller has low THD of 10% and high PF of 0.99 when the TLM technique is adopted. Furthermore, the proposed TLM can effectively clamp overshoot and undershoot voltages to be less than 24 V. The test circuit fabricated in the VIS 500 V UHV LDMOS process demonstrates the performance of the highly integrated PFC controller.

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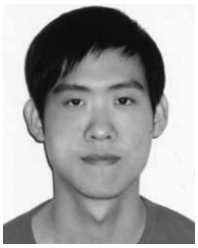

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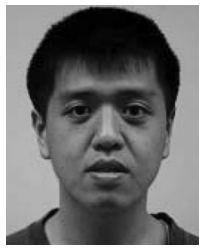

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