Expert Systems with Applications 40 (2013) 1491–1504

Contents lists available at SciVerse ScienceDirect

Expert Systems with Applications

journal homepage: www.elsevier.com/locate/eswa

Design of heart rate variability processor for portable 3-lead ECG monitoring system-on-chip

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ARTICLE INFO

Keywords:
ECG
Heart rate variability
Integrated health-care system
Portable system
Lomb periodogram

ABSTRACT

The worldwide population of people over the age of 65 has been predicted to more than double from 1990 to 2025. Therefore, ubiquitous health-care systems have become an important topic of research in recent years. In this paper, an integrated system for portable electrocardiography (ECG) monitoring, with an on-board processor for time–frequency analysis of heart rate variability (HRV), is presented. The main function of proposed system comprises three parts, namely, an analog-to-digital converter (ADC) controller, an HRV processor, and a lossless compression engine. At the beginning, ECG data acquired from front-end circuits through the ADC controller is passed through the HRV processor for analysis. Next, the HRV processor performs real-time analysis of time–frequency HRV using the Lomb periodogram and a sliding window configuration. The Lomb periodogram is suited for spectral analysis of unevenly sampled data and has been applied to time–frequency analysis of HRV in the proposed system. Finally, the ECG data are compressed by 2.5 times using the lossless compression engine before output using universal asynchronous receiver/transmitter (UART). Bluetooth is employed to transmit analyzed HRV data and raw ECG data to a remote station for display or further analysis. The integrated ECG health-care system design proposed has been implemented using UMC 90 nm CMOS technology.

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1. Introduction

The worldwide population of people over the age of 65 has been predicted to be more than doubled amount from 375 million in 1990–761 million by 2025 (Hooyman & Kiyak, 2002). Within a few years, society will be faced with the problem of an aged population. The aging of the population will inevitably add to the burden of an already fragile healthcare system plaguing virtually every major government. This trend is sure to result in a shortage of medical personnel, which, along with rising costs, will leave hospitals unable to meet the medical requirements of a growing number of elderly patients. In addition, the development of long-term health care environments has lagged behind compared to advancements in medical science. Therefore, whilst life expectancy is seen to be rising, inadequacies in daily healthcare may decrease the quality of life.

Technology can assist in alleviating the burden of doctors and medical staff by introducing a shift in the healthcare infrastructure (Grove, 2005). To maintain prolonged wellness, technologies designed for healthcare can be pushed towards the home environment enabling real-time monitoring, diagnosis, and prevention. Healthcare technologies that are able to be used at home can enable early detection of diseases or complications resulting from diagnosed or dormant cardio-vascular diseases (CVD). After detection, preventive steps can be taken to neutralize the problem before it develops into a life-threatening condition. Moreover, monitoring systems can provide remote observation of patients during prolonged treatment and indicate the state of recovery. Thus, ubiquitous healthcare for cardiac relating diseases is essential in improving the quality of life and longevity of our gradually aging population.

Portable ECG medical devices have become more and more widespread in recent years. The potential to acquire and monitor the ECG of a patient is a prospective ability with viable applications in telemedicine and various researches. However, such devices only provide a solution to wireless signal acquisition, and very often a remote science station is still needed for off-line analysis of the ECG signal. For a truly ubiquitous health care system, it should not only include basic functions for signal acquisition, but also provide the ability to perform accurate real-time analysis of the ECG data. Through SOC technology, integrated systems are able to acquire ECG data, to perform real-time data analysis, and to transmit data wirelessly all in a single low-area and low-power chip solution.

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http://dx.doi.org/10.1016/j.eswa.2012.08.042

In this paper, a portable multi-channel ECG monitoring system-on-chip with an on-board effective heart rate variability (HRV) processor is proposed. The first part of this system includes a front-end circuit and ADC controller for acquisition of three-channel ECG. In the second part, time–frequency analysis of HRV in ECG can be performed using a developed on-board HRV processor. Finally, in the third part, a compression engine is included in the system to reduce the size of data before wireless transmission. In the proposed SOC, the universal asynchronous receiver/transmitter (UART) standard is employed as the method of output.

This paper also consists of spectral estimation methods for short-term frequency domain HRV analysis as well as implementation considerations for SOC design. The capabilities of the Lomb periodogram for spectral analysis over traditional methods, such as Fourier transform, are compared and analyzed. A VLSI implementation of an HRV processor for time–frequency analysis using the Lomb periodogram has also been proposed. Finally, the HRV processor has been integrated into an ECG SOC for applications in portable ECG monitoring and real-time analysis with low-power and low-area. The significance of this ECG SOC is to enable practical development of portable real-time heart monitoring and analysis systems.

This paper is organized as follows. Sections 2 and 3 describe an integrated ECG health-care system and a time–frequency HRV processor, respectively. Performance analysis of HRV processor is provided in Section 4. We propose the ECG chip design and implementation in Sections 5 and 6, respectively. Finally, we conclude this paper in Section 7.

2. An integrated ECG health-care system

An integrated ECG health care system differs from many commercial ECG medical devices in that the functions are not restricted to only ambulatory monitoring. Through integration, the system can provide the user with on-line real-time analysis of the acquired ECG data in addition to being compact and portable. An integrated portable system with the ability to wirelessly transmit data has the following advantages:

- Increase the mobility of patients and allow for normal routines.
- Reduce the stress of patients from being attached to a medical system.
- More comfort during monitoring.
- Increase the applicability of ECG health-care.
- Provide on-the-fly analysis for immediate reaction.
- A more in-depth monitoring of heart status.
- Lower cost.

With these guidelines in mind, we are going to design our HRV processor.

3. A time–frequency HRV processor

3.1. The use of heart rate variability (HRV)

Heart rate variability is a normal physiological phenomenon where the interval between successive heart beats of an individual varies over time. The term "heart rate variability" has widely become the adopted term to describe the variations of both instantaneous heart rate and RR interval, or the interval between heart beats (Task Force of the European Society of Cardiology and the North American Society of Pacing Electrophysiology, 1996).

HRV has been shown to be an important indicator of cardiovascular health (Task Force of the European Society of Cardiology and the North American Society of Pacing Electrophysiology, 1996). As the regulation mechanism of the heart is closely governed by the sympathetic and parasympathetic nervous systems, HRV is often used as a quantitative marker of the autonomic nervous system. Studies have indicated that the HRV is an important indicator in many diseases and may contribute to a better treatment (Acharya, Joseph, Kannathal, Lim, & Suri, 2006; Joo, Choi, & Huh, 2012). Applications of HRV have been applied to many forms of medical researches including studies in sleep apnea, patient monitoring after cardiac arrest (Tiainen, Parikka, Makijarvi, Takkunen, Sarna, & Roine, 2009), and use in intensive care units (Kasaoka, Nakahara, Kawamura, Tsuruta, & Maekawa, 2010.

3.2. Spectral analysis of HRV

In signal processing, power spectral density (PSD) is a method of estimating how the total power of a data sequence is distributed over different frequencies (Stoica & Moses, 2005). The PSD is simply the representation of the signal using oscillations of various frequencies.

The time intervals between R-peaks, or RR intervals shown in Fig. 1(a), formulate a time series with the intervals between consecutive samples, as shown in Fig. 1(b). In other words, it is an unequally sampled time series where the time distance to the next sample depends on the magnitude of the next sample. This results in complications in performing HRV analysis as traditional power spectral analysis methods require the data to be equidistantly sampled.

Lomb developed a method for deriving the PSD of unevenly spaced data sets without the need for interpolation and re-sampling (Lomb, 1976). The Lomb periodogram has been shown to be a robust and accurate method for spectral analysis of HRV. It uses least squares fitting to estimate the magnitude of a given sinusoid with angular frequency ω_j over non-uniformly sampled data. In other words, the power of the given sinusoid, $P_N(\omega_j)$, for a set of data points of length N is computed using a least-squares fit to the model

$$x(t_i) = A \cdot \cos(\omega_j t_i) + B \cdot \sin(\omega_j t_i) + n(t_i) \tag{1}$$

for $i = 0,1,\ldots,N$, where $n(t_i)$ denotes noise. The Lomb transform is based on the discrete Fourier transform (DFT) for unevenly sampled signals given as

$$X_N(\omega) = \sum_j x_j \cdot e^{-i\omega t_j}. \tag{2}$$

As the Lomb method weights the data on a "per point" basis rather than a "per time interval" basis (Press & Rybicki, 1989), it is suitable for the analysis of non-uniform data. In the case of equal spacing it reduces to the Fourier power spectrum (Lomb, 1976). The Lomb periodogram of unevenly sampled data is

$$P_N(\omega) \equiv \frac{\left[\sum (x_j - \mu) \cdot \cos(\omega(t_j - \tau))\right]^2}{2\sigma^2 \cdot \cos^2(\omega(t_j - \tau))} + \frac{\left[\sum (x_j - \mu) \cdot \sin(\omega(t_j - \tau))\right]^2}{2\sigma^2 \cdot \sin^2(\omega(t_j - \tau))} \tag{3}$$

where μ and σ^2 are the mean and variance of data sequence, and τ is given as

$$\tau \equiv \frac{1}{2\omega} \tan^{-1}\left(\frac{\sum \sin(2\omega t_j)}{\sum \cos(2\omega t_j)}\right). \tag{4}$$

However, as the HRV is a reflection of physiological phenomena, it is considered to be a non-stationary signal. To monitor the changes of heart rate over a course of time, time–frequency spectral analysis is used. Time–frequency analysis using Lomb periodogram can be performed by applying a window $w(t)$ to the data and evaluating each segment individually. Using a sliding window configuration $w(t_j - t)$ the time–frequency distribution $P_N(t, \omega)$ is obtained, giving

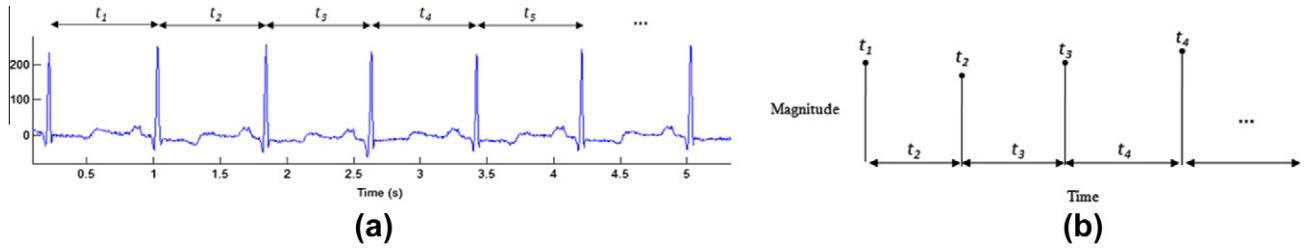

Fig. 1. (a) The *R*-peak to *R*-peak intervals of the ECG. (b) The derived non-equidistant RR interval time series.

$$P_N(t,\omega) \equiv N \cdot \left[\sum x'_j \cos(\omega t_j)\right]^2 + N \cdot \left[\sum x'_j \sin(\omega t_j)\right]^2 \quad (5)$$

where x' is the windowed zero-mean data at time t.

For portable biomedical applications such as devices for remote ECG monitoring, it is crucial to decrease device size through an efficient algorithm and optimized hardware architecture. Low-power and low-cost are also essential considerations when designing such systems. The real-time HRV processor comprises an RR interval calculation unit, a memory unit, and an HRV analysis unit. ECG data is sent into the processor, and the time intervals between heart beats are calculated through the RR interval calculation unit, and are stored in the on-chip memory. Using a sliding windowing scheme, time–frequency analysis of HRV is performed by the HRV analysis unit. The overall architecture of the proposed HRV processor is depicted in Fig. 2.

A flowchart demonstrating the signal processing steps of the Pan and Tompkins algorithm (Pan & Tompkins, 1985) for the classical derivative-based QRS detection is shown in Fig. 3. The ECG signal first passes through a set of linear processes, including a band-pass filter comprising a cascaded low-pass and high-pass, and a derivative function. Non-linear transformation is then employed in form of a signal amplitude squaring function. Finally, moving window integration is performed before an adaptive threshold is applied for detection of the QRS complexes.

The underlining principle of the algorithm is the detection of the slope of the *R* wave through the derivative function, amplified by the squaring function. The moving-window integration then provides wave-form feature information in addition to the detected *R* wave slope. Different from conventional method, in our system, as we are only interested in the RR interval in HRV analysis, we choose to assign an *R* peak to each detected *R* slope from the

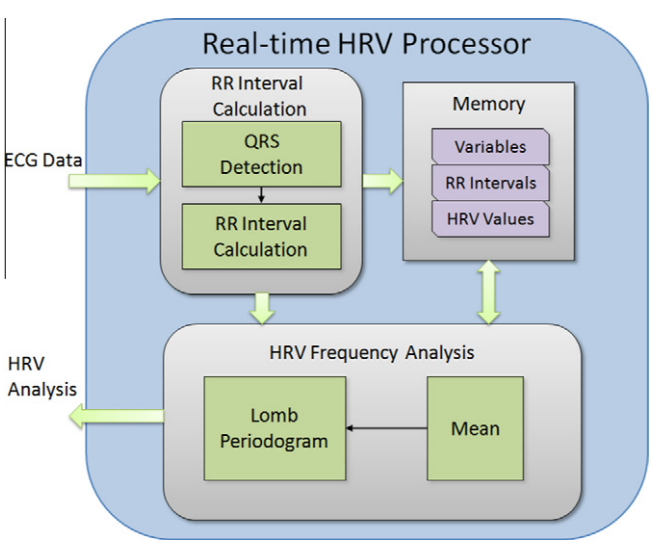

Fig. 2. Overall architecture of the HRV processor.

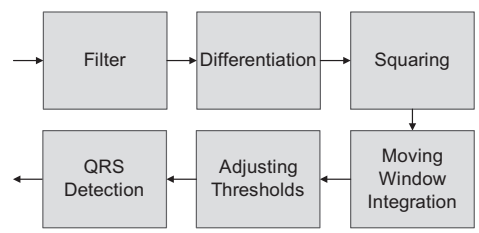

Fig. 3. Flowchart of the QRS detection algorithm by Pan and Tompkins.

output of the squaring function through an adaptive threshold. Thus, we only require the band-pass filter, derivative function, squaring function, and adaptive threshold in our system.

After differentiation, squaring function is employed to enhance the characteristics of the signal. Then a threshold is applied to the squared signal to detect the start of the QRS complex. The peak of the squared signal is identified as the *R* peak of the ECG data. Fig. 4 presents the flowchart for the detection of the R peak.

For evaluation of short term HRV, RR intervals of 2–5 min are suggested (Task Force of the European Society of Cardiology and the North American Society of Pacing Electrophysiology, 1996). In our design, in order to be able to address the high frequency (HF) and low frequency (LF) components of HRV, a two-minute window is adopted. Time–frequency analysis of HRV is achieved by performing spectral analysis on the RR intervals using a sliding window configuration. This produces a series of power spectra from sequential windows of data over time. To ensure a smoother transition between windows, and to provide better capability for observation, the sliding window is configured to have 50% overlap. This implies that the window of data moves forward by 1 min after every analysis of power spectra. The configuration of the sliding window is depicted in Fig. 5.

An SRAM memory is used to store the RR intervals before HRV analysis. The size of the memory depends on the maximum number of RR intervals obtainable in 2 min. As RR intervals are the time intervals between heart beats, the number of RR intervals should correspond to the number of beats. Thus, assuming that the maximum safe heart rate does not exceed 220 bpm (Tanaka, Monahan, & Seals, 2001), a 512-word SRAM memory is chosen. The overlap period between each window is 1 min, hence each minute of RR intervals, or each frame, has to be stored separately. In our design, the SRAM memory is categorized into two sections to store the different frames of RR intervals, thus 256 words can be allocated for each minute of data. During the one-minute period, data are stored into one section of the memory, after which the number of elements is noted and storage of data is switched to the second section using a path selector. After 2 min, the RR intervals are passed to the HRV analysis unit for spectral analysis. The scheme for SRAM memory usage is shown in Fig. 6.

To output the RR intervals to the HRV analysis unit, a bank selector is employed to choose which section of the SRAM is currently active. After all RR interval data are read from one section,

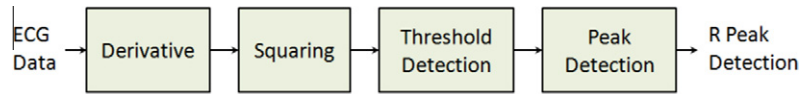

Fig. 4. Flowchart for *R* peak detection.

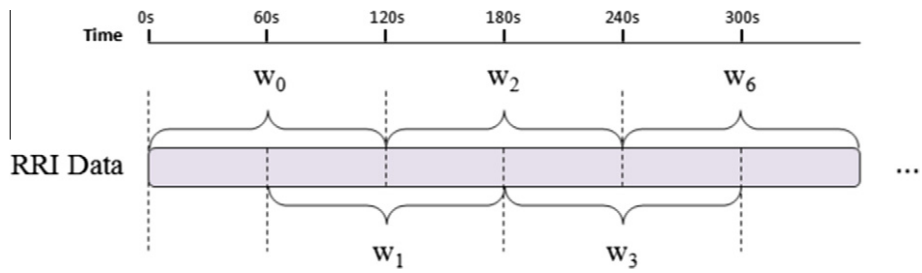

Fig. 5. The sliding window configuration. RR intervals are divided into 1 min frames.

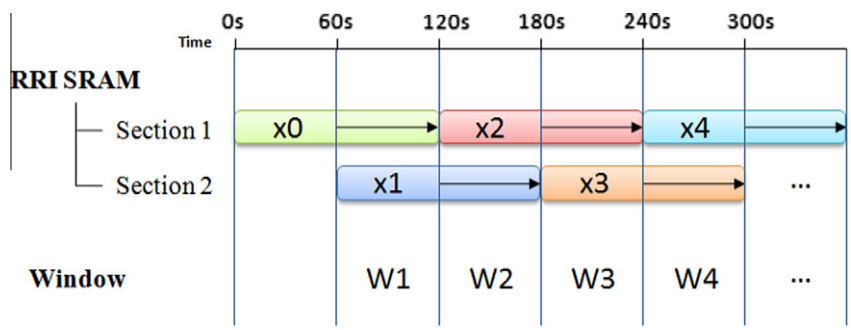

Fig. 6. Usage of the SRAM memory for RR intervals. X_i are the frames of data for one minute. The length of retention is marked by the arrows. W_i denotes the corresponding windows.

the next section is selected. As spectral analysis in Eq. (5) requires the signal to be zero-mean, the mean of the data in each section is calculated and stored. This ensures that when the next window is encountered, the overlapping section from the previous window has the correct mean value. The two mean values are added together to form the final mean of the data. Division of two is simplified to a bit-shift (or re-position of the fixed point). The architecture of the SRAM memory control unit is shown in Fig. 7.

The HRV analysis unit comprises the hardware implementation of the Lomb periodogram given in Eq. (2). RR intervals are aperiodic finite-energy signals, therefore they have continuous spectra. This would be unrealistic in hardware implementation, so we suppose that the spectrum can be periodically sampled. Considering that discrete-time sampled signals are periodic with period 2π (Proakis & Manolakis, 2006), we can take N equidistant samples in the interval $0 \leqslant \omega < 2\pi$ with spacing $\delta\omega = \frac{2\pi}{N}$. Evaluating Eq. (2) at $\omega = \frac{2\pi}{N} \cdot k$ for $k = 0, 1, \cdots, N-1$, we can obtain

$$X_N\left(\frac{2\pi k}{N}\right) = \sum_j x_j \cdot \cos\left(\frac{2\pi k}{N} \cdot t_j\right) + i \cdot \sum_j x_j \cdot \sin\left(\frac{2\pi k}{N} \cdot t_j\right). \tag{6}$$

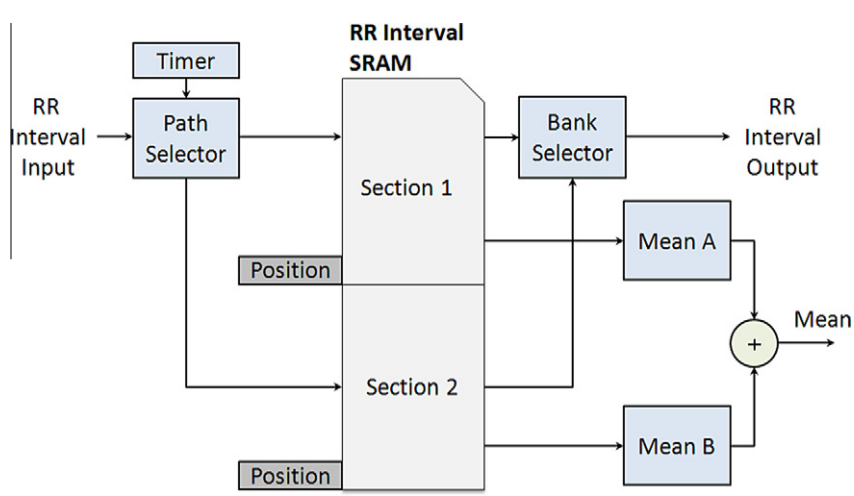

Fig. 7. Architecture of the memory control unit.

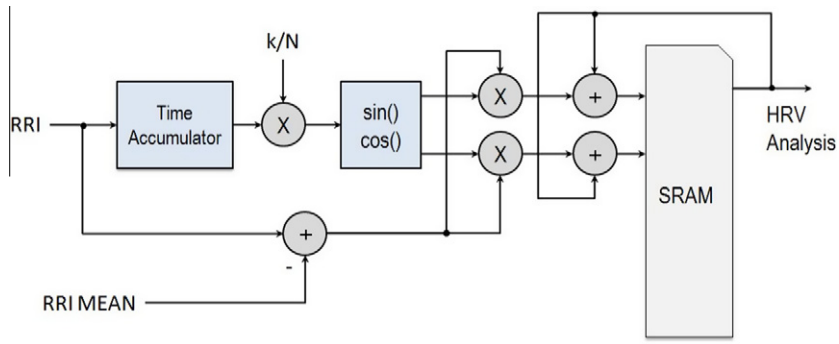

Fig. 8. Architecture of the HRV analysis unit.

In spectral analysis of discrete-time equidistant data series, the spectrum is normalized to the sampling rate. However, for the Lomb periodogram, the time value t_j is included in the calculation, therefore actual frequency values vary according to the unit of time used. In our design, the RR intervals are represented using seconds, therefore, remembering that $k = 0, 1, \cdots, N-1$, the spectrum is normalized to 1 Hz. The frequency ranges of the components in HRV are below 0.4 Hz, thus only less than half of the frequencies are required. To simplify the design, only frequencies over 0–0.5 Hz are analyzed. The number of points over this frequency range is selected to be 256 points, which yields a frequency resolution of approximately 0.002 Hz per point.

To calculate the point in time of the current input, recall that RR intervals are the time intervals between beats, the current point in time can be inferred from the sum of time intervals of previous inputs. This is accomplished in our system using an accumulator. Inputs are added to the previous point in time to obtain the current time value. The time value is then multiplied with the index k, which is implemented with a counter to increment 0 to $N-1$ for each input. Synopsys DesignWare is employed to implement the sine and cosine functions before being multiplied with the RR interval inputs. The result is added to previously calculated coefficients stored in SRAM memory and updated after each calculation. To be able to read and write during the same cycle, synchronous two-port SRAM is applied to store the coefficients. The architecture of the HRV analysis unit is shown in Fig. 8.

4. Performance and analysis of the HRV processor

4.1. ECG beat detection

To analyze the performance of the RR interval calculation unit, ECG signals from the MIT-BIH Arrhythmia Database are used. It contains 48 30-min excerpts of two-channel ambulatory ECG recordings. The recordings are digitized at a sampling rate of

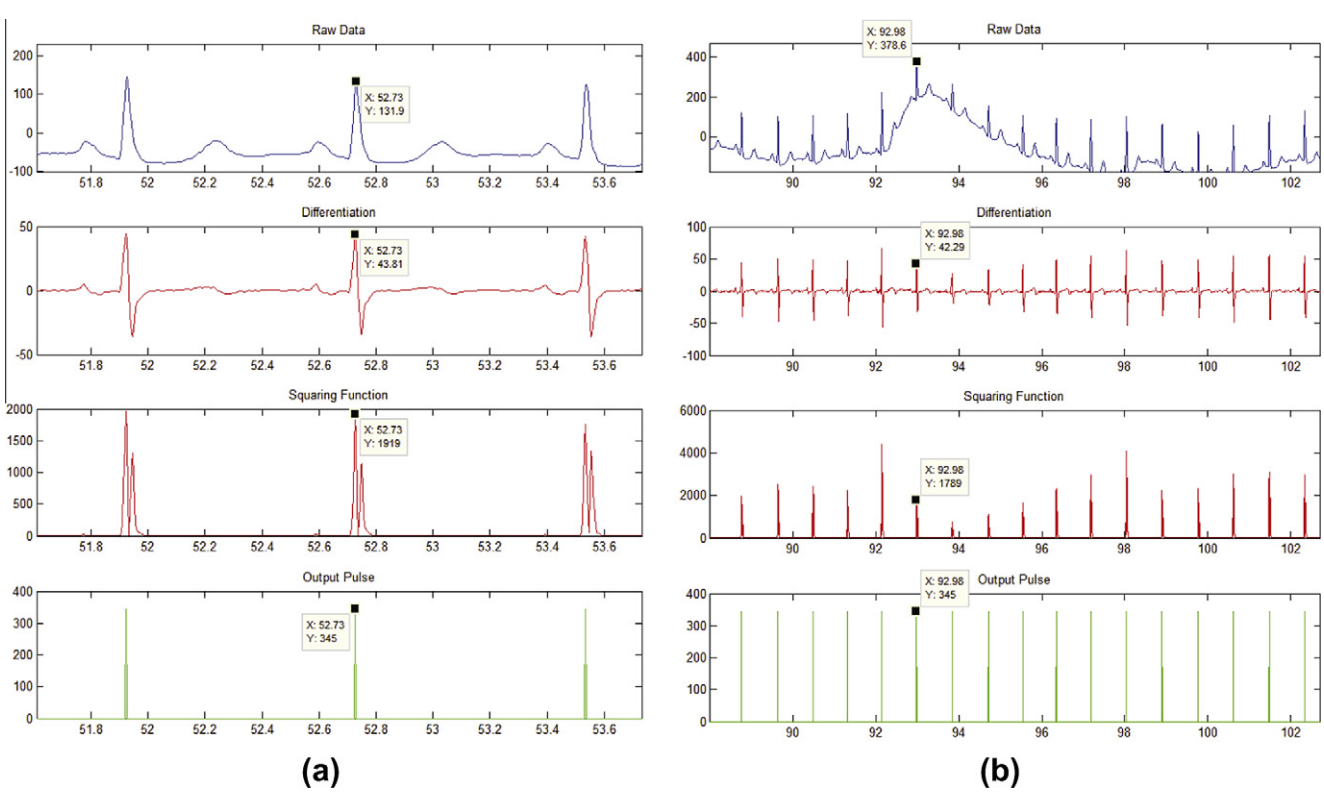

Fig. 9. Resulting output from each stage of the QRS detection algorithm for (a) clean ECG signal and (b) ECG signal with motion artifact. The detected output pulse corresponds to the R peak of the original ECG signal.

360 Hz with an 11-bit ADC. To maintain consistency with our system specification, the ECG signals are re-sampled to 256 Hz with 10-bit precision before being used to test the performance of our beat detection unit. Only channel 1 (Lead II) of the two-channel ECG recording is used in our analysis.

Corresponding to Figs. 3, 4 and 9 shows the output of each stage in our beat detection unit: differentiation, squaring, and final output pulse. The output pulse can clearly pinpoint the *R* peak of a clean ECG signal and an ECG signal with motion artifact within a precision of one sample. For ECG signals with various types of noise, artifacts, and distortion, the designed system is able to identify beats in most cases, as shown in Fig. 10.

4.2. Spectral analysis of HRV

To compare spectral analysis performance, an understanding of the underlining oscillations within the signal is required. Since this can rarely be done with real RR tachograms, an artificial signal that

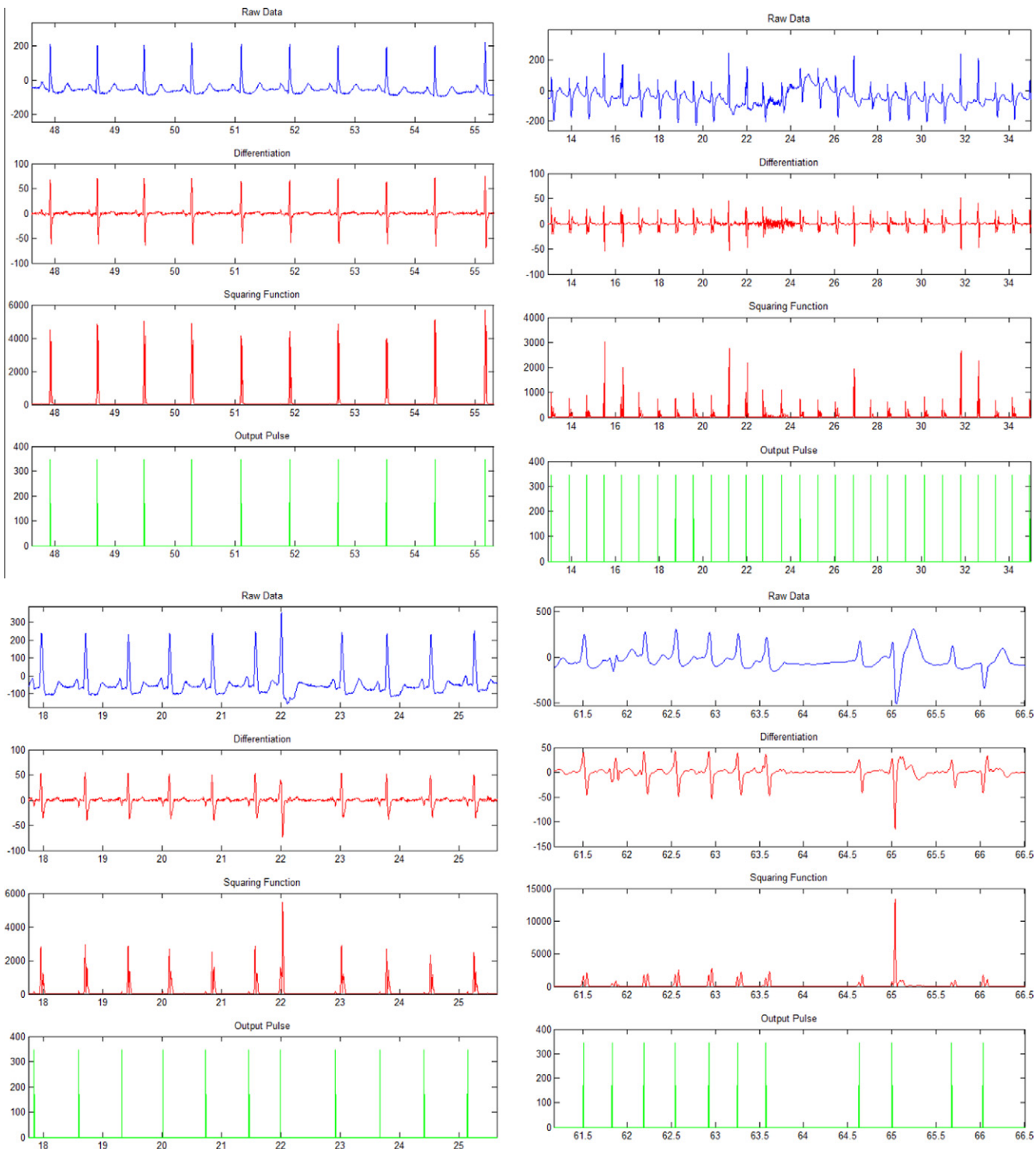

Fig. 10. Beat detection of ECG signals with different types of distortion.

closely simulates the characteristics of RR intervals is generated to verify the performance.

To generate an artificial heart rate signal, we consider that the peaks in the PSD of a short-term RR tachogram can be represented roughly as 0.25 and 0.1 Hz corresponding to the HF and LF regions respectively (McSharry, Clifford, Tarassenko, & Smith, 2002). Thus, artificial RR signal is modelled as the oscillation of these two frequencies around the average heart rate. Assuming an average heart rate of 70 bpm, the artificial heart rate function can be

$$\mathrm{HR}(t) = \mathrm{HR}_0 + A_L \cdot \sin(2\pi f_L t + \theta_L) + A_H \cdot \sin(2\pi f_H t + \theta_H) \quad (7)$$

where θ_L and θ_H are initially assumed to be 0, $\mathrm{HR}_0 = 70$, $A_L = A_H = 1$, $f_L = 0.095$, and $f_H = 0.275$.

The heart rate function is applied to iteratively calculate the RR intervals, which is obtained by dividing one minute by the instantaneous heart rate. Starting with an initial interval, the next interval can be calculated from the heart rate function in Eq. (7). The obtained interval is then added to the time consumed previously to generate the next interval from the heart rate function.

The generated artificial RR interval is shown in Fig. 11. There are 256 points analyzed in our implementation of the Lomb periodogram, so to produce a fair comparison, the results are compared with those that have the same number of points. As we interpolate using a re-sampling rate of 4 Hz, to produce 256 points between 0 and 0.5 Hz requires 1024-point FFT. The resulting PSD of the artificial RRI using Lomb periodogram compared with results using 1024 point FFT is shown in Fig. 12. Also, the LF/HF ratio is calculated for each method and the error percentage is compared in Table 1.

Finally, to simulate time-varying properties, the central frequency of the HF is configured to sweep linearly from 95% to 105% of the original value over the course of generation. The result-

Table 1
LF/HF ratio comparison of artificially generated RRI (LF/HF = 1).

LF/HF ratio	Value	Error
Actual	1.000000	–
FFT	1.095631	9.563%
Lomb–Scargle	0.983035	1.697%
This work	1.003755	0.375%

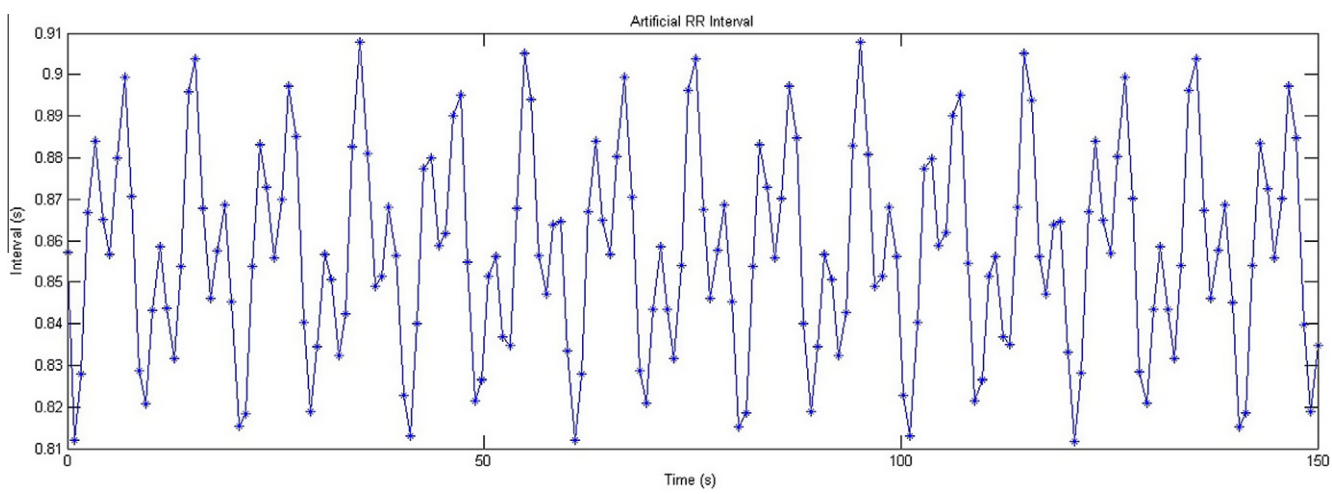

Fig. 11. Generated artificial RR interval time series.

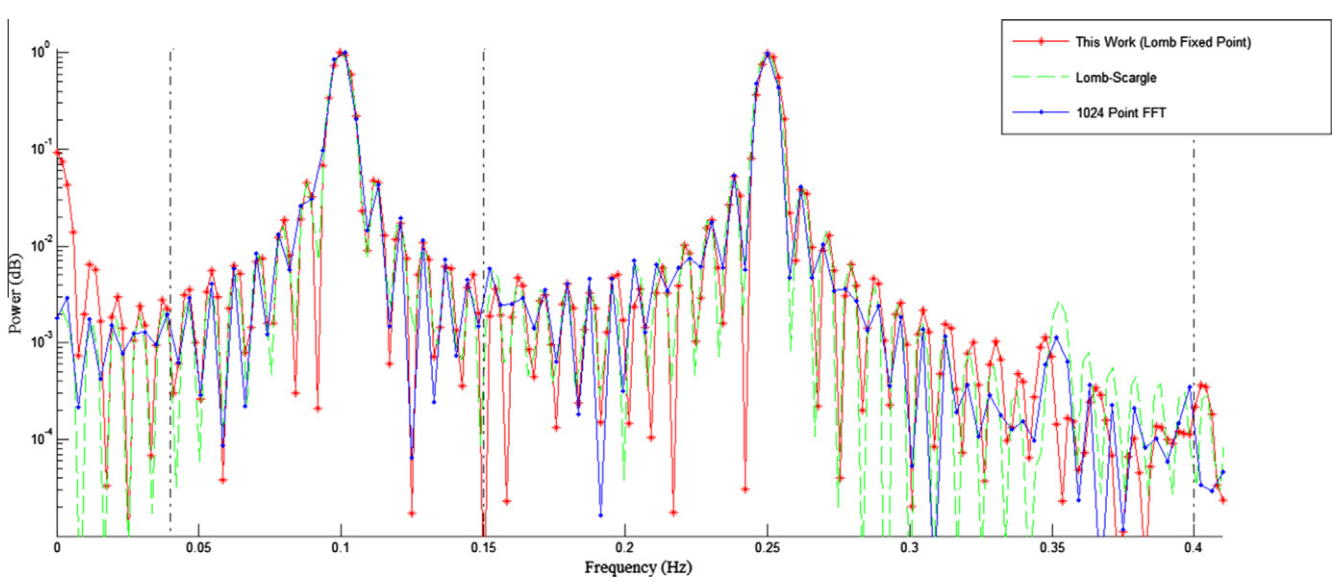

Fig. 12. Power spectral density of artificially generated RRI in Fig. 11 using 1024 point FFT, Lomb–Scargle periodogram, and our fixed point Lomb method. The RRI time series is re-sampled at 4 Hz before FFT analysis.

ing time frequency distribution using the Lomb periodogram is shown in Fig. 13.

In addition to simulation using artificial RRI, data from PhysioBank's online ECG database has been used to verify the HRV processor design. Databases including the MIT-BIH Arrhythmia Database and the MIT-BIH Normal Sinus Rhythm Database have been used to compare results. Fig. 14 depicts the PSD of a single window compared with results using 1024 point FFT and the Lomb–Scargle periodogram. A time–frequency distribution of HRV is shown in Fig. 15.

4.3. Discussions

The Lomb–Scargle periodogram has been demonstrated to be a good PSD estimator of unequally sampled data. Although the errors due to re-sampling are difficult to perceive using real bio-signals, as it is impossible to obtain the original components, it is important to note how efficient the Lomb periodogram is at performing PSD analysis of un-equidistant data. When compared to traditional time frequency distributions using FFTs of approximately the same area size (or total number of points), the Lomb periodogram yields higher frequency resolution within the frequencies of interest. Due to the need to re-sample RR intervals at higher frequencies for FFT analysis, only a portion of the FFT outputs are within frequencies of interest. The Lomb periodogram, however, maps all points to the frequencies of interest. This is due to the fact that the Nyquist rate is not well defined for unequally spaced data and we are able to obtain information from well above the Nyquist rate. With a higher re-sampling frequency, the number of required points for FFT becomes unrealistic for hardware implementation, whereas there is no need to consider re-sampling frequency when using Lomb periodogram. Therefore, the Lomb periodogram has been proven to be a hardware efficient method of performing PSD analysis of HRV.

Summing up the results of this section, a time frequency distribution using Lomb periodogram for HRV analysis has been developed. The algorithm has been implemented in an HRV processor

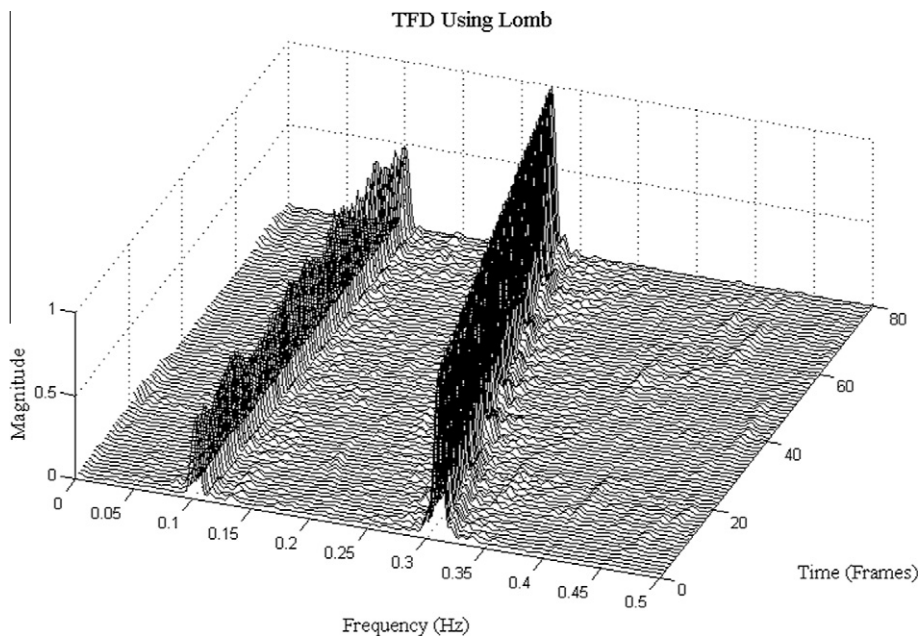

Fig. 13. Time–frequency distribution of artificial RR interval with HF frequency sweep using the Lomb periodogram.

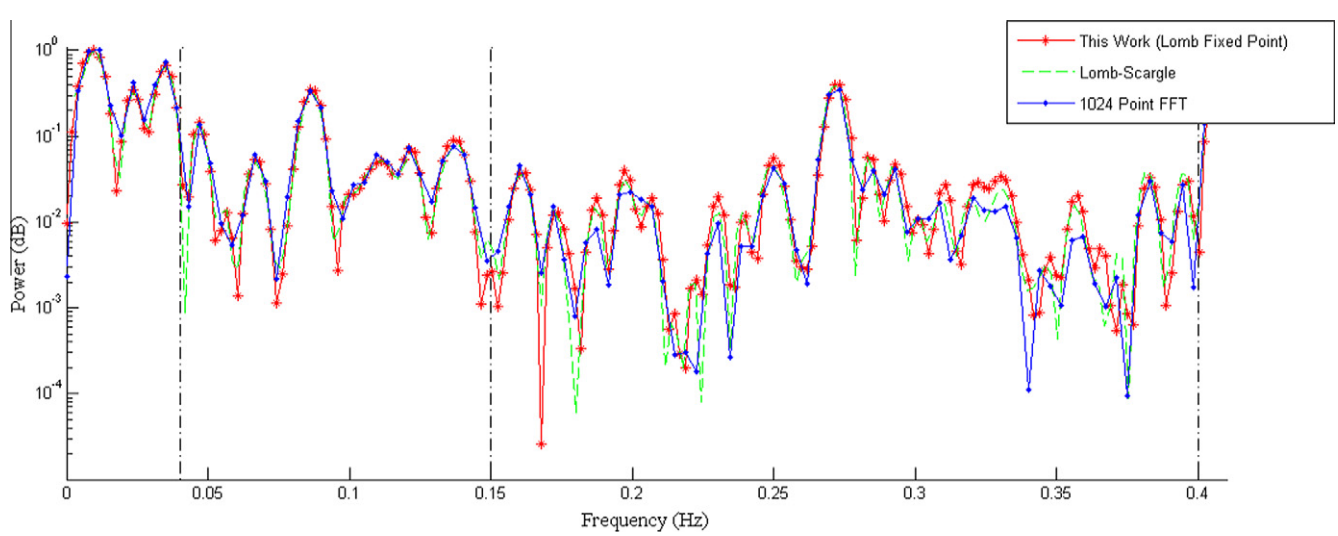

Fig. 14. Power spectral density of RRI data from the MIT-BIH Arrhythmia Database as calculated using 1024 point FFT, Lomb–Scargle periodogram, and our Lomb method.

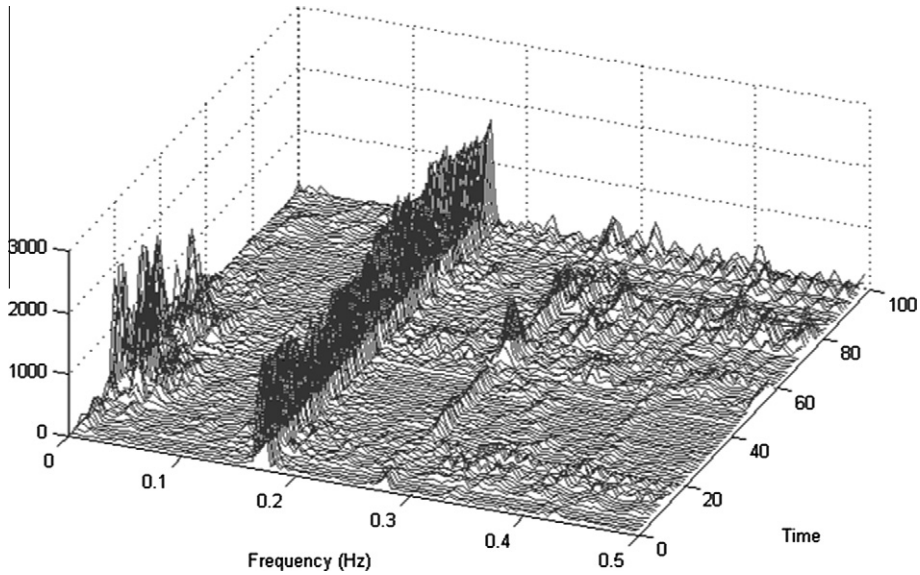

Fig. 15. Time–frequency HRV analysis using Lomb TFD of ECG data from the MIT-BIH arrhythmia database.

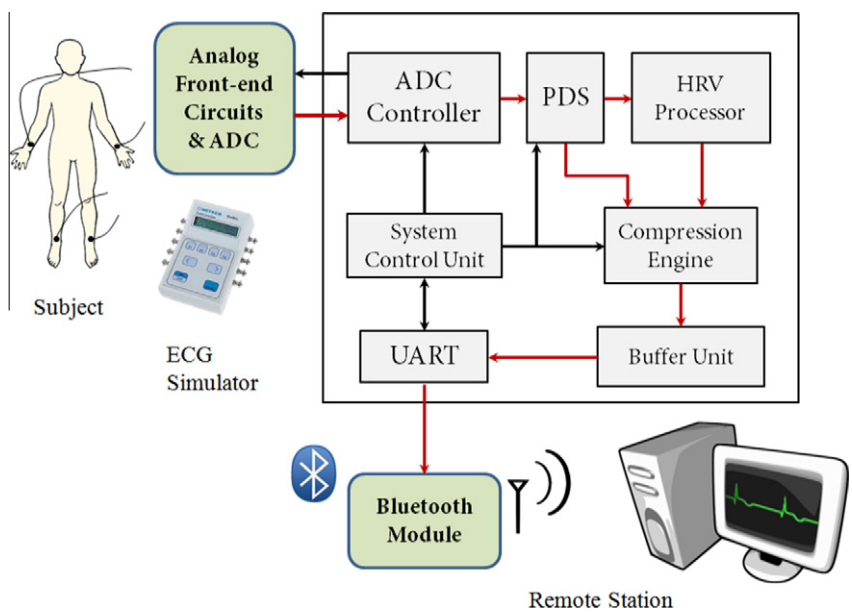

Fig. 16. Overall system architecture for the ECG SOC.

for processing raw ECG data and performing HRV analysis. Moreover, the HRV processor has been implemented as an ECG system for portable ECG monitoring and HRV analysis system. The proposed system, integrated with an HRV processor using windowed Lomb periodogram, is suitable for portable and low power medical devices for ECG monitoring and TFD HRV analysis.

5. ECG system-on-chip design

In this section, providing adequate healthcare for the gradually aging population, in light of reduced personnel and rising costs, is a problem the modern world that is currently faced with. Portable medical systems developed for bringing healthcare to the average user as well as the elderly is a rising trend which can benefit the entire social healthcare infrastructure. To enable practical employment of ubiquitous healthcare devices for portable medical applications, an experimental ECG system-on-chip prototype has been developed. Here we describe the architecture of the proposed ECG SOC as well as the means of system verification.

5.1. Overview of system architecture

The designed ECG SOC can serve as a portable solution to 3-lead ECG acquisition and remote monitoring. An on-chip HRV processor is also included in the system for time–frequency analysis of HRV using the Lomb periodogram. To communicate with a remote station, the UART module has been implemented to interface with a Bluetooth module or a PC. The final ECG SOC has been implemented using UMC 90 nm CMOS technology.

The system architecture of the ECG SOC is illustrated in Fig. 16. It is composed of three parts. First, an ADC controller is included to retrieve three-channel ECG from the 10-bit ADC in front-end circuits. Secondly, an onboard beat detection unit and HRV analysis engine is employed to perform time–frequency HRV analysis using

Table 2
Specifications of the analog front–end circuits & ADC.

Parameters	Value
ECG channel number	3
Sample rate (Hz)	256
LPF cut-off freq. (Hz)	150
Gain (dB)	40
Output range (V)	0.3 ~ 1.5
ADC resolution	10
ADC effective no. of bits	8.6

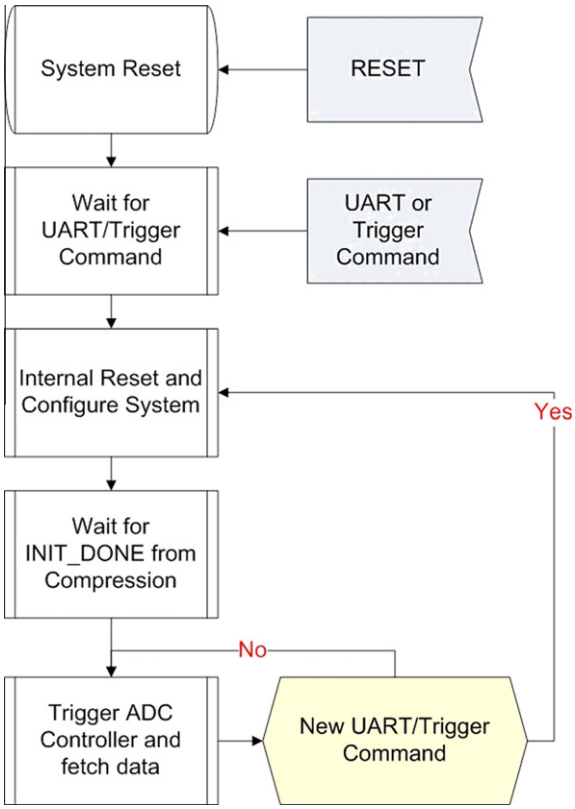

Fig. 17. System control flow diagram.

a windowed Lomb periodogram. Finally, a lossless ECG compression engine compresses data before wireless transmission using Bluetooth to a remote station for display or further diagnosis. As UART is used for the communication interface, the system is able to interface with other devices that have UART, such as ZigBee modules or a PC.

5.2. ADC controller and system control

The ECG SOC is interfaced with an analog front-end IC designed for biomedical applications. The analog front-end IC comprises multi-channel amplifiers and filters for acquisition of up to 7 channels of ECG; to meet our specifications depicted in Table 2, in our system only 3 channels are activated. An ADC is also included in the IC for data conversion.

The system control unit (SCU) is responsible for initialization of the system, decoding of the current configuration, and generating control signals decoded from the current configuration to corresponding modules. The ECG SOC receives configurations from a remote station via the UART interface to startup the system. In addition, a trigger signal is employed to enable a manual start so that the system can be reset to a default mode without the need of configuration commands from the remote station.

After receiving a configuration command, the SCU decodes the command. If system re-configuration is required, it issues an internal reset to all modules. The system then restarts with the new control signals and the configuration is loaded. The control flow diagram of the SCU is depicted in Fig. 17.

5.3. HRV processor

The overall architecture of the HRV engine is depicted in Fig. 18. It performs time–frequency HRV analysis on a heart rate window of two minutes with 50% overlap. Spectral analysis using the Lomb periodogram is calculated using a novel low area fixed-point hardware design. With Figs. 7 and 18, the proposed HRV engine is cost-effective in obtaining accurate time–frequency domain HRV analysis without the need for microprocessors or software on remote stations.

5.4. Compression engine

Wireless data communication occupies a large share of the total power consumption in most portable wireless devices or systems,

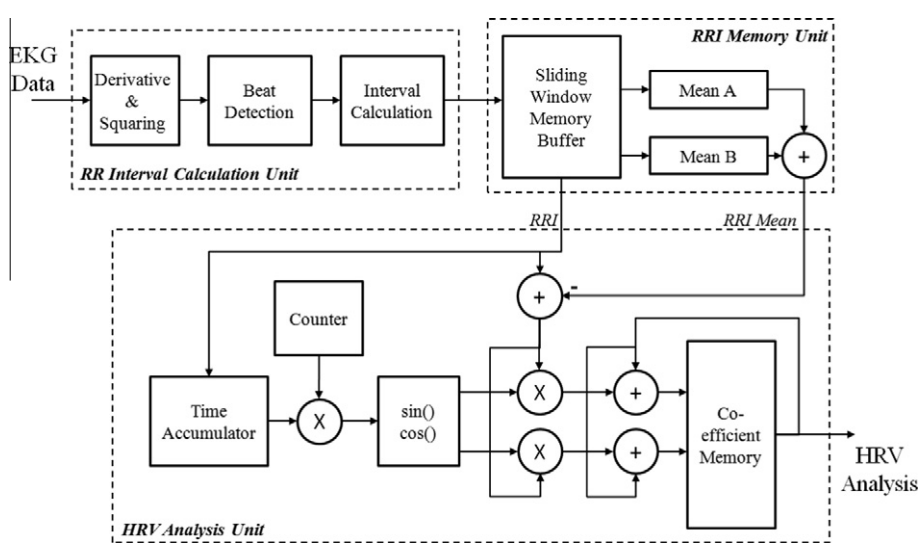

Fig. 18. Architecture of HRV processor.

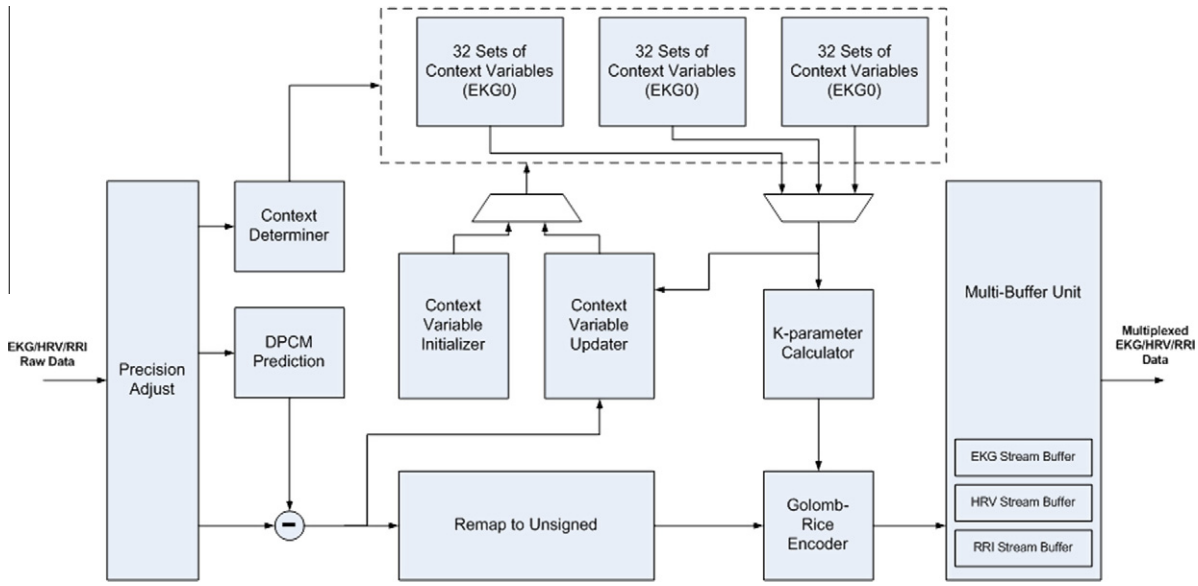

Fig. 19. Architecture of the lossless compression engine.

with power dissipation proportional to the amount of data transferred. With the energy consumption of today's wireless transceivers ranging between 0.6 and 75 nJ/bit depending on modulation scheme, protocol, data rate and transmitter power output (Thoné, Radiom, Turgis, Carta, Gielen, & Puers, 2009), data compression performed in a submicron technology domain is expected to result in overall power savings. For our ECG processor, a lossless compression technique is chosen to avoid the possibility of losing ECG artifacts of potential diagnostic value.

Table 3
Specifications of the compression engine.

Parameters	This work	K. Chen, Chua, Tseng, Fu, & Fang, 2010
Max. operation frequency	32 MHz	32 MHz
Data type	ECG	EEG
No. of channels	3	4
Sample bit precision	8, 10, 12, 16, 20	8, 10, 12, 16
Memory size	3,168 bits	4,224 bits
Header support	Yes	No
Compression ratio	2.50	1.70
Technology	90 nm CMOS	90 nm CMOS

The architecture of the compression engine, shown in Fig. 19, comprises a precision adjust unit, a context determiner, a differential pulse code modulation (DPCM) predictor, a context-based *k*-parameter estimator, a prediction memory array (3-channel ECG), a set of context variable upkeep modules, a remap to unsigned unit, a Golomb-Rice entropy coder, and a 40-bit multi-stream packer/multiplexer. To enhance the compression performance, each ECG sample is classified according to a context rule based on a finite number of previous samples (Memon, Xuan, & Cinkler, 1999), with the Golomb-Rice *k*-parameter estimated for each context and particular sample. To minimize area and latency, the need for sample buffers is replaced by employing an adaptive *k*-parameter estimation algorithm (Weinberger, Seroussi, & Sapiro, 2000). The compression unit also accepts RR interval and HRV

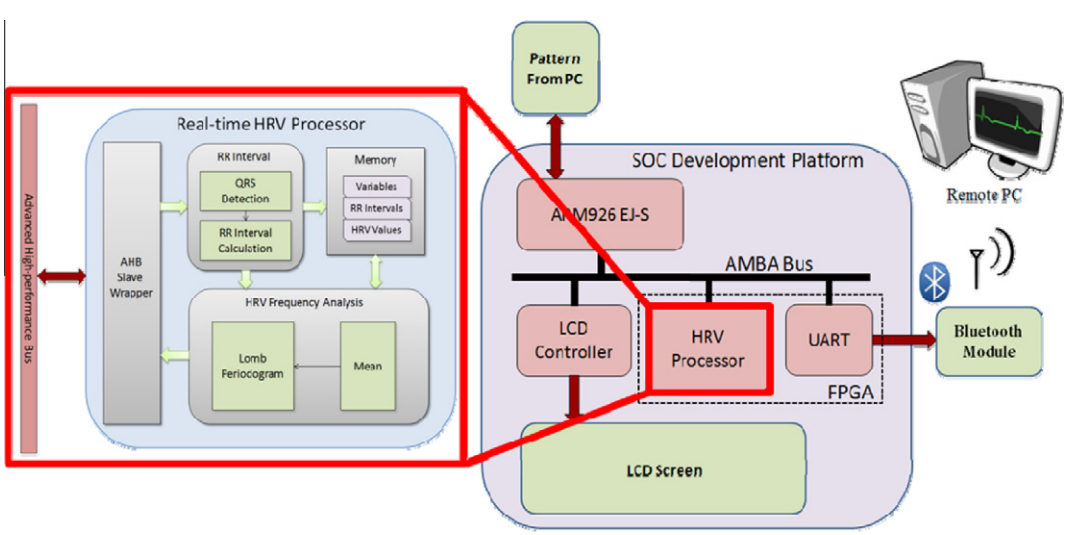

Fig. 20. Verification of the HRV processor on FPGA.

coefficient data, which, together with compressed or raw ECG data are packetized and multiplexed onto a single data stream. Table 3 shows the specifications of the compression engine compared to previous works in Chen, Chua, Tseng, Fu, and Fang (2010).

5.5. Wireless communication

As the UART standard is used for output of data, many forms of communication protocols can be utilized. Through UART, the system can be interfaced with a wireless chip solution, a PC, or any other device with UART. To verify the capabilities of various output methods, wireless transmission using the IEEE 802.15.4 standard as well as the Bluetooth standard are implemented in this paper.

5.6. System verification

An SOC development platform from Socle Technology is initially employed to verify the system blocks. The SOC development platform provides an ARM926EJ-S processor and various peripheral modules, including a Xilinx FPGA, which are connected to the ARM processor through an AMBA High-performance Bus (AHB). The designed HRV processer is implemented on the FPGA and verified with patterns sent from a PC. In-circuit emulator (ICE) is employed to feed ECG patterns into the ARM processor which then passed the data to the FPGA on the AHB bus. To connect the HRV processor on the FPGA to the AHB bus, an AHB wrapper is added to the original architecture, which provides a handshaking interface between the HRV processor and the AHB bus. The UART module is also implemented so that the capability to communicate with the Bluetooth module using a system clock of 24 MHz could be verified. The setup of FPGA verification is shown in Fig. 20.

Tests using the Socle Development Platform have verified that the HRV processor is capable of calculating time–frequency analysis in real-time and is possible to implement using VLSI technology. Results also indicate that the UART module is successful in communicating with the IEEE 802.15.4 module, Bluetooth module, as well as a PC using RS-232. Wireless transmission with the Bluetooth module is enabled for a prolonged time to check for possible data-loss during transmission. Final results have verified that the FPGA system can effectively operate and send data without data-loss.

6. Chip implementation

6.1. Chip tape-out

The ECG System-on-Chip design proposed in Sections 5 is scheduled for tape-out under UMC 90 nm SPHVT 1.0V 1P9M process technology. To reduce static power consumption, the chip has been implemented using high Vt process (HVT) library. The floorplan and I/O plan of the chip is depicted in Fig. 21(a), with the total number of pads is 36, including 14 power pads and 22 logic pads. Fig. 21(b) shows the layout of the chip. The die size is 800 μm by 800 μm, and the core size is 512 μm by 512 μm, with the working system clock frequency is 24 MHz. By using HVT library, a reduction of 31% in total power consumption is achieved compared to RVT library. The overall power consumption of the chip is 523 μW as simulated with Synopsys Prime Power. Detailed statistics of the chip are shown in Table 4.

6.2. Setup of the integrated ECG health-care system

The fabricated ECG SOC will be applied to the prototype of an integrated ECG health-care system. The integrated ECG system includes front-end circuits for amplification and filtering of three-channel ECG signals. As the ECG is a bioelectric signal, its amplitude is relatively small and can be easily corrupted by noise. Therefore, an instrumentation amplifier (IA) is included in the front-end circuits to amplify the ECG signal at the first section. Next, the signal is filtered using a notch filter with cut-off frequency of 60 Hz for rejection of power-line interference. Then

Table 4
Summary of the ECG SOC chip design.

Parameters	Value
Technology process	UMC 90 nm SP_HVT process 1.0 V
Die size	800 μm × 800 μm
Core size	512 μm × 512 μm
IO pad number	36 (14 power, 22 logic)
Gate count	93,701
Clock frequency	24 MHz
On-chip SRAM	3.2 KB
Power consumption	523 μW

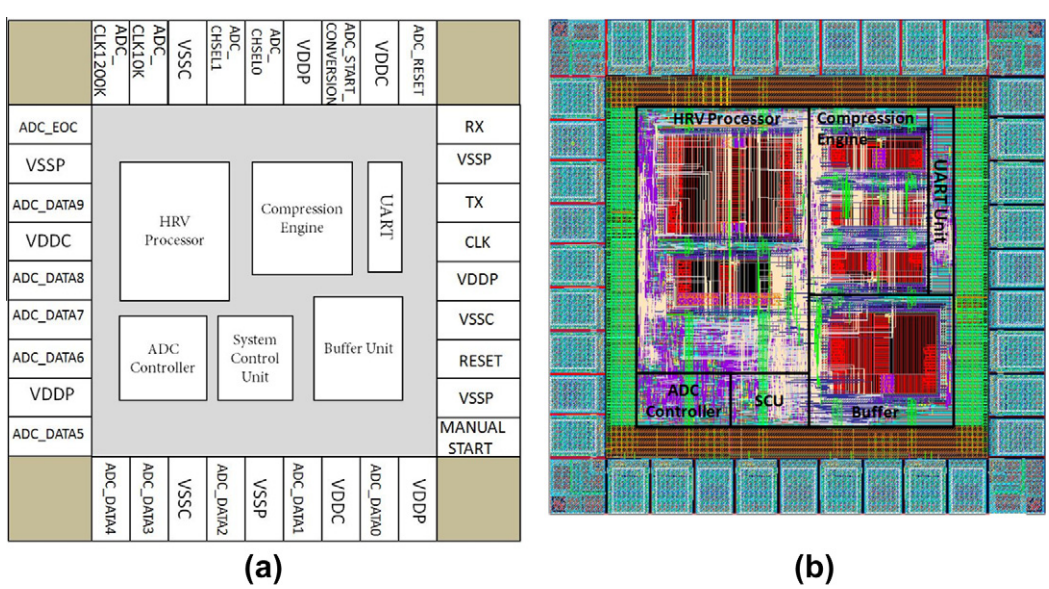

Fig. 21. The on-board HRV processor. (a) Floorplan and I/O plan. (b) Chip layout of the ECG SOC.

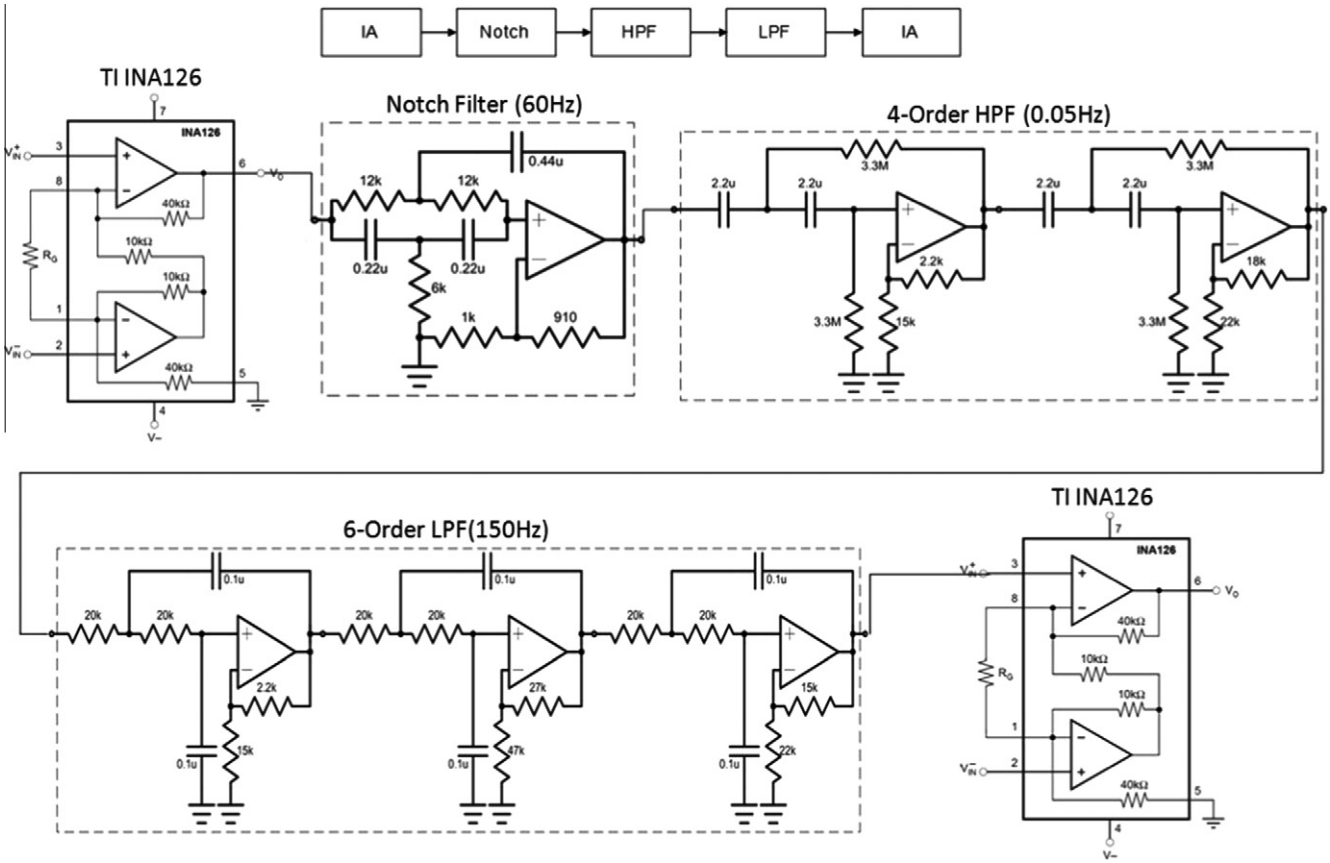

Fig. 22. Circuit schematic of the front–end sensor circuit.

a high-pass and low-pass filter limits the ECG signal to 0.05 and 150 Hz before another IA amplifies the final output signal. The schematic of the front-end circuits is shown in Fig. 22. After the front-end circuits, there is an analog multiplexer and 10-bit ADC that can be controlled by the ECG SOC for acquisition of ECG data. Finally a Bluetooth module is included to transmit data to a remote base station.

7. Conclusions

In light of the aging population, healthcare systems designed for portable and at-home applications can alleviate the problems of caring for a growing number of elderly patients. Such medical devices can also assist in maintaining a healthy condition of the general population. In this paper, we propose a design of a low area and low power ECG system-on-chip for applications in portable biomedical devices. The ECG SOC can acquire three-channel ECG data from external front-end circuits through an ADC controller. A lossless compression engine with compression ratio of 2.5 is employed before data is sent by wireless transmission through a Bluetooth module. An on-board HRV processor is able to perform time–frequency analysis of HRV according to user configurations. The proposed system is well integrated and is configurable through remote commands or a trigger signal. Through the use of UART standard, the system is able to easily connect with other modules or ICs increasing the compatibility and robustness of the design. The ECG SOC has been verified on FPGA and implemented using UMC 90 nm SPHVT 1.0V 1P9M process technology.

In portable applications, the tradeoff between system complexity and device size is often an important issue. However, VLSI design can help in the implementation of an architecture that has high analysis capability and yet is small in device size. The design and implementation of the ECG SOC proposed in this paper demonstrates the possibility of an SOC solution for portable medical devices that can benefit doctors, patients, and researchers.

Acknowledgments

This work was supported in part by the National Science Council of Taiwan, ROC, under Grants NSC-99-2220-E-009-071, NSC-100-2220-E-009-052, NSC-100-2220-E-009-054, and NSC-101-2220-E-009-049. Prof. Wai-Chi Fang was sponsored in part as the TSMC Distinguished Chair Professor by the TSMC Foundation. The authors would also like to express their sincere appreciation to the UMC University Shuttle Program and the National Chip Implementation Center for chip fabrication and testing service.

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