A 0.33-V, 500-kHz, 3.94-μW 40-nm 72-Kb 9T Subthreshold SRAM With Ripple Bit-Line Structure and Negative Bit-Line Write-Assist

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***Abstract*—This paper presents an ultra-low-power 72-Kb 9T static random-access memory (SRAM) with a ripple bit-line (RPBL) structure and negative bit-line (NBL) write-assist. The RPBL scheme provides over 40% read access performance improvement for VDD below 0.4 V compared with the conventional hierarchical bit-line structure. A variation-tolerant ripple-initiated NBL write-assist scheme with the transient negative pulse coupled only into the single selected local bit-line segment is employed to enhance the NBL, boosting efficiency and reducing power consumption. The 331 $\times$ 385 μm^2 72-Kb SRAM macro has been fabricated in UMC 40-nm low-power CMOS technology and was tested with full suites of SRAM compiler qualification patterns. Error-free full functionality without redundancy is achieved from 1.5 V down to 0.33 V. The measured maximum operation frequency is 220 MHz (500 kHz) at 1.1 V (0.33 V) and 25 °C. The measured total power consumption is 3.94 μW at 0.33 V, 500 kHz, and 25 °C.**

***Index Terms*—Negative bit-line (NBL), ripple bit-line (RPBL), subthreshold static random-access memory (SRAM), ultra-low voltage, 9T SRAM cell.**

I. Introduction

FOR ultra-low-power portable applications, it is crucial to minimize energy per operation to extend battery life. It has been shown that the minimum energy point is formed by operating the circuits slightly below the threshold voltage [1], [2]. However, the benefit comes at the expense of significantly larger variations and degradation of transistor characteristics in subthreshold region. The exponential dependency of drive current on $V_{\rm GS} - V_{\rm T}$ leads to large process, voltage, and temperature (PVT) variations. The degradation and large dispersion of I_{on}/I_{off} ratio pose significant design challenges for circuit functionality and reliability.

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For the most commonly used on-chip 6T static random-access memories (SRAMs), the degradation of cell stability and write-ability with reduced supply voltage severely limits the minimum operating voltage $V_{\rm MIN}$ [3]. Most low-voltage SRAM cells [4]–[22] utilize a dedicated Read port to decouple the cell storage node from the BL Read current path, thus eliminating the Read disturb [4]–[16], [20]–[22]. However, many of the low-voltage SRAM cells [4]–[15], [20]–[22] perform a 6T-like Write operation; hence, the Write Half-Select disturb persists, and these cells are not suitable for bit-interleaving architecture and would suffer more severe soft error [23], [24]. Cross-point SRAM cells [17]–[19] that utilize a row-based word-line (RWL) and column-based write word-line (WWL) to form a cross-point Write structure have been proposed to eliminate Write Half-Select disturb and facilitate bit-interleaving architecture.

In this paper, we present a 40-nm 72-Kb subthreshold SRAM based on our previously proposed disturb-free 9T cell [Fig. 1(a)] [19]. The cell features a dedicated Read port with row-based VVSS control to eliminate Read disturb and mitigate BL leakage, and column-based data-aware WWLA/WWLB to form a cross-point Write structure to eliminate both row and column Half-Select disturb and facilitate bit-interleaving architecture. The 40-nm design employs a ripple bit-line (RPBL) structure that provides an over 40% read access performance improvement for $V_{\rm DD}$ below 0.4 V compared with the conventional hierarchical BL (HBL) structure. A variation-tolerant ripple-initiated negative bit-line (NBL) write-assist scheme with the transient negative pulse coupled only into the single selected local bit-line (LBL) segment is used to enhance the NBL boosting efficiency and reduce power consumption. Fig. 1(b) shows the 9T cell layout in UMC 40-nm low-power (40LP) CMOS technology. The cell size is $0.82\,\mu{\rm m} \times 1.03\,\mu{\rm m} = 0.8446\,\mu{\rm m}^2$ using standard logic rule, which represents a 0.48$\times$ shrink from our previous design in UMC 65LP CMOS technology with a cell size of $1.535\ \mu{\rm m} \times 1.155\ \mu{\rm m} = 1.773\ \mu{\rm m}^2$ [19].

II. RPBL Structure

In deeply scaled technology, the wire delay becomes a significant portion of the total delay. Particularly for subthreshold operation [25]–[27]. The HBL structure (Fig. 2) with short LBLs muxed into a long global bit-line (GBL) has been widely used in SRAM design [19]. The weak LBL discharging capability of the 9T cell due to three-stacking NMOS Read buffer and

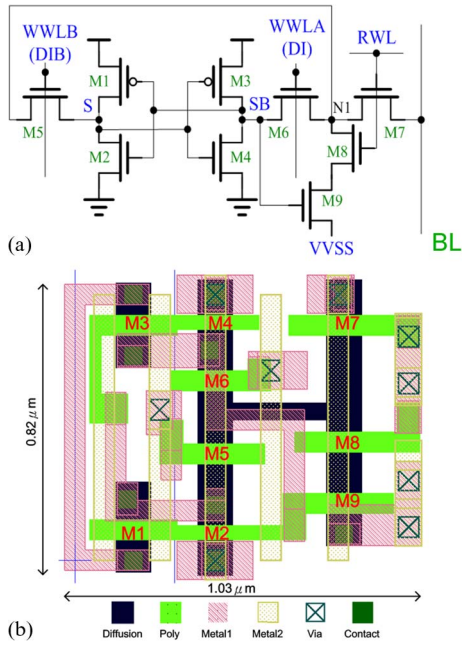

Fig. 1. (a) Schematic of the disturb-free 9T cell [19] and (b) layout of the 9T cell in UMC 40-nm low-power (40LP) CMOS technology.

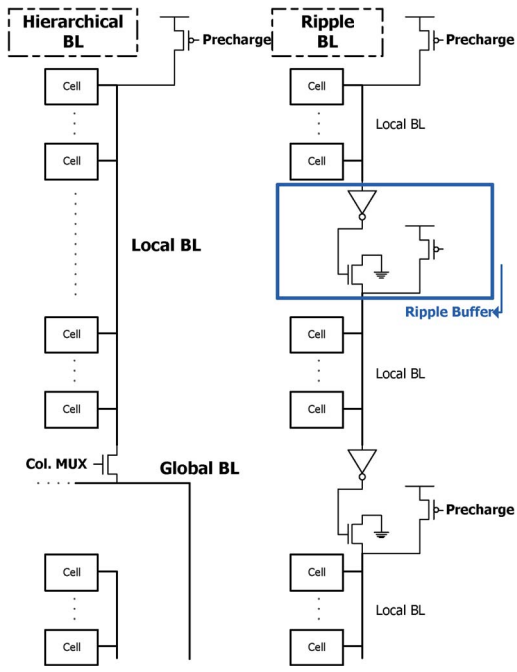

Fig. 2. Conventional hierarchical BL (HBL) scheme and proposed ripple BL (RPBL) scheme. The ripple BL scheme isolates each LBL segment through ripple buffer insertion.

the long GBL result in a long Read access delay. In [28], a "Cascaded bit-line" scheme was proposed, where NMOS pass-gates are used as "BL gates" to isolate the LBL segments, and data from or to the accessed cell is transferred through the cascaded LBLs. The scheme, however, has the drawback of timing control of the "BL Gates." If BL gates open too early, the LBL segment that is presently propagating the signal will see the loading of succeeding LBL segment, thus degrading the performance and power. On the other hand, if BL gates open too late, the delay adds directly to the signal propagation delay through the cascaded LBL segments. This "BL gates" timing problem becomes particularly serious for a subthreshold operation where severe variability may completely undermine its benefits.

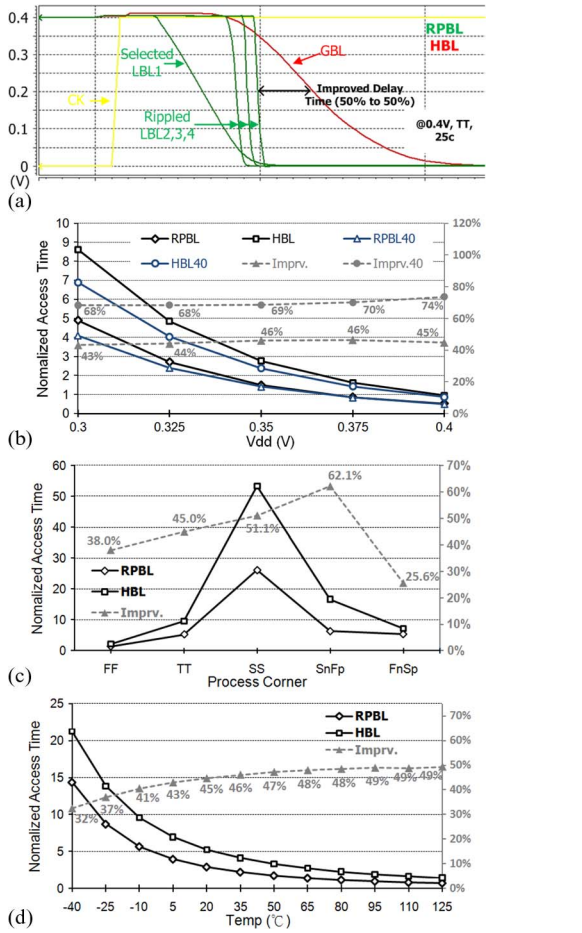

Fig. 3. Comparison of the conventional HBL and the proposed RPBL scheme in UMC 65LP CMOS technology: (a) pertinent sensing waveforms at 0.4 V, TT, 25 °C; (b) Read access delay (Ta) versus VDD at TT, 25 °C, also shown for comparison are the 40LP results (labeled HBL40, RPBL40, and Imprv.40); (c) Ta versus process corner at 0.4 V, 25 °C; and (d) Ta versus temperature at 0.4 V, TT.

The basic structure of the proposed RPBL is shown in Fig. 2. Short LBL segments are isolated by a simple ripple buffer consisting of an inverter and an NMOS. The ripple buffer also serves as local SA for LBL. Sensing signal propagates uni-directionally in domino-like fashion by ripple buffer from segment to segment. Non-active LBL segments are completely isolated at all times. The propagation from segment to segment is automatic without any extra/external timing control. The scheme is easily adaptable with single-ended large-signal sensing and is area efficient. The size of the ripple buffer is easily tunable for performance and power optimization. The static logic circuit-based ripple buffer facilitates low-voltage operation. Each LBL segment is 32 bits long in our implementation.

Fig. 3(a) shows the pertinent waveforms for the Read operation of HBL and RPBL schemes at 0.4 V, TT, 25° in UMC 65LP CMOS technology. The detailed structures for the HBL and RPBL schemes are shown in Fig. 2. The HBL and RPBL schemes are individually optimized for performance. In the comparison of HBL and RPBL, the GBL length is fixed at 128 bits. For the HBL structure, several LBL segments are muxed into the GBL. To shorten GBL length, the GBL (which runs parallel to LBL at a higher layer of metal) starts at the

bottom of the top LBL segment. If the LBL length is 64 bits long, 2 LBL segments are muxed into GBL and the GBL will be $(2-1)\times 64$ bits $=64$ bits long. If the LBL is 32 bits long, 4 LBL segments are muxed into GBL, and the GBL will be $(4-1)\times 32$ bits $=96$ bits long. Hence, 64-bit-long LBL results in 64-bit-long GBL, while 32-bit-long LBL results in 96-bit-long GBL. From detailed SPICE simulations, the latter case (64-bit-long LBL and 64-bit-long GBL) offers better performance and therefore is chosen for HBL structure. The proposed RPBL scheme has four 32-bit-long LBL. The "Selected LBL1" curve represents the voltage waveform of the selected "farthest" (first) LBL segment. The "GBL" curve represents the voltage waveform of GBL in the HBL scheme. For the HBL scheme, the total BL delay comprises the delays through LBL, mux, and GBL. It can be seen that the long GBL and mux loading in the HBL scheme result in slow discharging of GBL. For the RPBL scheme implemented in this 40-nm design, there is no GBL and the sensed signal simply ripples from the "Selected LBL1" (first) segment, through the LBL2/LBL3 (middle) segment, to the LBL4 (last) segment. Notice that the ripple buffers reshape the waveforms, resulting in short delays with fast falling edges through the LBL segments. At TT, 25 °C, the improvement of the Read access delay (measured from 50% of Clock through the entire SRAM critical path to 50% of Data Out) of RPBL ranges from 43% to 46% for $V_{\rm DD}$ ranging from 0.3 V to 0.4 V [Fig. 3(b)]. Also shown for comparison in Fig. 3(b) are the simulation results for the 40LP process. It can be seen that the proposed RPBL scheme provides an even larger performance advantage at 40 nm. Fig. 3(c) shows that for 65LP, at 0.4 V, 25 °C, the Read access delay improvement ranges from about 25% to 62% across process corners. At 0.4 V, TT, the Read access delay improvement ranges from 32% to 49% for temperature ranging from -40 °C to 125 °C [Fig. 3(d)].

As the ripple buffers isolate the individual LBL segments, each LBL segment needs its own Precharge (PMOS) device. During read operation, if the top LBL segment is selected, the (sensed) signal propagates through the entire ripple chain and the Precharge devices for all LBL segments need to be turned off. On the other hand, if a middle LBL segment is selected, the sensed signal propagates (ripples) only through the succeeding LBL segments and only the Precharge devices of the succeeding LBL segments are turned off. The preceding LBL segments remain precharged, thus reducing the power consumption. The details of the precharge circuits are illustrated in Fig. 4. The top LBL segment has the simple Precharge PMOS controlled by the segment selection signal (Block Address Bit 1 Bar, active "Low" when the selected WL address belongs to the LBL1 segment), while the Precharge PMOS's for the middle LBL segments are controlled by the NAND (NAND1) of the signal from the preceding LBL segment and the segment selection signal (Block Address Bit n Bar). Thus, the low-going signal of the preceding LBL segment turns off the Precharge PMOS of the succeeding LBL segment, allowing the sensed signal to ripple through.

III. NBL Write-Assist for Ripple BL Structure

NBL [19] write-assist is employed to improve the write-ability, write margin, and write performance by simultaneously

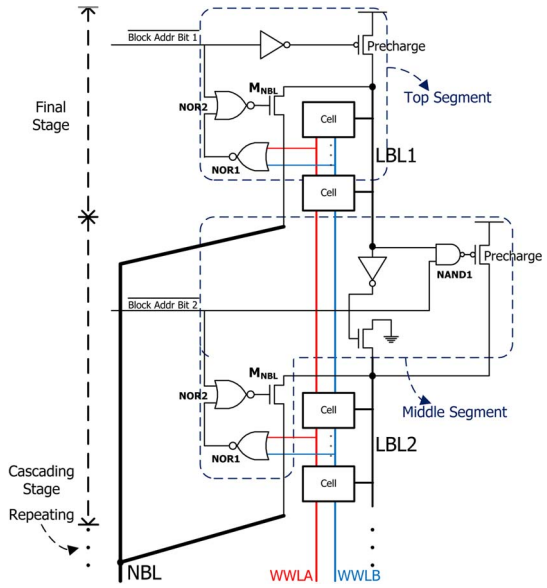

Fig. 4. Details of precharge circuits for the top LBL segment and middle LBL segment, and coupling of negative bit-line (NBL) transient pulse into the selected LBL segment.

enhancing $V_{\rm GS}$ and $V_{\rm DS}$ across the access NMOS. The transient negative pulse is coupled directly into the selected LBL segment, as illustrated in Fig. 4. During the write operation, depending on data-in, either WWLA or WWLB goes high. The high-going WWLA or WWLB is passed through NOR1, and through NOR2 in the selected LBL segment to turn on $M_{\rm NBL}$, thus allowing the transient negative pulse (at NBL) to pass through $M_{\rm NBL}$ into the selected LBL segment. Coupling only into a single selected LBL segment reduces the loading on the NBL circuit (Fig. 5), improves the NBL boosting efficiency, and reduces power consumption. The NBL circuitry and pertinent timing diagram during write operation are shown in Fig. 5. The NBL circuit is shared between an upper block (_U) and a down block (_D). At Standby, both LBL_U (the last segment of LBL in the upper block) and LBL_D (the last segment of LBL in the down block) are precharged high, therefore, the gate of Mnd is at high and node CB is at low. Meanwhile, WEN_U (write enable for the upper block) and WEN_D (write enable for the down block) are both at low, thus conditioning Node CT to high. Once the Write operation commences, either WEN_U or WEN_D goes high, and the low signal at node CB is passed to either NBL_U or NBL_D (depending on whether the upper block or the down block is selected) and fed to node NBL in Fig. 4. This low signal then passes through NOR1, NOR2, and $M_{\rm NBL}$ to pull down the selected LBL segment, ripples down through the succeeding LBL segments in the selected block. When the low signal propagates (ripples) to the last LBL segment in the selected block (i.e., LBL_U or LBL_D), NBL action is activated, Mnd is turned off, and node CT goes from high to low, causing node CB to follow, and the transient negative pulse is passed through either WEN_U or WEN_D to node NBL (Fig. 4) of the selected LBL segment. Note that the NBL action is initiated entirely by the ripple action through the LBL segments in the selected block, thus are tolerant to PVT variations. The area penalty for NBL write-assist, including boosting capacitor and timing/control circuitry, is about 2.5% for the 72-Kb SRAM macro.

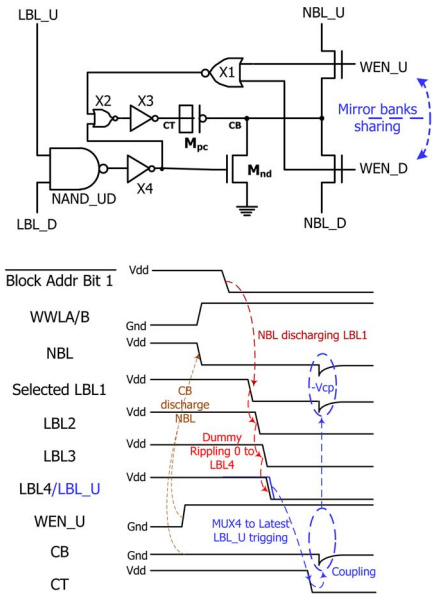

Fig. 5. Ripple-initiated NBL circuitry and pertinent timing diagram during Write operation. $M_{\rm pc}$ is the boosting capacitor implemented with PMOS.

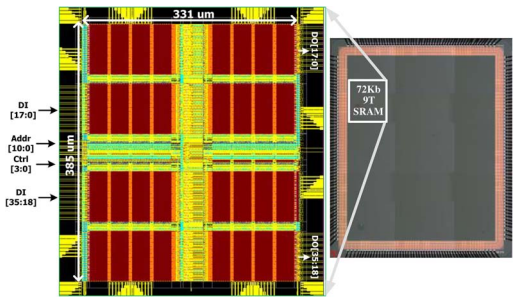

Fig. 6. Die photo (right) and layout view (left) of the 72-Kb test chip in UMC 40-nm low-power (40LP) CMOS technology.

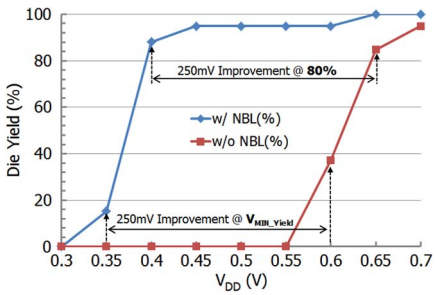

Fig. 7. Measured error-free full functionality die yield versus $V_{\rm DD}$ at room temperature. A total of 59 dies are measured.

IV. Test Chip Implementation and Measurement

Fig. 6 shows the die photo and layout view of the 72-Kb test chip in UMC 40-nm 40LP CMOS technology. The test chip macro consists of 32 array blocks of 72 × 32 bits per block. The design implements bit-interleaving 4 (BL MUX4) architecture to improve soft error immunity and for efficient area sharing of write-assist circuitry in Global IO circuit. The chip size is 331 μm × 385 μm.

Fig. 7 shows the measured die yield versus $V_{\rm DD}$ at room temperature. A total of 59 dies are tested with full suites of SRAM compiler qualification patterns including MATS+, MARCH C-, and MARCH C+ test patterns with all high/low-Read/Write

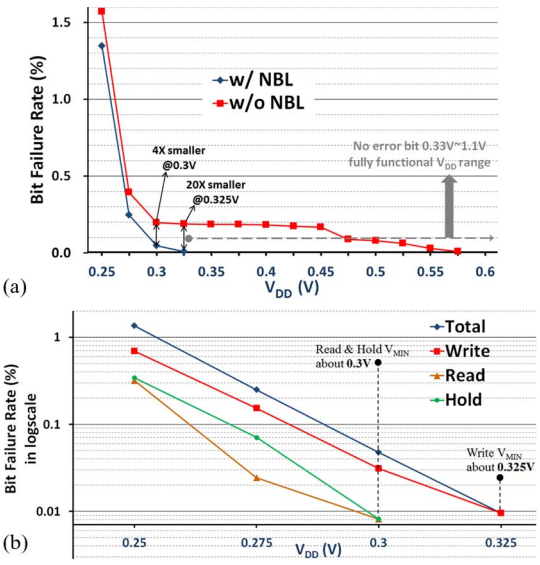

Fig. 8. (a) Measured bit failure rate (BFR) versus $V_{\rm DD}$ and (b) measured Hold, Read, Write, and Total BFR versus $V_{\rm DD}$.

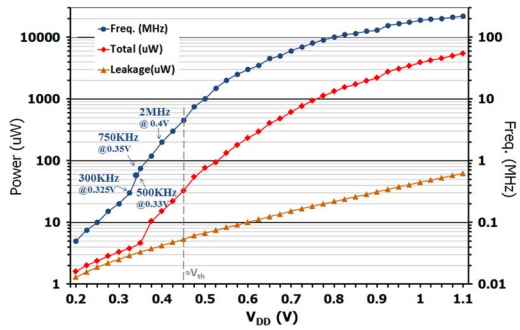

Fig. 9. Measured maximum operation frequency, the leakage power, and total power versus $V_{\rm DD}$.

combinations. The design uses a built-in finite state machine [19] to control the WL pulse width, so the die yield would be the same up to the maximum operating frequency at each $V_{\rm DD}$. With NBL Write-assist, the $V_{\rm MIN}$ improves by more than 250 mV to below 0.35 V. Fig. 8(a) and (b) show the measured bit failure rate (BFR) versus $V_{\rm DD}$. Error-free full functionality is achieved from 1.5 V down to 0.33 V without redundancy. At 0.325 V, only single bit error is observed. At 0.3 V, the BFR is less than 0.1%. With NBL Write-assist, the BFR is reduced by 20× at 0.325 V and by 4× at 0.3 V. The Write $V_{\rm MIN}$ is 0.325 V, and the Read/Hold $V_{\rm MIN}$ is 0.3 V.

Fig. 9 shows the measured maximum operation frequency, the leakage power, and total power versus $V_{\rm DD}$. The maximum operation frequency is 220 MHz (500 kHz) at 1.1 V (0.33 V) and 25 °C. The measured total power consumption is 3.94 μW at 0.33 V, 500 kHz, and 25 °C. Fig. 10 shows the measured Shmoo plot. The characteristics of the chip is summarized in Table I.

V. Conclusion

We presented a 72-Kb 9T subthreshold SRAM with a RPBL structure and ripple-initiated NBL Write-assist. The RPBL scheme provided over 40% Read access performance improvement at low $V_{\rm DD}$ compared with the conventional HBL structure. The variation-tolerant ripple-initiated NBL Write-assist

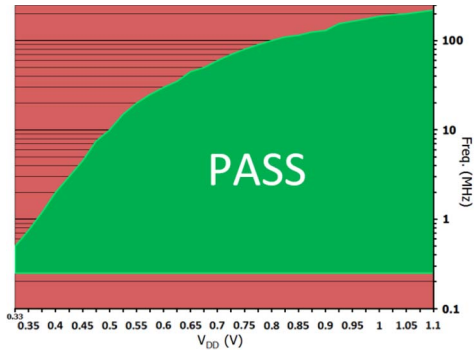

Fig. 10. Measured frequency-voltage Shmoo plot of the 72-Kb RPBL test chip.

TABLE I
FEATURE OF THE 72-Kb TEST CHIP

Technology	UMC 40nm LP CMOS
SRAM Macro Area	331 x 385 μ m^2
Fully Functional V_{DD} Range	0.33 V~1.5 V
Write V_{MIN}	≈ 0.325 V
Read/Hold V_{MIN}	≈ 0.3 V
Operation Frequency	500 KHz @ 0.33 V
Total Power	3.94μ W @ 0.33 V
Leakage Power	3.00μ W @ 0.33 V
ALL Measurements @ Room Temperature 25 ℃	

with the transient negative pulse coupled only into the single selected LBL segment enhances the NBL boosting efficiency and reduces power consumption. Implemented in UMC 40-nm LP CMOS technology, the test chip achieved error-free full functionality without redundancy from 1.5 V down to 0.33 V. The measured maximum operation frequency was 220 MHz (500 kHz) at 1.1 V (0.33 V) and 25 °C. The measured total power consumption was 3.94 μW at 0.33 V, 500 kHz, and 25 °C.

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