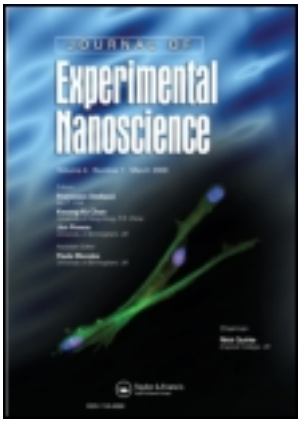

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Nickel nanocrystals (NCs) embedded flash memory structure with SiO_2 tunnelling and pulsed laser deposition grown Al_2O_3 blocking oxide is reported here. The post-deposition thermal annealing of an ultrathin (~5 nm) nickel film evaporated on thermally grown SiO_2 tunnelling barrier has been performed to form the nickel NCs. The formation of tiny nickel NCs is confirmed from the high-resolution transmission electron microscope micrographs. The electrical capacitance–voltage (C–V) characteristics of the optimised 1000°C, 5 min annealed sample shows a large memory window of 20 V at ±20 V sweeping voltage. The charge storage properties are found to be significantly improved as compared to control samples. The frequency dependent C–V measurements indicate the dominant charge trapping in Ni NCs, making the memory structure attractive for use in future nanoscale high-performance applications.

Keywords: non-volatile flash memory; nickel nanocrystals; PLD; electrical measurement; large memory

1. Introduction

Memory elements with higher density, faster read/write cycles and lower power dissipation are required for next generation electronic systems. Therefore, significant attention has been paid to the development of different types of non-volatile memory such as nanocrystals (NCs) flash memory, magnetoresistive random access memory, phase change memory, resistive switching memory, etc., which are comparable in speed and capacity to volatile random access memory [1–16]. As the devices are scaled down, non-volatile flash memory devices employing conventional floating gates as charge storage nodes have faced the stringent leakage and reliability challenges. NC floating gates, embedded between the blocking and tunnelling oxides, can significantly improve the non-volatile charge retention time due to the Coulomb blockade effect, quantum confinement and the reduction of charge leakage from weak spots in the tunnel oxide [1,3,4]. In addition, floating-gate flash memory structures using NCs can improve flash memory performance in many aspects such as read/write/erase speed, device scaling, device life time and operating power [4]. In order to obtain faster program/erase (P/E) operation in NC memory, a thinner tunnelling oxide is needed. On the other hand, a thicker tunnelling oxide is

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favourable to achieve longer retention time. In order to resolve this problem, several researchers have focused on high-dielectric constant (high-k) materials for tunnel and control oxides [6–9].

Floating gate memory devices with metal NCs [6–9] are superior to the semiconductor one because of the higher density of states around the Fermi level, a wide work function range, smaller energy perturbation due to carrier confinement and stronger coupling with conduction channel [6–8]. The above properties may lead to small operating voltages, provide better cycling and faster write/erase speeds with smaller fluctuations and interface states [3]. Among different metals, Ni has received much attention in CMOS technology for application as a silicide contact [17], trapping layer [6–9] and metal gate electrodes [18]. On the other hand, high-κ materials with a large barrier height, such as Al_2O_3 films are interesting alternatives as a blocking oxide to improve the device performance like lower program/erase voltage and scaling [19–21]. In this article, we report the fabrication and enhanced charge storage characteristics of Ni–NCs embedded memory capacitors using SiO_2 as a tunnelling barrier and pulsed laser deposition (PLD) Al_2O_3 as control dielectrics. The effect of post-deposition annealing (PDA) on the memory characteristics of the capacitors has been studied.

2. Experimental

First, a thin (4 nm) tunnelling oxide (SiO_2) was grown by dry oxidation (900°C, 5 min) on Si (100) substrates with resistivity of 10–20 Ω-cm, after conventional Si cleaning. An intermediate ultrathin nickel layer of 3–4 nm was thermally evaporated on it. Following this, Al_2O_3 blocking oxide (~30 nm) was deposited by PLD using a pure Al_2O_3 target. Control samples without Ni intermediate layer were also prepared for comparison. The schematic structure of the NCs embedded device is shown in Figure 1. The PDA of the samples was performed with the temperature ranging from 900°C to 1000°C in pure N_2 ambient for 5–10 min, to form the Ni NCs. The Al metal gate electrode, having an area $1.75 \times 10^{-4}\,cm^2$ was evaporated on the annealed samples using a metal shadow mask. The microstructural properties of the memory structures were carried out with X-ray diffraction (XRD) using a Philips (X'Pert Pro MRD) diffractometer and high-resolution transmission electron microscope (HRTEM) using JEOL JEM-2100F system operated at 200 kV. Electrical memory and leakage current characteristics were studied using a Keithley 4200 SCS semiconductor analyser system.

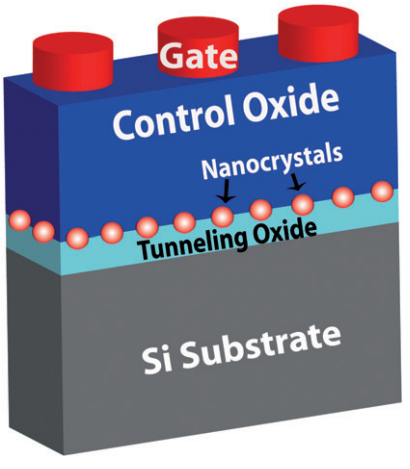

Figure 1. Schematic structure of the tetralayer MOS capacitors.

3. Results and Discussions

Figure 2 shows the grazing angle XRD patterns of the as-deposited and annealed samples. The peak at an angle 56.6° corresponds to Ni_2O_3 (202) and peaks at 57.8°, 59.3° corresponds to Al_2O_3 (116) and (221). The broadness of the peaks increases with increasing annealing temperature representing the enhanced crystallinity of Ni_2O_3 in the samples, as shown in Figure 2(b). A core shell structure of nickel surrounded by nickel oxide is formed after high temperature annealing [6,17,22].

Plane-view HRTEM study of the grown samples was carried out to examine the formation of Ni NCs on post-growth annealing of the middle Ni layer. Figure 3 shows the surface morphology of the Ni film on SiO_2 after annealing at 1000°C for 5 min. It clearly shows the formation of isolated nickel NCs. The average diameter of the NCs (at lower annealing temperature 950°C, 5 min) varies from 6 nm to about 22 nm having a Gaussian size distribution (not shown here), with the maximum number of NCs ($3.5 \times 10^{13}\,cm^{-2}$) of diameter 12 nm. A much improvement in the uniformity of size distribution is observed on increasing the annealing temperature to 1000°C. We observed a uniform distribution of the NCs with smaller size on annealing the films at 1000°C for 5 min, as shown in the plane-view HRTEM micrograph in Figure 3. Figure 3(a) shows the low-resolution view, whereas Figure 3(b) shows the high-resolution micrograph of the films. The high magnification HRTEM image of a single Ni NC is shown in the inset of Figure 3(b). The lattice fringes appearing in the single crystal domain exhibit *d*-spacing of 0.12 nm corresponding to the {2 2 0} lattice spacing of nickel. The average diameter of the NCs ranges from 3 to 6 nm, having a large number of NCs of about $1.3 \times 10^{14}\,cm^{-2}$ with size 4 nm, as shown in Figure 3(c). The spacing between the NCs is in the order of 2–5 nm. The coalescence of NCs is observed with further increase in the annealing time to 15 min at 1000°C. Due to agglomeration, size of the NCs increases and the NC density decreases (not shown here).

High frequency (1 MHz) C–V characteristics with different voltage sweeps of the optimised (1000°C, 5 min annealed) memory device are shown in Figure 4. The measurements were taken at room temperature by sweeping the gate voltage (±5 to ±20 V) from accumulation to inversion region and then sweeping back. A very small hysteresis width is observed for the control and as-deposited samples compared to the NCs embedded one. The maximum memory window of 20 V at the sweeping voltage of ±20 V is reproducibly observed in 1000°C, 5 min

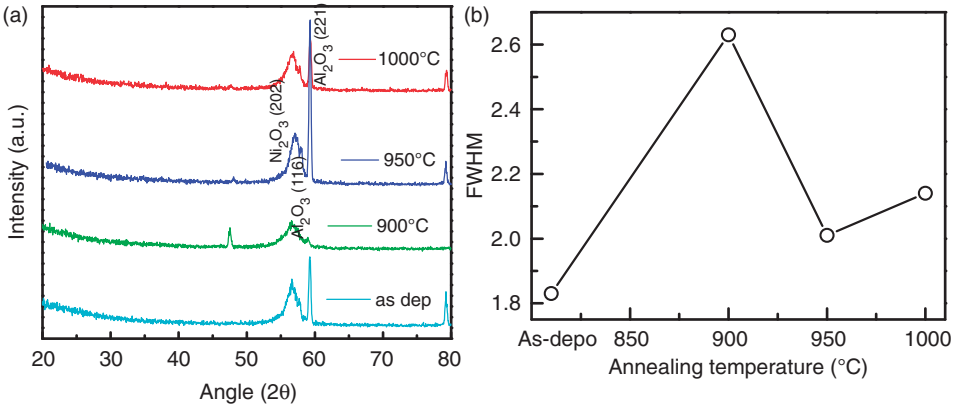

Figure 2. (a) XRD spectra of the memory structure annealed under different conditions and (b) variation of FWHM from the XRD spectra of Ni_2O_3 peak of the different samples.

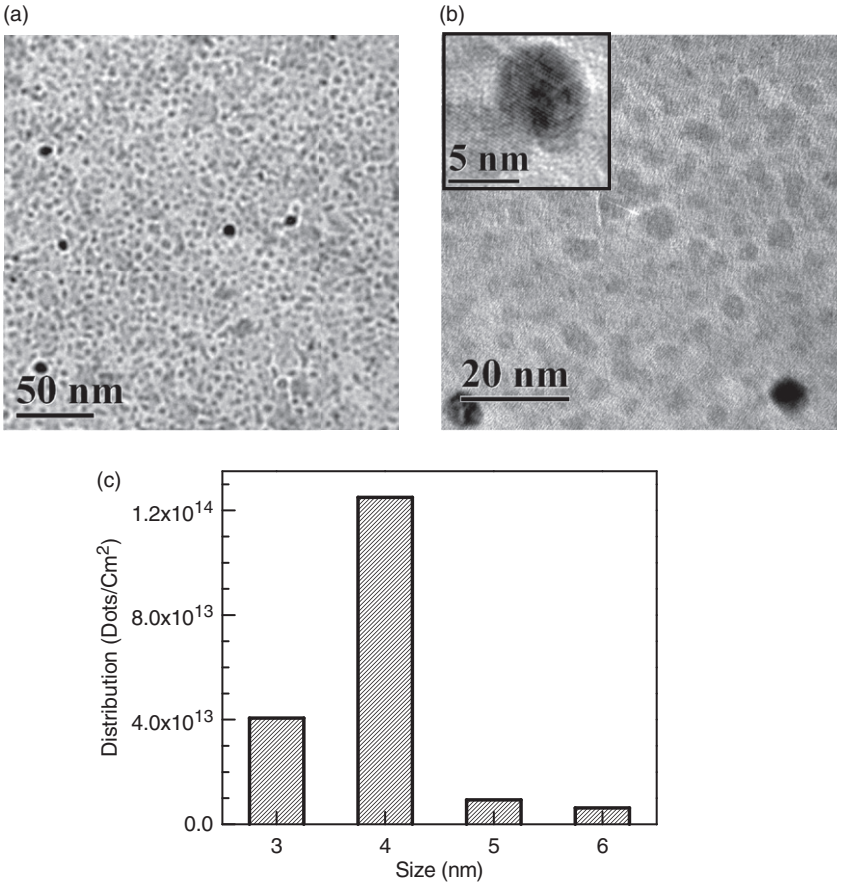

Figure 3. Plane view HRTEM image of the 1000°C, 5 min annealed nickel NCs (a) Low-resolution view (b) high-resolution view; inset shows the single nickel NCs and (c) size distributions.

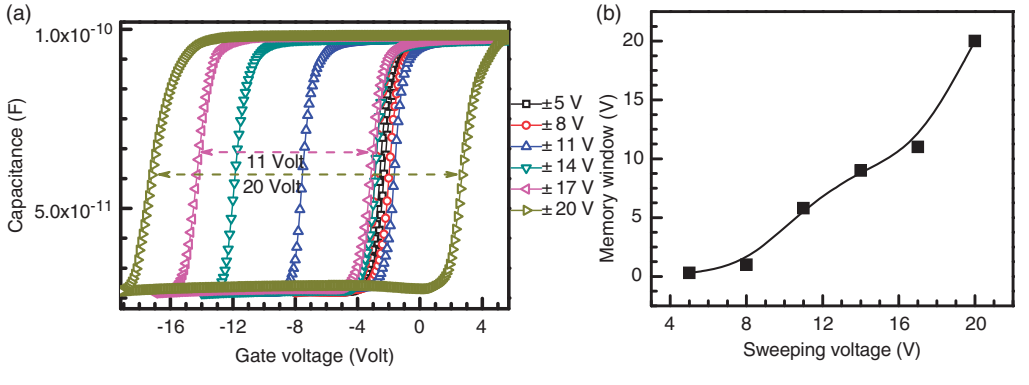

Figure 4. (a) C–V characteristics of 1000°C, 5 min annealed nickel NCs embedded MOS devices with different sweep voltages and (b) variation of memory window with the sweeping voltage of this sample.

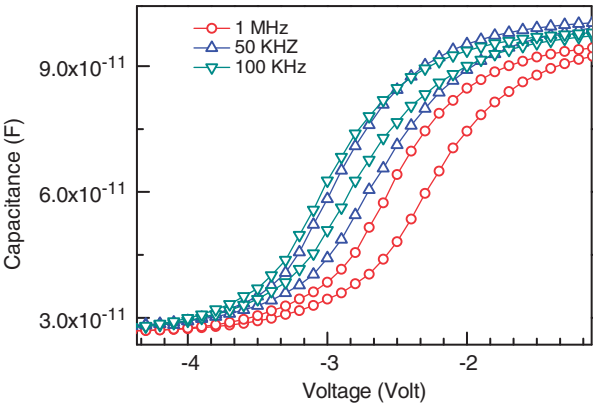

Figure 5. Frequency dependent C–V curve of the 1000°C, 5 min annealed nickel NCs embedded MOS devices.

annealed sample, because of the charge trapping in tiny isolated nickel NCs. At a lower annealing temperature (950°C for 5 min), the memory window decreases. From Figure 4, we also notice that a very small memory window is observed at ±5 and ±8 V sweep. This is due to the larger thickness of oxide dielectrics. During programming, the electrons are injected to the NCs by tunnelling from the substrate through tunnelling SiO_2. Whereas during erase process, the electrons are returned back to the substrate on applying opposite bias. The rate of electron tunnelling strongly depends on the electrical field across the oxide. It needs more potential to tunnel electrons at higher oxides thickness, which results in smaller memory window at low bias. All the samples exhibit clockwise C–V hysteresis loops, indicating the electron injection from substrate to the charge trapping layer containing Ni NCs [6,8]. The MOS structures without Ni–NCs showed very small memory window (almost no memory effect) indicating that the charge trapping is solely due to the Ni NCs. At a relatively low-sweep bias, the flat band voltage is shifted along the negative voltage axis with respect to an ideal MOS structure. The shift increases with the increase of sweep voltage, which indicates the existence of fixed charges in the Al_2O_3/Al or SiO_2/Si interface. The variation of memory window as a function of the sweeping voltage is shown in Figure 4(b). On increasing the sweeping voltage from ±5 to ±20 V, the memory window increases from 0.9 to 20 V. This suggests that the resultant hysteresis may be attributed to the injected trapped charges in Ni–NCs or at the interfaces between the NCs and the surrounding oxides [1–8]. Almost, no memory effect is observed at low sweeping voltage, for the higher thickness of the oxide dielectrics.

In order to confirm that the charge trapping takes place in metal NCs rather than the interface traps, frequency dependent C–V characteristics have been measured from 50 kHz to 1 MHz [22]. Figure 5 shows the frequency dependent C–V curve of the 1000°C, 5 min annealed sample. The C–V measurement has been carried out at ±5 V sweep voltage of this memory structure. As shown in Figure 5, a constant memory width with negligible dispersion is observed as a function of frequency. This indicates that the large memory window in C–V characteristics originates due to the stored charges in Ni NCs in the tetralayer memory structures, rather than the oxide traps. At higher frequency, the maximum capacitance slightly decreases, with the degradation of slope. This is due to the presence of interface states in the tetralayer device structure.

4. Conclusions

In conclusion, Ni NCs embedded MOS capacitors using SiO_2 tunnelling barrier and pulse laser ablated Al_2O_3 control oxide showed superior memory characteristics suitable for nonvolatile flash memory devices. The formation of Ni–NCs by thermal annealing has been confirmed from the HRTEM micrographs. The structural properties of the film have been studied using XRD spectra. The clockwise hysteresis C–V curves of the fabricated MOS structures indicate the charge storage characteristics of Ni–NCs during voltage sweeping. A maximum 20 V flatband voltage shift (±20 V) have been observed for the optimised annealed samples. Frequency dependent C–V confirms the charge storage is due to the trapping in NCs rather than the traps. This tetralayer Ni NC embedded structure appears attractive for high-density nonvolatile memory devices.

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