

FPGA Realization of Space-Vector PWM Control IC for Three-Phase PWM Inverters

Ying-Yu Tzou, *Member, IEEE*, and Hau-Jean Hsu

Abstract—This paper presents a new circuit realization of the space-vector pulse-width modulation (SVPWM) strategy. An SVPWM control integrated circuit (IC) has been developed using the state-of-the-art field-programmable gate array (FPGA) technology. The proposed SVPWM control scheme can be realized using only a single FPGA (XC4010) from Xilinx, Inc. The output fundamental frequency can be adjusted from 0.094 to 1500 Hz. The pulse-width modulation (PWM) switching frequency can be set from 381 Hz to 48.84 kHz. The delay time for the PWM gating signals is adjustable. This SVPWM IC can also be included in the digital current control loop for stator current regulation. The designed SVPWM IC can be incorporated with a digital signal processor (DSP) to provide a simple and effective solution for high-performance ac drives. Simulation and experimental results are given to verify the implemented SVPWM control IC.

Index Terms—FPGA, PWM control IC, space-vector PWM.

I. INTRODUCTION

OWING to the rapid progress in motor control and microelectronics technologies, the development of universal ac drives has become a major trend. Although most ac drives [ac servo drives or universal pulse-width modulation (PWM) inverters] in use today adopt microprocessor-based digital control strategy, implementation of current control loop and PWM control are still tied to analog control circuitry, as Fig. 1(a) depicts. This kind of control scheme possesses the advantage of fast dynamic response, but suffers the disadvantages of complex circuitry, limited functions, and difficulty in circuit modification.

The rapid development in high-performance low-cost digital signal processors (DSP's) [1], [2] has encouraged research on digital PWM control [3], [4] and digital current control [5] for ac drives. Fig. 1(b) illustrates a typical control architecture of a DSP-based ac drive. This control scheme has the advantages of simple circuitry, software control, and flexibility in adaptation to various applications. However, generating PWM gating signals and current control loops requires a high sampling rate to achieve a wide bandwidth performance. Therefore,

most computation resources of the DSP must be devoted to generating the PWM signals and executing of current control algorithms [6]. As a result, only limited functions are left for other control loops and functions. Although the employment of a further DSP can resolve the problem, additional hardware and software design for such a dual-DSP controller will complicate the design process enormously [7].

Dynamic and ever progressing change in very large-scale integration (VLSI) technology has radically affected the design process. The life cycle of modern electronic products may be even shorter than the design cycle. Therefore, the need for rapid prototyping poses a design challenge. In recent years, the development of application-specific integrated circuit (ASIC) technology has made it possible to integrate complex analog and digital circuits by utilizing the libraries of basic circuit cells [8], [9].

The ASIC approach provides a rapid low-cost manufacturing solution for IC's with special applications. For sophisticated technology linked to a medium-size marketing requirement, it is an optimal solution. However, the longer lead time and higher setup cost for prototyping render it inappropriate for product development in the early stage. Since the 1980's, ASIC technology has given rise to several new specialized technologies, including mask-programmable gate array, cell-based IC (CBIC), programmable array logic (PAL), and field-programmable logic array (FPLA).

With the advancement of the various technical aspects of ASIC, three major categories have been categorized: CBIC, gate array, and programmable logic device (PLD). The CBIC has the longest lead time with the highest number of gates, while the PLD allows the user to define the gate connections, but with the lowest number of gates. The field-programmable gate array (FPGA) is a new PLD developed by Xilinx, Inc. [10], [11]. The FPGA comprises thousands of logic gates, some of which are grouped together as a configurable logic block (CLB) to simplify higher level circuit design. The interconnections of the gates are defined by external SRAM or ROM. The simplicity and programmability of FPGA designate it as the most favorable choice for prototyping an ASIC. The advent of FPGA technology has enabled rapid prototyping of digital systems.

PWM dc-ac converters may serve a wide range of applications in ac motor drives and ac power conditioning systems. The PWM strategy plays an important role in the minimization of harmonics and switching losses in these converters, especially in three-phase applications. In the past

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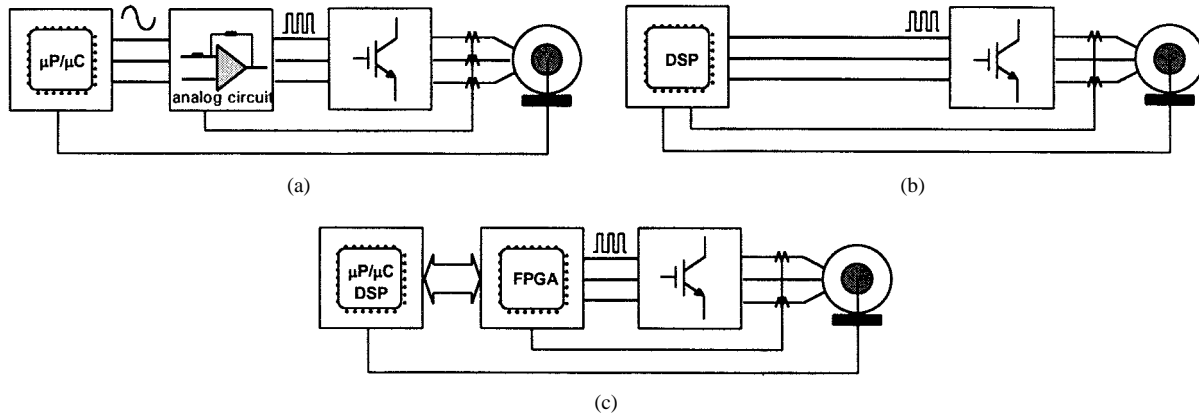


Fig. 1. PWM control structures of digital ac drives: (a) analog, (b) DSP-based digital control, and (c) ASIC/FPGA-based digital control.

two decades, various PWM strategies, control schemes, and realization techniques have been developed [4], [12]–[17]. These PWM strategies were realized either by analog circuit or microprocessor-based software control techniques. However, with the advance of high-frequency switching power devices, complex modulation schemes can no longer be realized, even employing the most advanced digital signal processors, because of the high-speed switching requirement. In recent years, motor control and power conversion IC's employing ASIC/FPGA technology are receiving increased attention [18]–[21]. Fig. 1(c) illustrates a DSP and ASIC/FPGA-based digital ac drive control structure. This type of hardware architecture will become the major control scheme for advanced ac drives.

Employing FPGA to realize PWM strategies provides advantages such as rapid prototyping, simple hardware and software design, higher switching frequency, and relieving the computation load of microprocessors. Realization of the SVPWM schemes by state-of-the-art FPGA technology has so far still not been reported in the literature. This paper proposes a new DSP/FPGA-based control structure for ac drives depicted in Fig. 2 and develops a novel digital circuit realization scheme for the SVPWM control IC employing a single FPGA (4010) from Xilinx, Inc. The designed SVPWM IC may serve either for ac motor drives or three-phase ac-voltage regulation systems. It can also be incorporated as part of the digital current loop for ac motor drives. Fig. 3 shows the circuit configuration of a DSP-controlled ac drive using the SVPWM control IC. The rest of this paper is organized as follows. Section II briefly introduces the principle of the space-vector PWM method. Section III discusses developing a strategy for FPGA-based SVPWM IC and gives a detailed description of the digital circuit realization scheme for SVPWM. Section IV describes the hardware implementation and experimental results. Section V is the conclusion.

II. PRINCIPLE OF SPACE-VECTOR PWM

The major purpose of the PWM inverter is to generate a variable-voltage variable-frequency (VVVF) three-phase voltage to the ac motor such that the resulted rotating magnetomotive force (mmf) will suffer a minimum of harmonics

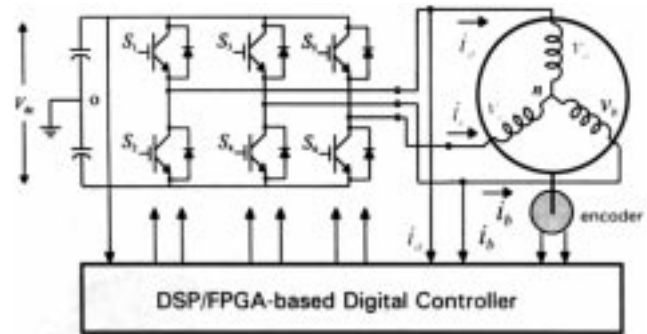


Fig. 2. Circuit schematics of a voltage-source full-bridge three-phase PWM inverter.

distortion. Conventional sinusoidal PWM employs different sampling methods with sinusoidal signals according to a carrier signal, e.g., natural sampling [12], [13], or (symmetric or asymmetric) regular sampling [14].

The operational principle of the space-vector PWM (SVPWM) is more clearly explained by representing a space vector [22]. The motor stator voltage vector can be expressed as a combination of the inverter output-phase voltage v_a , v_b , and v_c , which can be expressed in vector form as

$$\vec{v}_s = v_a + \gamma^2 v_b + \gamma v_c, \quad \gamma = \exp\left(j\frac{2\pi}{3}\right) \quad (1)$$

where

$$\begin{aligned} v_a &= V_m \sin \omega t \\ v_b &= V_m \sin(\omega t - 120^\circ) \\ v_c &= V_m \sin(\omega t + 120^\circ) \end{aligned}$$

and V_m is the amplitude of the fundamental component. As Fig. 4(a) illustrates, there are eight basic switching configurations of the three-phase PWM inverter. Their corresponding voltage vectors are depicted in Fig. 4(b), expressed as

$$v_n = \frac{2}{3} V_d \exp\left[j\frac{(n-1)\pi}{3}\right] \quad (2)$$

where V_d is the dc-link voltage and $n = 1, 2, \dots, 6$ and $v_0 = v_7 = 0$.

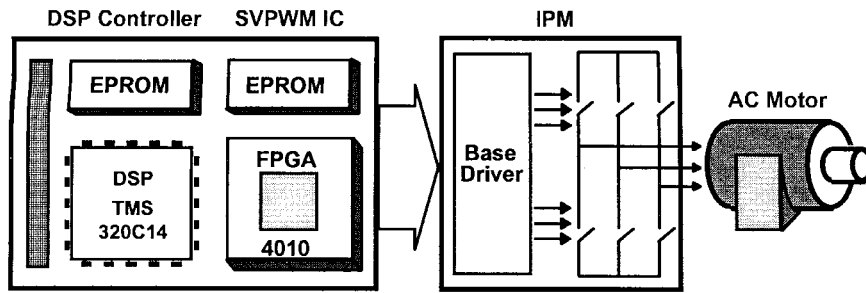


Fig. 3. Circuit configuration of the DSP-controlled FPGA-based PWM current controller for the ac drive.

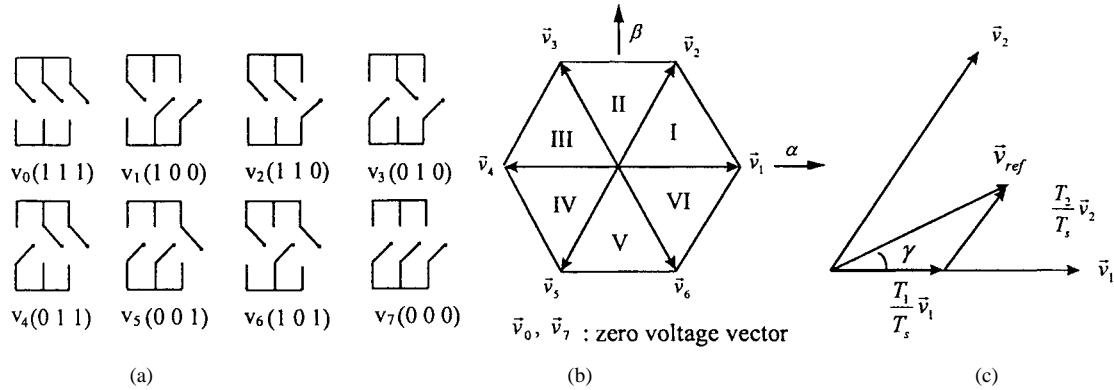


Fig. 4. (a) The switching configurations of a three-phase PWM inverter, (b) corresponding vectors, and (c) decomposition of the voltage vector.

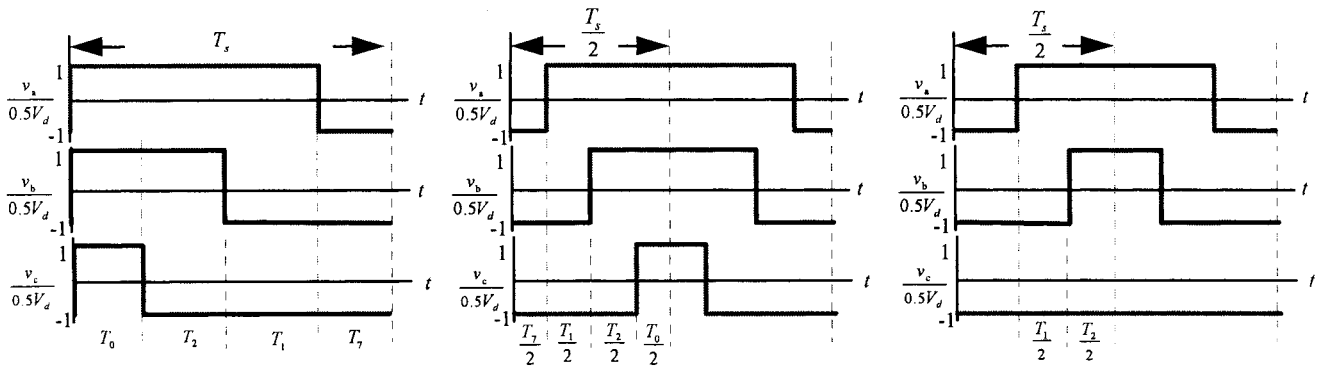


Fig. 5. Equivalent PWM switching patterns generated from three-phase duty ratios to produce same flux vector.

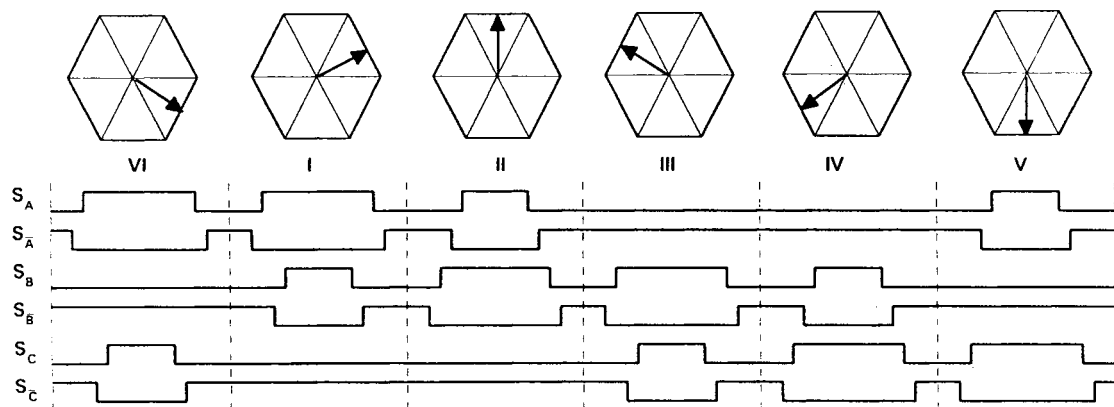


Fig. 6. PWM gating signals of the SVPWM operating at each section.

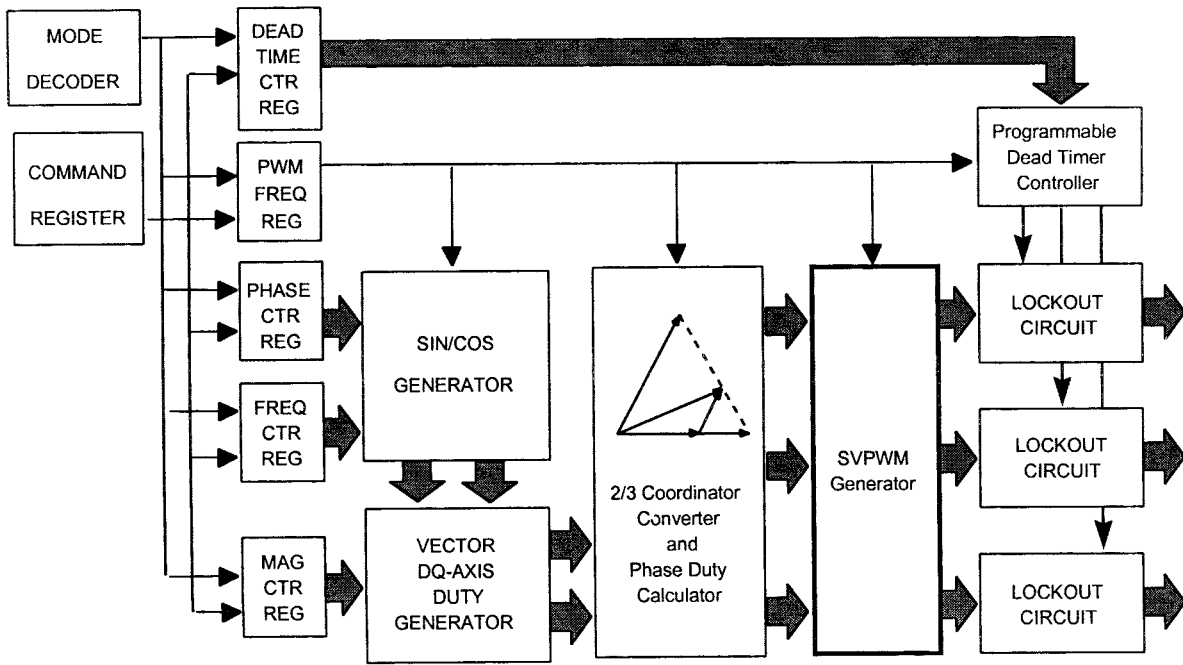


Fig. 7. Functional block diagram of the programmable FPGA-based SVPWM IC.

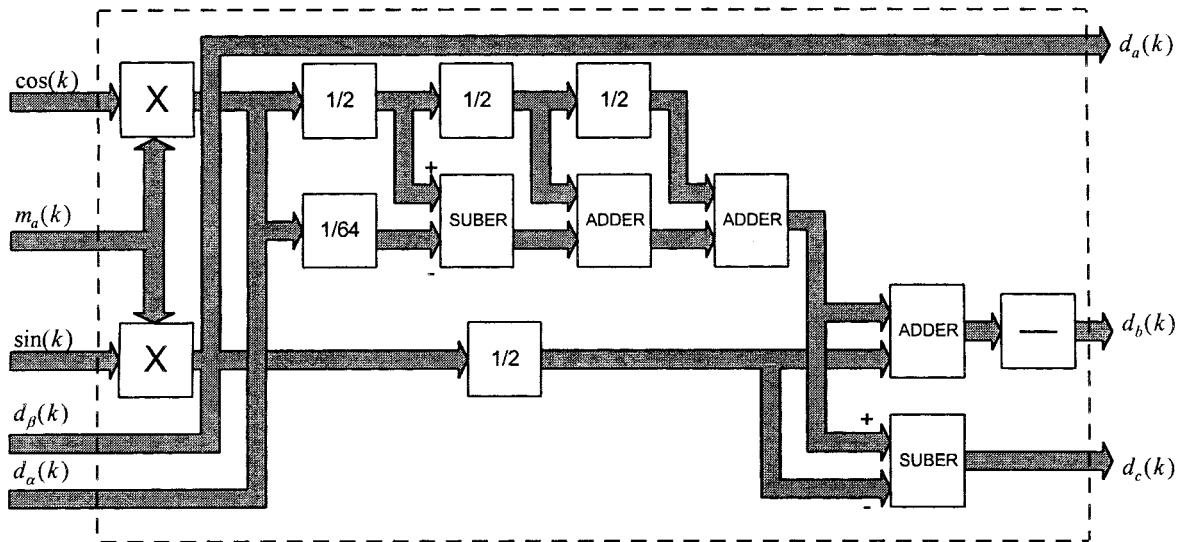


Fig. 8. 8-b circuit realization of the 2-axis-three-phase voltage converter.

The stator voltage vector can be decomposed into two orthogonal components in a two-axis coordinate or as a combination of two basic vectors, as Fig. 4(b) indicates. An example of the voltage vector decomposition is given in Fig. 4(c). The SVPWM strategy aims to minimize harmonic distortion in the current by selecting the appropriate switching vectors and determining of their corresponding dwelling widths.

If the reference vector is located in sector I, then it is composed of voltage vector v_1 , v_2 , and zero voltage vectors v_0 and v_7 as illustrated in Fig. 5(a). The flux produced by the reference voltage vector in a PWM switching period is a combination of each individual flux resulted by its corresponding

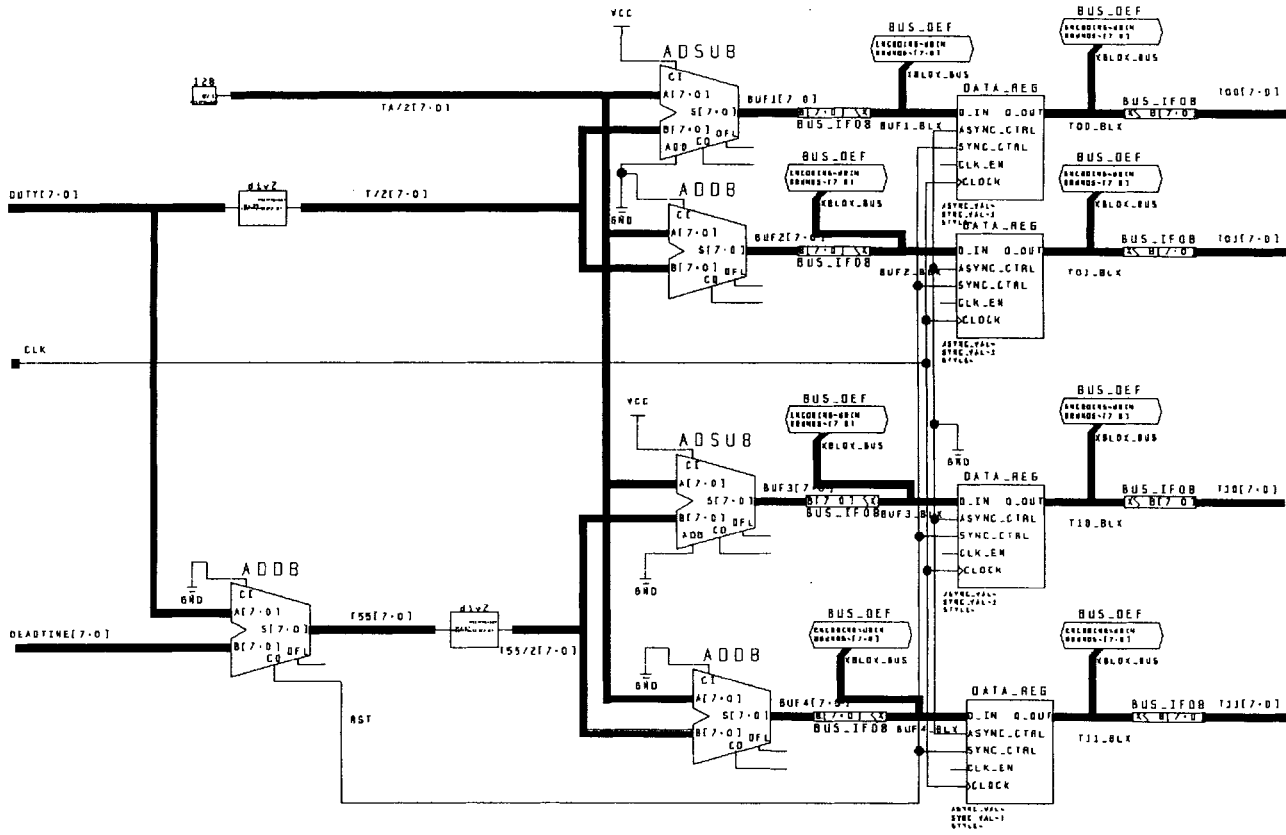
voltage vector. Their relationships can be expressed as

$$\int_0^{T_s} v_{ref} dt = \int_0^{T_0} v_0 dt + \int_{T_0}^{T_1} v_1 dt + \int_{T_1}^{T_2} v_2 dt + \int_{T_2}^{T_7} v_7 dt. \quad (3)$$

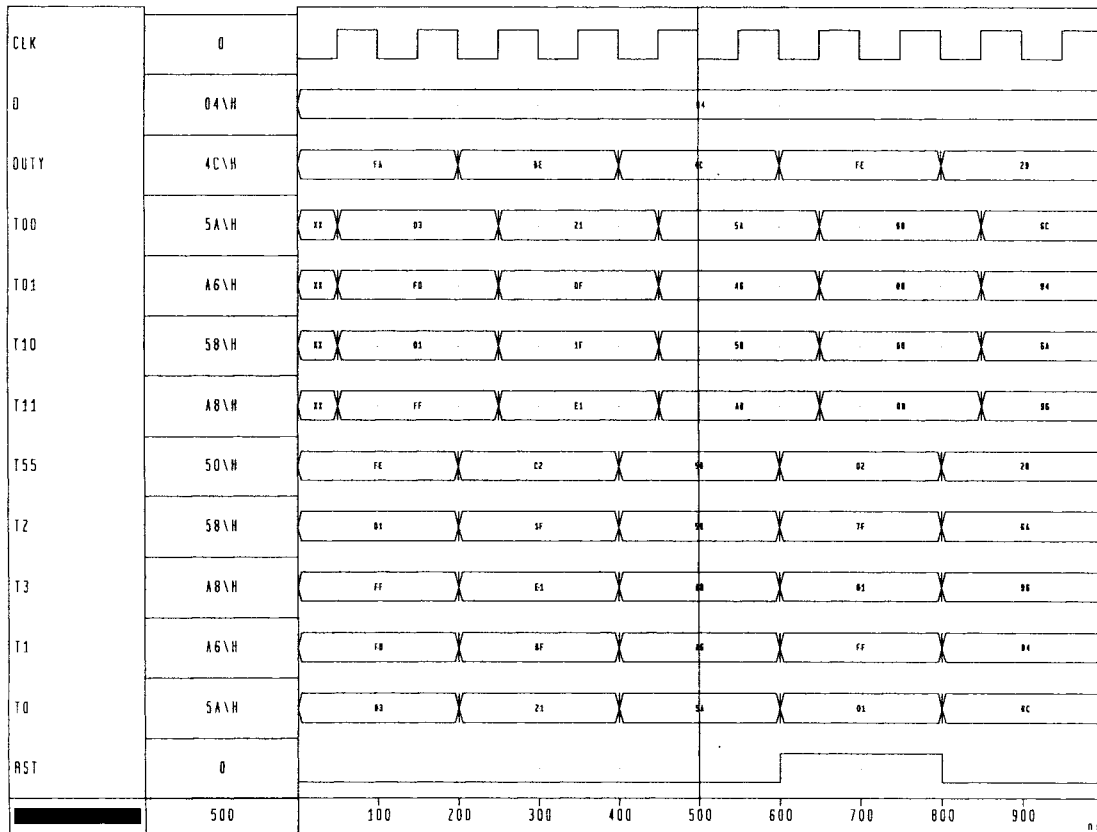
Because the voltage vectors v_1 and v_2 are basic vectors and v_0 and v_7 are zero vectors, this gives

$$v_{ref} = v_1 \frac{T_1}{T_s} + v_2 \frac{T_2}{T_s} \quad (4)$$

where T_s is the switching period and T_1 and T_2 are the dwelling time for v_1 and v_2 , respectively. This voltage space



(a)



(b)

Fig. 9. (a) Schematics of the voltage vector to three-phase PWM duty ratio converter and (b) simulation results.

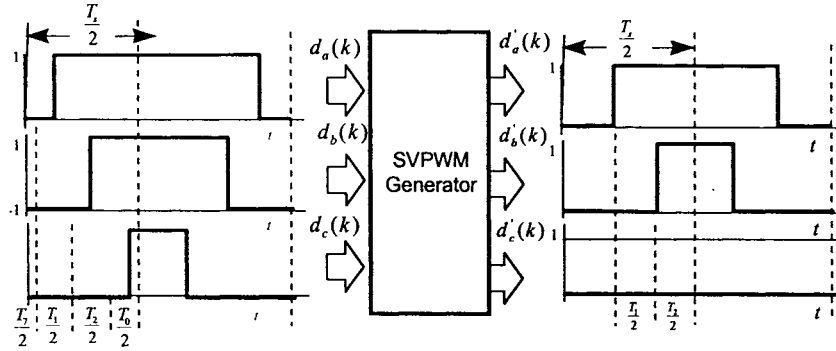


Fig. 10. The centralized encased three-phase PWM waveform converter.

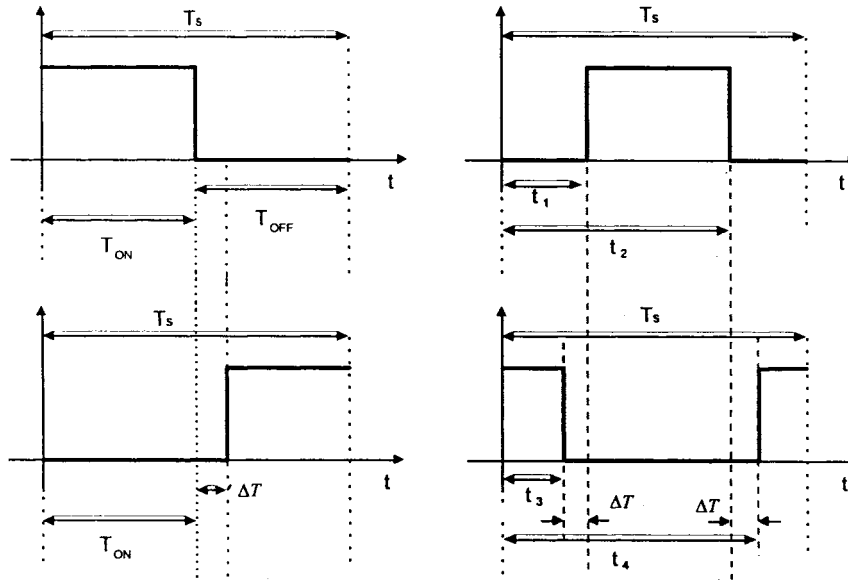


Fig. 11. Timing diagram of the PWM signals with delay time.

vector can be described in rectangular coordinates as follows:

$$T_1 \cdot \sqrt{\frac{2}{3}} V_d \cdot \begin{bmatrix} 1 \\ 0 \end{bmatrix} + T_2 \cdot \sqrt{\frac{2}{3}} V_d \cdot \begin{bmatrix} \cos 60^\circ \\ \sin 60^\circ \end{bmatrix} = \frac{T_s}{2} \sqrt{\frac{2}{3}} V_d \cdot a \cdot \begin{bmatrix} \cos \theta \\ \sin \theta \end{bmatrix} \quad (5)$$

where $a = |v_{ref}| / \sqrt{2/3} V_d$, $0 \leq \theta \leq 60^\circ$, and V_d is the dc-link voltage. From (5), we can obtain

$$T_1 = \frac{T_s}{2} \cdot a \cdot \frac{\sin(60 - \theta)}{\sin 60^\circ} \quad (6)$$

$$T_2 = \frac{T_s}{2} \cdot a \cdot \frac{\sin \theta}{\sin 60^\circ} \quad (7)$$

$$T_7 = T_0 = \frac{T_s}{2} - T_2 - T_1. \quad (8)$$

The equivalent PWM waveforms, which produce the same average flux, may consist of various combinations of the basic vectors. Fig. 5(b) and 5(c) are alternatives to 5(a), producing the same flux. Fig. 5(c) is the optimal synthesis of the flux vector due to its minimum flux ripple and minimum number of switchings. Fig. 6 illustrates the PWM gating signals of the SVPWM scheme in each operation section.

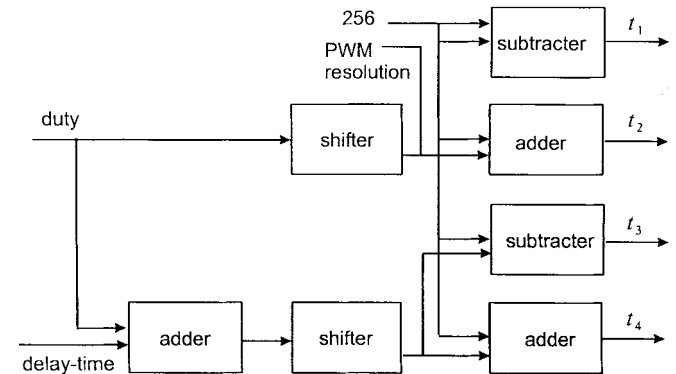


Fig. 12. Circuit block diagram for the generation of the delay time for a single-phase PWM signals.

III. DESIGN OF THE FPGA SVPWM CONTROL IC

In the design of a PWM control IC, many factors need considering, such as simplicity, flexibility, and complexity of the circuit design. In practical applications, the PWM IC should still be compatible with a conventional microprocessor, and, therefore, needs a computer interface. One major design goal is to relieve the microprocessor from time-consuming

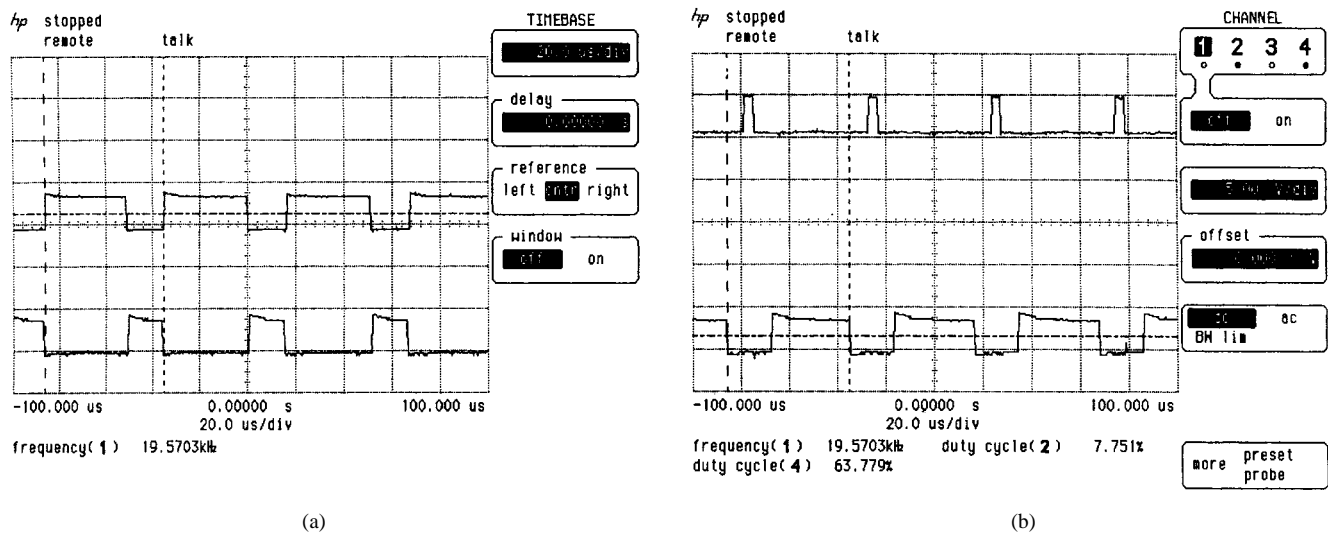


Fig. 13. Experimental results of the programmable delay time with (a) 1.6 and (b) 14.4 μ s, respectively.

TABLE I
SPECIFICATIONS OF THE FPGA 4010

Device	XC4003A	XC4010
Appr. Gate Count	3000	10000
CLB Matrix	10 x 10	20 x 20
Number of CLBs	100	400
Number of Flip-Flops	360	1120
Max RAM Bits	3200	12800
Number of IOBs	80	160
Program Data	45636	178096
PROM Size (bits)	45676	178136

TABLE II
NUMBERS OF CLB ALLOCATION FOR THE SVPWM IC

	CLB function generator	CLB flip-flop
I/O ports	0	40
frequency controller	52	32
amplitude controller	254	0
dead-time controller	180	63
sin/cos generator	37	33
duty-ratio controller	88	0
coordinate converter	241	0
PWM generator	180	63

computational tasks such as PWM signal generation, delay-time compensation, and current control.

Fig. 7 depicts the block diagram of a proposed programmable FPGA-based SVPWM control IC. This design consists of five command registers for settings of the frequency, amplitude, and phase of the stator voltage vector, the switching frequency of the PWM, and the delay time for the power device. To simplify the interface circuit, commands to these registers are routed through a common data bus and decoded by a command mode decoder. The control parameters can be set by externally connected hardware, such as analog-to-digital (A/D) converters, digital switches, or a microprocessor. The internals of the designed SVPWM IC consist of a sin-table address decoder, a duty-ratio calculator, a 2/3-axis converter, a PWM waveform generator, and a programmable delay-time controller.

Determining the pulse width of an SVPWM waveform involves computing of sin function and converting a 2-axis coordinate to a 3-axis coordinate. Therefore, arithmetic com-

putational methods and the bit length for manipulating data are important factors in designing the digital hardware for the SVPWM. Floating-point arithmetic greatly complicates the approach to hardware design; only integer arithmetic can provide a feasible solution. In this paper, 8-b integer arithmetic with an external EPROM-based sin-table reference has been adopted for the digital realization of the SVPWM.

The basic requirements for realizing the SVPWM scheme is to first compute the orthogonal components of the voltage vector. Second, these 2-axis orthogonal components are converted to 3-axis components, and then these three-phase PWM waveforms are converted to centralized encased PWM waveforms with minimal switchings. Finally, the PWM gating signals are inserted with adjustable time delay to protect the phase legs from short circuiting.

The SVPWM IC receives a rotating voltage-vector command with specified amplitude, frequency, and initial phase to produce three-phase PWM gating signals. An external EPROM is required to produce the sin reference used for the PWM duty-ratio generator. The command voltage vector

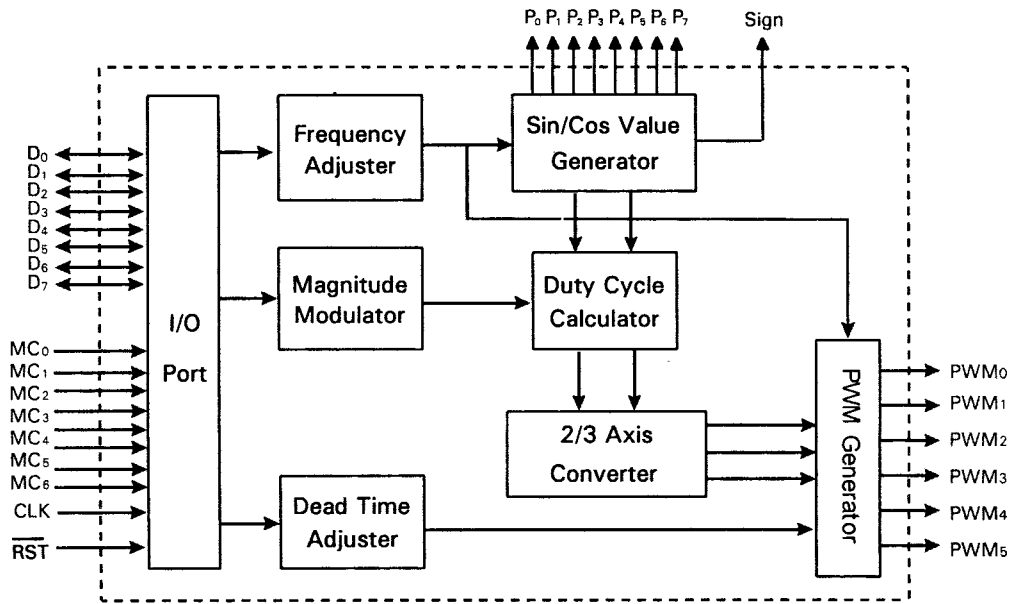


Fig. 14. Pin assignment of the FPGA-based SVPWM IC.

is initially decomposed to two orthogonal vectors $v_\alpha(k)$ and $v_\beta(k)$ in the stationary dq -axis, and then they are converted to corresponding duty ratios $d_\alpha(k)$ and $d_\beta(k)$. The 2- to 3-axis coordinate transformation expressed in duty ratios can be defined as

$$\begin{aligned} d_A(k) &= d_\alpha(k) \\ d_B(k) &= -\frac{1}{2}d_\beta(k) - \frac{\sqrt{3}}{2}d_\alpha(k) \\ d_C(k) &= -\frac{1}{2}d_\beta(k) + \frac{\sqrt{3}}{2}d_\alpha(k). \end{aligned} \quad (9)$$

Exactly calculating (9) requires floating-point arithmetic, which greatly complicates the hardware design. In practical applications, due to the programmable timers, PWM gating signals are usually subject to a resolution limitation. Appropriately determining the PWM control resolution also requires considering the turn-on and turn-off time of the power switches. A 20-kHz PWM switching signal has a switching period of 50 μ s. A 256 resolution of the PWM signal indicates a control clock period of around 0.2 μ s. This period is usually much shorter than the turn-off time of the PWM switches for motor drives and is acceptable in most applications. An integer approximation of the $\sqrt{3}/2$ can be expressed as

$$\frac{\sqrt{3}}{2} = 0.8660 \approx \frac{1}{2} + \frac{1}{4} + \frac{1}{8} - \frac{1}{64} = 0.8594. \quad (10)$$

This approximation results in a 0.76% error for an 8-b integer realization, which corresponds to a 0.38- μ s delay-time error for a 50- μ s switching period. The total switching time of a 20-kHz switching device is usually around several μ s, and, therefore, this truncation error is negligible.

Fig. 8 illustrates the block diagram of an 8-b approximate integer realization of the 2/3 coordinate transformation. Fig. 9(a) is the detailed circuit schematics of the FPGA design of the 2/3 coordinate converter, and Fig. 9(b) illustrates its simulation results.

The three-phase duty ratios of $d_A(k)$, $d_B(k)$, and $d_C(k)$ are then routed to the optimal PWM generator, as Fig. 10 illustrates. The thinking behind this process is to generate PWM waveforms with minimum switchings and the same duty-ratio equivalence. There are two zero vectors, v_0 and v_7 , in the basic switching vectors. However, only one of them should be used during one switching period. Determining the proper zero vector depends on the duration of its dwelling time. The one with the longer dwelling time is selected as the one.

In ideal conditions, the gating signals to the power switches of same phase leg of the PWM inverter should be complementary. However, the turn-off time of a power switch is usually longer than its turn-on time, and, therefore, an appropriate delay time must be inserted between these two gating signals. The length of this delay time is usually about 1.5~2 times the maximum turn-off time. A programmable delay-time controller is included in the designed SVPWM IC, which greatly facilitates its practical applications.

The PWM gating signals and their corresponding delay signals are depicted in Fig. 11. The relationship of the gating signal are as follows:

$$t_1 = \frac{T_s - T_{on}}{2} \quad (11)$$

$$t_2 = \frac{T_s + T_{on}}{2} \quad (12)$$

$$t_3 = \frac{T_s - (T_{on} + \Delta T)}{2} \quad (13)$$

$$t_4 = \frac{T_s - (T_{on} + \Delta T)}{2} \quad (14)$$

where ΔT is the specified delay time. The delay-time controller generates the gating signals to the toggle registers, which includes a digital comparator and results in PWM signals with a specified time delay. Fig. 12 shows the circuit block diagram for the generation of the delay time for single-

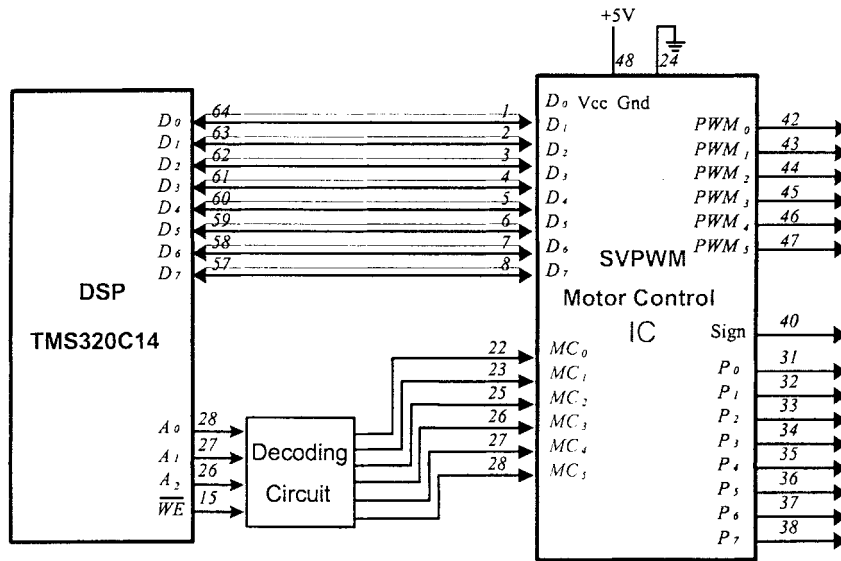


Fig. 15. Circuit schematics of the designed SVPWM IC interface with a single-chip DSP TMS 320C14.

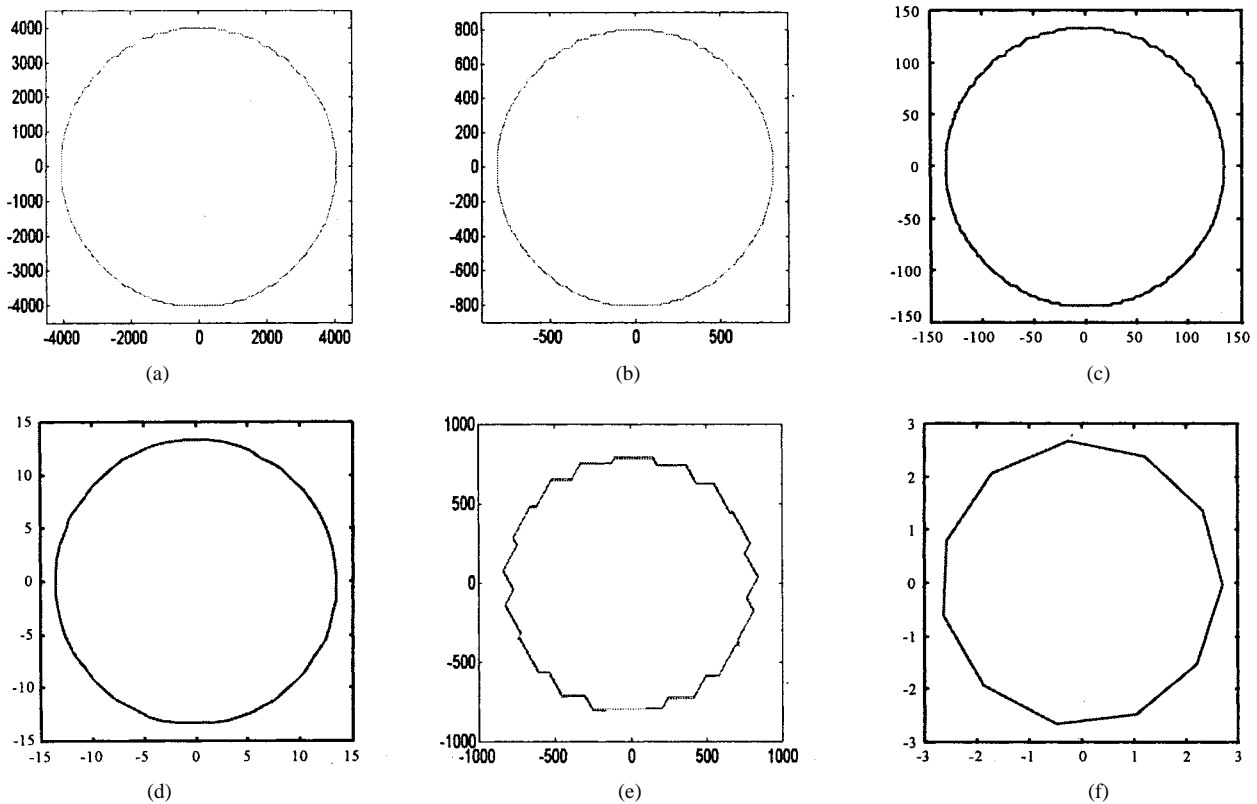


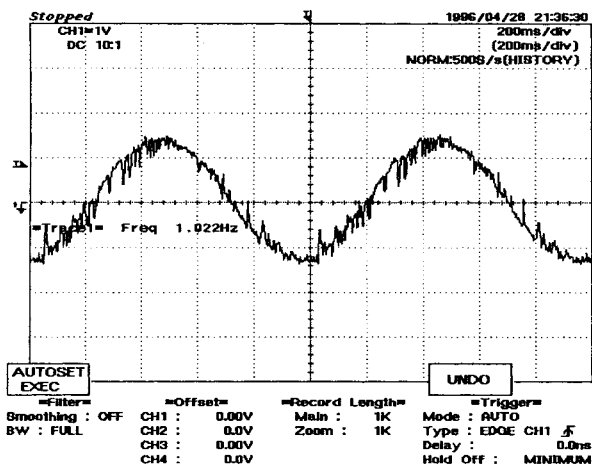
Fig. 16. Experimental results of the voltage vector integration of the SVPWM gating signals at various operation frequencies: (a) 94 MHz, (b) 10 Hz, (c) 60 Hz, (d) 300 Hz, (e) 1000 Hz, and (f) 1500 Hz.

phase PWM signals. Fig. 13 shows experimental results of the programmable delay-time controller with different settings.

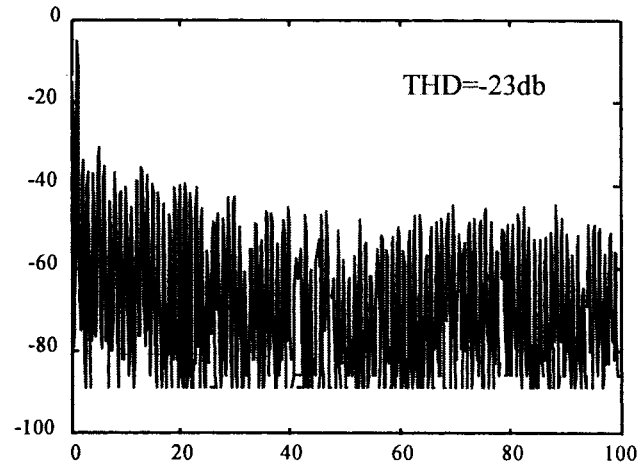
IV. HARDWARE REALIZATION AND EXPERIMENTAL RESULTS

In realizing the proposed SVPWM scheme, cost considerations led to selecting an SRAM-based FPGA XC4010 from Xilinx, Inc. for implementing of the SVPWM IC. The XC4010 has around 10 000 logic gates, 400 configurable logic

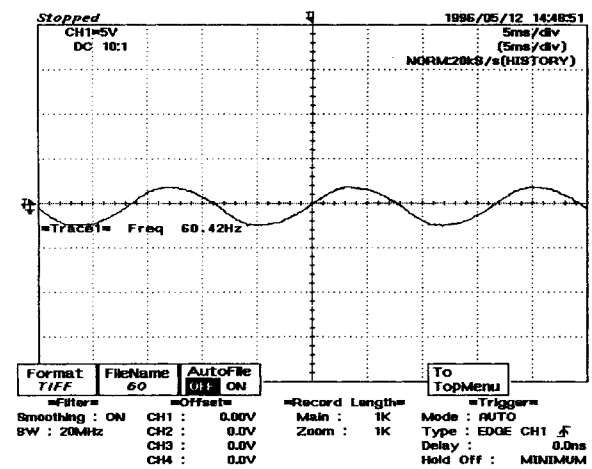
blocks (CLB's), and 160 input/output blocks (IOB's). Some important specifications of the XC4010 are listed in Table I. Xilinx also provides CAD tools (XACT) for the development of ASIC's employing FPGA's. The XACT consists of a schematic entry editor, a cell library, an interface with the schematic entry editor, logic and timing simulation software, and design implementation software. The logic and timing simulation software is especially relevant to the design of



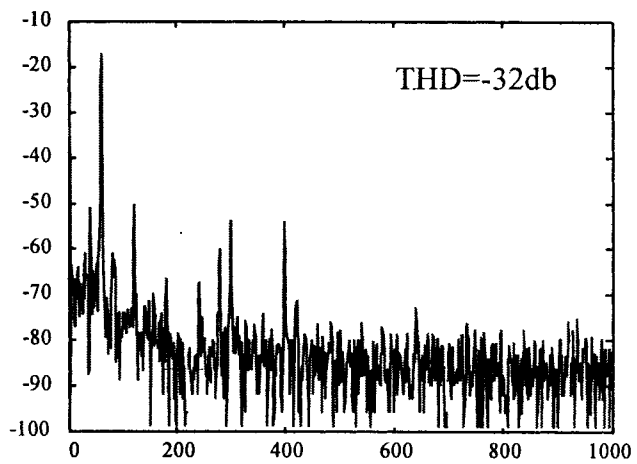
(a)



(b)



(c)



(d)

Fig. 17. Experimental results of the SVPWM IC used in a 1-hp PWM inverter drive with 1- and 60-Hz output: (a) and (c) are the phase currents and (b) and (d) are the corresponding harmonics spectrum.

complicated digital circuits because it is best suited to resolve circuit problems during the early design stage.

In the design of an ASIC employing FPGA, careful placement of the circuit components and their interconnections is state-of-the-art in minimizing of CLB's. The number of CLB's serving each major functional block of the SVPWM IC are listed in Table II. Fig. 14 illustrates the pin assignment of the designed SVPWM IC. Fig. 15 depicts an application of this SVPWM IC employing a single-chip DSP (TMS 320C14) from Texas Instruments. The simplicity in the interface circuit design illustrates its feasibility for practical applications.

Fig. 16 illustrates the experimental results of integrating the voltage vector of the SVPWM gating signals at various operation frequencies. The output fundamental frequency can be adjusted from 0.094 to 1500 Hz. Such a wide frequency control range, with high-frequency switching, is only feasible by utilizing the state-of-the-art VLSI digital circuit design technique. The PWM switching frequency can be set from 381 to 48.84 kHz. The delay time for the PWM gating signals

is adjustable. Fig. 17 shows the experimental results of the designed SVPWM IC used in a PWM inverter ac motor drive with 1- and 60-Hz output, respectively. Experimental results show the constructed SVPWM IC can generate a wide range of output frequencies with controlled fundamental voltage.

V. CONCLUSION

This paper presents the design and implementation of a programmable SVPWM control IC for ac motor drives. This SVPWM control IC was implemented employing the FPGA technology. A static RAM-based FPGA was used to implement the proposed scheme. It can also be included in the digital current control loop for stator current regulation. The SVPWM IC can be incorporated with a DSP to provide a total solution for high-performance ac drives. Simulation and experimental results are provided to verify the implemented SVPWM control IC. The constructed SVPWM IC can generate a wide range of PWM output voltages and frequencies. Given that an economic manufacturing cost can be achieved, it is believed

that such PWM control IC's will become key components in power converters and motor drives of the future.

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