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Investigating the degradation behavior caused by charge trapping effect under DC and AC gate-bias stress for InGaZnO thin film transistor

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This letter investigates the degradation mechanism of amorphous indium-gallium-zinc oxide thin-film transistors under gate-bias stress. The larger V_t shift under positive AC gate-bias stress when compared to DC operation indicates that an extra electron trapping mechanism occurs during rising/falling time during the AC pulse period. In contrast, the degradation behavior under illuminated negative gate-bias stress exhibits the opposite degradation tendency. Since electron and hole trapping are the dominant degradation mechanisms under positive and illuminated negative gate-bias stress, respectively, the different degradation tendencies under AC/DC operation can be attributed to the different trapping efficiency of electrons and holes. © 2011 American Institute of Physics. [doi:10.1063/1.3609873]

Amorphous indium-gallium-zinc oxide (a-IGZO) thin-film transistors (TFTs) have attracted attention for application in the next generation display industry owing to their high mobility (10 cm^2/V$_s$), superior uniformity, and good transparency to visible light, as well as their low cost room temperature fabrication process for applications in active-matrix liquid crystal displays and active-matrix organic light-emitting diodes.[1–3] In order to make the a-IGZO TFTs affordable for practical applications, an understanding of the degradation mechanism under bias stress and light illumination is critically important. In the previous studies, the instabilities of Zn-based TFTs under gate-bias stress and light illumination have been investigated.[4–8] In addition, the apparent negative threshold voltage (V_t) shift under illuminated negative gate-bias stress has been attributed to the photo-generated hole trapping in the gate insulator or in the a-IGZO interface.[9] In general, for a switching operation in practical display driver circuits, the dynamic AC bias stress in a-IGZO TFTs should be performed under backlight or ambient light. However, the degradation mechanism under DC and AC gate-bias stress has not been reported and is worthy of further investigation. In this letter, the degradation behaviors under AC/DC gate-bias stress have been investigated in dark and under illumination. The different degradation tendencies under positive and illuminated negative gate-bias stress illustrate that the trapping efficiency of electrons and holes is different in a-IGZO TFTs.

Inverted coplanar a-IGZO TFTs were produced on a glass substrate in this work. The shaped Ti/Al/Ti (50/200/50 nm) gate electrodes were capped with 300-nm-thick SiO$_x$ gate dielectric. The source/drain electrodes were formed with DC-sputtered Ti/Al/Ti (50/200/50 nm) and then patterned by wet-etching. An active layer of 30-nm-thick

a-IGZO film was deposited by a DC magnetron sputtering system using a target of In:Ga:Zn = 1:1:1 atomic ratio. Finally, the device was capped with a 200 nm SiO$_x$ layer by PECVD at 170°C and sequentially annealed in an oven at 330°C for 2 h. In this work, the electrical properties were analyzed by Agilent B1500 and the threshold voltage (V_t) is defined as the gate voltage (V$_g$) when the normalized drain current ($I_d \times L/W$) reaches 1 nA, with transfer characteristics measured by gate voltage sweeping from −10 V to 15 V with a fixed drain voltage (V_d) of 5 V.

Figure 1(a) shows the transfer I$_d$−V$_g$ characteristics as a function of applied stress time for *a*-IGZO TFTs with a DC bias stress condition of $V_g = 30$ V and $V_{s,d} = 0$ V. Both the measurements of electrical characteristics as well as the application of bias stress were performed in dark. The parallel threshold voltage (V_t) of 3.8 V after 250 s stress time without significant subthreshold swing (SS) degradation indicates that the state creation can be excluded. In previous studies, the bias stress-induced degradation of a-IGZO TFTs has been attributed to the charge trapping model, with the time dependence of ΔV_t under stress following a stretched-exponential equation, as follows:

$$\Delta V_t = V_0\{1 - \exp[-(t/\tau)^\beta]\},$$

where ΔV_t is the V_t shift before recovery phase, $V_0 = V_g - V_{t0}$ where V_{t0} is the threshold voltage before stress, β is the stretched-exponential exponent, and τ represents the characteristic trapping time of carriers.[4,5,10] Therefore, the fine fitting of the stretched-exponential equation to the experimental data shown in the inset expresses that the V_t shift is caused by electron trapping in the gate dielectric or at the channel/dielectric interface. Figure 1(b) shows the time dependence of V_t shift after DC and AC positive bias stress (PBS) performed in the dark, with the AC stress conditions as follows: V$_g$ = 0 ∼ 30 V, V$_D$ = V$_S$ = 0 V, f = 25 kHz,

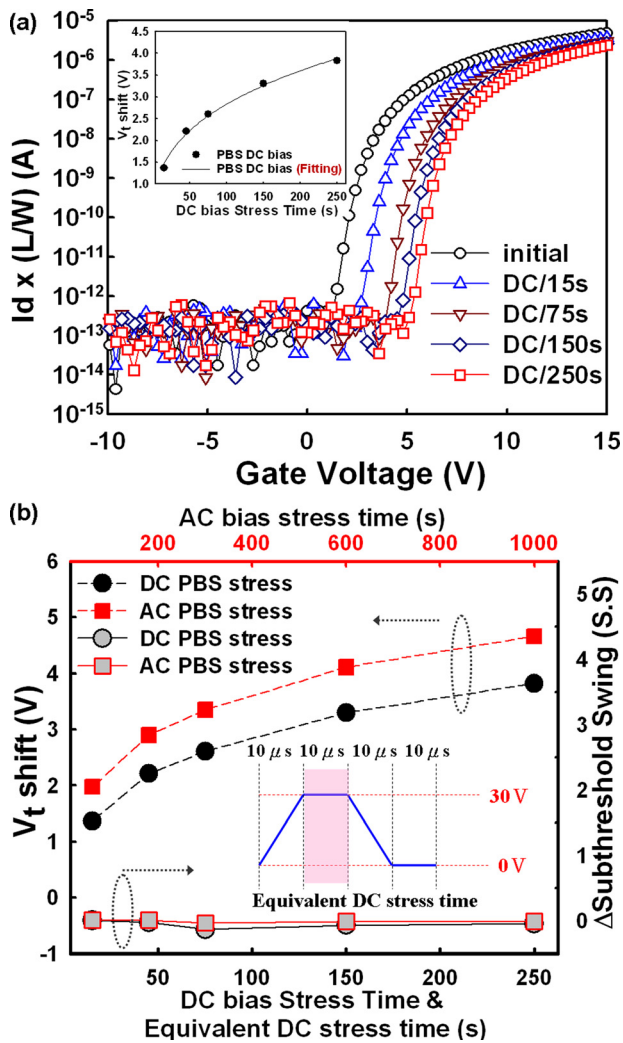a)Electronic mail: tcchang@mail.phys.nsysu.edu.tw.

FIG. 1. (Color online) (a) Normalized *I-V* characteristics of *a*-IGZO TFTs after positive DC gate-bias stress for 250 s at $V_G = 30$ V, $V_{S/D} = 0$ V. The inset shows the time dependence of ΔV_t under positive DC gate-bias stress and the fitting with stretched-exponential equation. (b) Time dependence of ΔV_t and SS degradation under positive DC and AC gate-bias stress; the inset shows the waveform of positive AC gate-bias pulse.

FIG. 2. (Color online) (a) Normalized *I-V* characteristics of *a*-IGZO TFTs under negative DC gate-bias stress for 250 s at $V_G = -20$ V, $V_{S/D} = 0$ V. (b) Normalized *I-V* characteristics of *a*-IGZO TFTs under illuminated negative DC gate-bias stress for 250 s at $V_G = -20$ V, $V_{S/D} = 0$ V; the inset shows the light spectrum and the time dependence of ΔV_t under illuminated negative DC gate-bias stress.

rising/falling time $t_r = t_f = 10$ μs, and duty ratio of 50% (as shown in the inset of Fig. 1(b)). In addition, the equivalent DC stress time for AC pulse represents the total stress time on the peak value (30 V). The experimental result demonstrates that the degradation behavior under AC stress is more obvious than the DC operation since the electron trapping mechanism occurs not only in the peak value of the AC pulse but also in the rising and falling time, resulting in an extra V_t shift. In addition, the slight variation of SS indicates that the state creation is negligible under AC bias stress.

Figures 2(a) and 2(b) exhibit the transfer I_d-V_g characteristics under DC negative bias stress (NBS) and negative bias illumination stress (NBIS), respectively. The DC electrical stress conditions are $V_g = -20$ V and $V_{s,d} = 0$ V for 250 s, and the light intensity under illumination is 10 000 lux with the spectrum shown in the inset of Fig. 2(b). The lack of apparent V_t variation under NBS can be attributed to the negligible holes in the n-type oxide semiconductor valence bands; therefore, the hole trapping at either the gate insulator or at the a-IGZO interface can be ignored. However, numerous holes are generated under light illumination with light in-
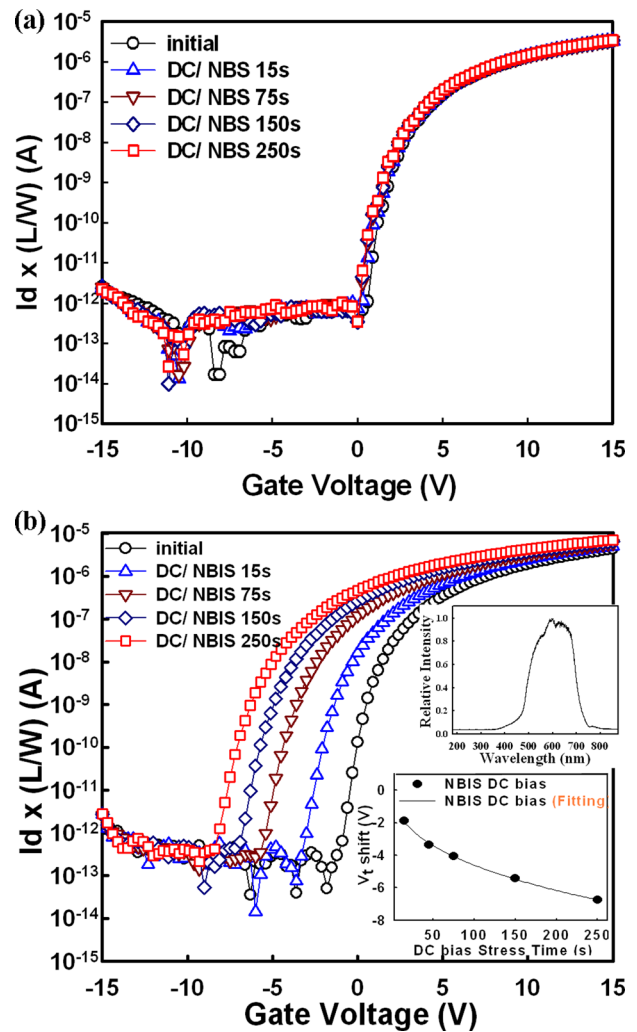
tensity of 10 000 lux by the trap-assisted electron-hole pair process but is further enhanced by gate bias. The generated holes will be trapped in the gate insulator or a-IGZO interface, resulting in a dramatic parallel negative V_t shift.[8] The inset of Fig. 2(b) shows the V_t shift versus stress time and the fine fitting to the well-accepted stretched-exponential model also verifies the hole trapping mechanism under NBIS.

To further investigate the hole trapping phenomenon under NBIS, we performed the AC operation with the electrical stress condition $V_g = 0 \sim -20$ V, $V_d = V_s = 0$ V, $f = 25$ kHz, rising/falling time $t_r = t_f = 10$ μs, and duty ratio of 50% (as shown in the inset of Figure 3) for comparison with the DC operation. According to the experimental result in Fig. 1(b), the extra charge trapping time contributed by the rising/falling time under positive AC bias operation can cause a more apparent V_t shift than under DC PBS. On the contrary, the result of Fig. 3 shows that the V_t shift under DC NBIS operation is more significant than under the AC NBIS operation. This phenomenal difference can be attributed to the trapping efficiency of electrons or holes. For electron trapping, because the a-IGZO TFT is an n-type oxide
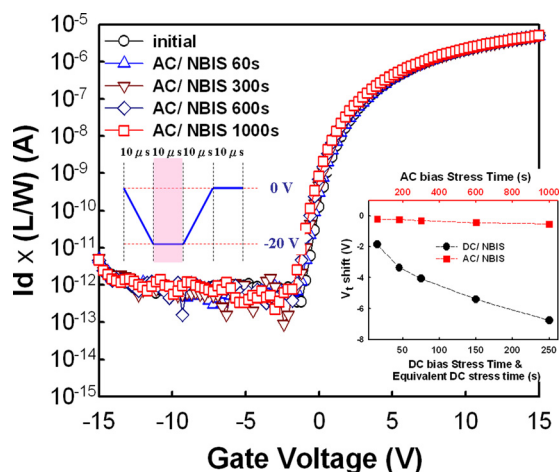
FIG. 3. (Color online) Normalized *I-V* characteristics of *a*-IGZO TFTs under illuminated negative DC gate-bias stress; the inset shows the time dependence of ΔV_t under illuminated negative DC and AC gate-bias stress and the waveform of negative AC gate-bias pulse.
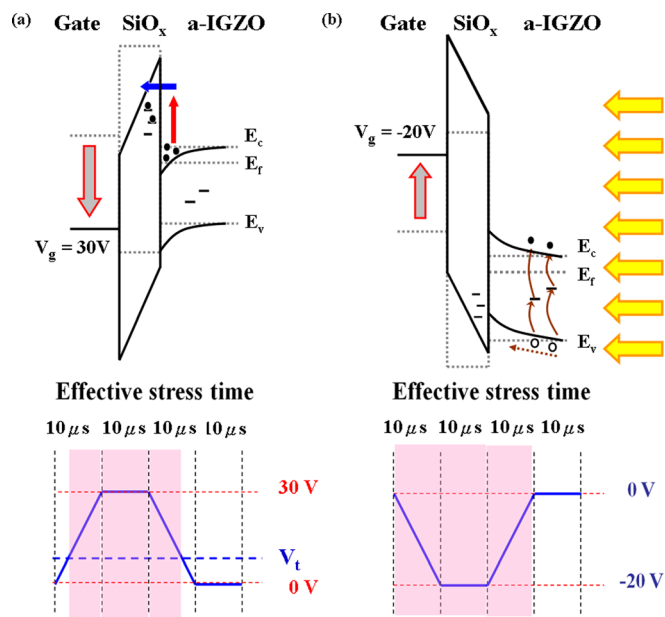

FIG. 4. (Color online) Schematic band diagrams of a-IGZO TFT and the stress pulse waveform under (a) PBS and (B) NBIS operation.

semiconductor and the electron trapping occurs once gate bias exceeds inversion voltage, the extra electron trapping occurs during the rising/falling time (the corresponding schematic band diagram is shown as Fig. 4(a)). However, although the photo-generated holes can drift to the interfaced once V_g switch to negative bias, the period of AC NBIS operation is too short to provide enough time for hole generation and drifting to the gate insulator or a-IGZO interface since the hole mobility is much smaller than electron.[11,12] Therefore, the V_t shift under NBIS AC operation is much slighter than DC operation.

In conclusion, the rising/falling time during the positive AC pulse period can cause an extra electron trapping mechanism; thus, the V_t degradation is more serious compared to the positive DC gate-bias stress. On the contrary, the V_t degradation of -0.52 V after AC NBIS is much slighter than the DC NBIS operation (-6.75 V). For dynamic AC operation, electron trapping occurs once gate bias exceeds inversion voltage even for the rising/falling time, whereas the negative gate pulse period under NBIS operation is too short to provide enough time for hole generation and trapping in either the gate insulator or a-IGZO interface. Therefore, the carrier trapping efficiency dominates the degradation behavior under AC/DC gate-bias stress.

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