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Effect of surface preparation on the radiation hardness of high-dielectric constant gate dielectric

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ABSTRACT

Effect of surface preparation on the radiation hardness of MOS devices with high dielectric constant gate dielectric of HfO_2 and metal gate of TiN is studied using extreme ultra-violet (EUV) light as the radiation source. Three kinds of surface treatment including HF-last, chemical-oxidation, and rapid-thermal-oxidation were evaluated. Among them, chemical-oxidation exhibits the best radiation hardiness in terms of interface traps and border traps. The state-of-the-art MOSFET with a thin high-*k* dielectric and a high quality chemical oxide interfacial layer shows that the degradation of subthreshold swing is more severe than degradation of threshold voltage. However, the overall degradation is less than 6% even after EUV irradiation to a total dose of 580 mJ/cm^2. Off-state current degradation is observed due to the generation of oxide traps and interface traps at the isolation region. This phenomenon does not occur in the conventional optical lithography process but should be considered if EUV lithography is used.
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1. Introduction

High-dielectric constant (high-*k*) dielectrics have replaced silicon dioxide (SiO_2) to be the gate dielectric of advanced MOSFETs since the 45 nm technology node. The reliability issues of high-*k* dielectric including time-dependent dielectric breakdown, charge trapping, and bias-temperature instability have been widely studied [1]. It is acknowledged that although the reliability issues of high-*k* dielectrics are different from those of the well known SiO_2 gate dielectric, these issues do not set fundamental limitations on the commercial applications. However, high performance and low power integrated circuits may be used in systems which operating under radiation environment so that the radiation hardness of high-*k* gate dielectric is also an important reliability issue. Radiation damages on high-*k* dielectrics have been reported in literature [2–5]. It is shown that both Hf-based dielectrics and Al_2O_3 have higher charge trapping efficiency than that of thermal oxide. Acceptable radiation tolerance of MOSFET with thin HfO_2 gate dielectric was also reported [5]. These reports used high energetic photons such as gamma-ray and X-ray, and focused on the charge trapping in the bulk of high-*k* dielectrics. However, the reliability of the high-*k* structures would be affected by the interfacial layer as well as the high-*k* layer. Furthermore, high-*k* dielectrics may expose to ionizing radiation during IC processing. In this case, low energy radiation source should be considered.

Recently, extreme ultra-violet (EUV) lithography technology achieves great progress. Several pre-production tools have been delivered since 2010. Both mask technique and photo-resist technique progress very fast. Therefore, EUVL has been seriously considered as the most promising next generation lithography technology. Several full-field EUVL technologies have been demonstrated [6–10]. A. Veloso et al. employed EUVL for single-patterning of denser arrays of smaller CH and M1 trenches [6]. Nakamura et al. demonstrated a 2-level Cu/low-*k* interconnects with 70 nm pitch featuring EUV lithography [8]. Tom Vandeweyer et al. used EUV lithography for the patterning four critical layers (active or fin, gate, contact and metal-1) of a 16 nm node 6T-SRAM cell [10]. This is the first time for using EUV in the front-of-line process. Once EUVL is employed in the front-of-line process, the high energy of EUV should be considered.

The currently used wavelength for advanced ICs is 193 nm. The energy of this light is 6.4 eV, and is lower than the energy bandgaps of typically used dielectrics. However, the 13.5 nm wavelength of EUV translates the energy of 91.85 eV. This energy is higher than the bonding energies and energy band gaps of all dielectrics. EUV

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irradiation during processing may result in reliability issue. Our previous study observed that oxide traps, border traps, and interface traps would be generated by extreme-ultra-violet (EUV) irradiation in SiO_2, Si_3N_4, Al_2O_3, HfSiO, and HfAlO [11,12]. And our preliminary result revealed that the interfacial layer plays important role on the radiation hardness. In this work, the effect of interface engineering on radiation hardness of MOS devices using HfO_2 as gate dielectric is studied. The radiation hardness of the state-of-the-art MOSFET is also evaluated.

2. Device fabrication

Simple metal-insulator-silicon (MIS) capacitor structure with HfO_2 deposited by an atomic layer deposition (ALD) system is used in this work. The devices were fabricated on (1 0 0)-oriented doron doped Si wafers with a resistivity of 1–10 Ω cm. After standard RCA clean, three kinds of surface preparation method were performed. On sample A, the chemical oxide formed during the RCA clean was removed by immersion in diluted HF (DHF) before HfO_2 deposition. On sample B, the chemical oxide formed during the RCA cleaning received a 900 °C rapid thermal annealing in N_2 ambient for 30 s before HfO_2 deposition in order to preserve the same thermal budget as sample C. On sample C, after removing the chemical oxide by DHF immersion, a 2-nm-thick SiO_2 layer was grown by a rapid thermal oxidation (RTO) system at 900 °C for 30 s. Then, a 15-nm-thick HfO_2 layer was deposited by an ALD system using TEMAH and H_2O as precursors at 250 °C. It should be noted that those important parameters of MOSFET including threshold voltage, subthreshold swing, and channel carrier mobility would be affected by irradiation, but these parameters cannot be measured using simple MIS capacitor. Therefore, only mid-gap voltage and flatband voltage are measured in this work using the MIS capacitor structure. Thicker dielectric produces more apparent shift and/or distortion of the *C–V* characteristic. Therefore, we choose a relatively thick dielectric thickness so that all of the possible damages either in the bulk of dielectric or at the dielectric/Si interface can be easily extracted from the simple MIS structure.

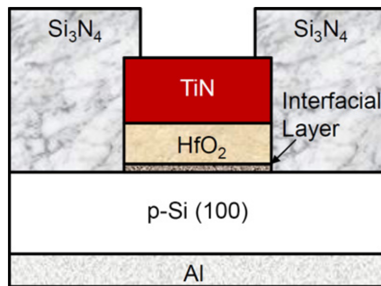

Fig. 1. Schematic cross-sectional structure of the metal-insulator-Si (MIS) structure used in this work.

After the HfO_2 layer deposition, samples were processed by a rapid thermal annealing in N_2 ambient at 500 °C for 30 s. A 5-nm-thick TiN layer was deposited immediately by the same ALD system to provide a good TiN/HfO_2 contact. An additional 35-nm-thick TiN layer was deposited by DC sputtering in order to increase the gate electrode thickness but shorten the process time. All samples were capped with a 100-nm-thick Si_3N_4 layer for protecting samples from moisture-uptake. The probing pads were opening by typical lithography and wet etchiing processes. Fig. 1 shows the schematic structure of the MIS capacitor. The main process conditions of all samples are listed in Table 1. The Sample R with 15-nm-thick SiO_2 gate dielectric is used as reference.

The 13.5-nm-wavelength radiation source comes from the beam-line 08A1 constructed at the National Synchrotron Radiation Research Center, Taiwan, ROC. The irradiation dose on high-*k* samples ranges from 150 to 500 mJ/cm^2. The 40-nm-thick TiN gate electrode absorbs 52% of the dose. The actual dose on high-*k* dielectrics is around 72–240 mJ/cm^2. According to the ITRS roadmap, the expected EUVL dose is 10–20 mJ/cm^2. The dose used in this manuscript is about 5–15 times higher than the expected dose in order to magnify the effects. This is a typical strategy for early stage reliability evaluation. Because SiO_2 is more resist to radiation damages than high-*k* dielectrics, the dose used for the SiO_2 sample is 1800 mJ/cm^2 in this work.

3. Results and discussions

Fig. 2 shows the high-resolution transmitted electron microscopic (HRTEM) micrograph of the interfacial structure of the three

Table 1
Process conditions of samples used in this work. The dielectric thicknesses are determinmed by high resolution transmission electron microscopic inspection.

Sample ID	R	A	B	C
Interface treatment	HF-last	HF-last	Chemical oxide 1.5 nm	Rapid thermal oxide 2 nm
Gate dielectric	SiO_2 15 nm	HfO_2 13.4 nm	HfO_2 12.7 nm	HfO_2 12.7 nm
Formation method	Oxidation	ALD	ALD	ALD
Formation temperature	900 °C	250 °C	250 °C	250 °C
Post-deposition annealing	Without	500 °C	500 °C	500 °C

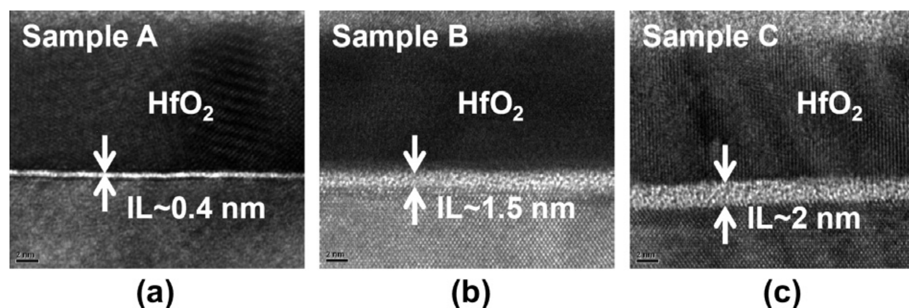

Fig. 2. Interface structure inspected by high-resolution transmitted-electron-microscope (HRTEM) of the samples with different surface treatments. (a) HF-last, (b) chemicaloxidation, and (c) rapid thermal oxidation.

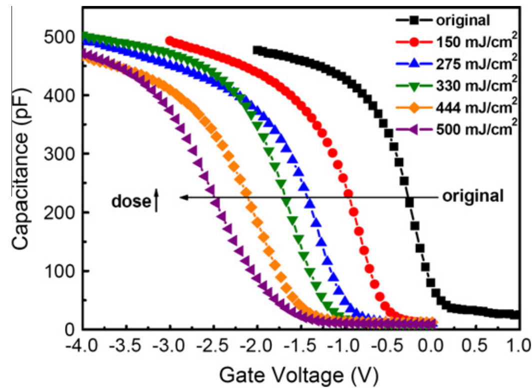

Fig. 3. Capacitance-voltage characteristics of the sample B after receiving EUV irradition to various doses. Higher irradiation dose results in more apparent *C–V* shift and distortion.

HfO_2 samples. A 0.4-nm-thick interfacial layer was formed during the 500 °C post-deposition annealing process on sample A and the physical thickness of the HfO_2 layer is 13.4 nm. The HfO_2 thickness for samples B and C is 12.7 nm, with an interfacial layer thickness of 1.5 nm and 2 nm, respectively. Fig. 3 shows the capacitance-voltage (*C–V*) characteristics of the sample B before and after EUV irradiation to various doses. The degradation increases with the increase of radiation dose as expected. No saturation phenomenon is observed up to 500 mJ/cm^2. Since the purpose of this work is to study the effect of surface preparation, we use the data with the intermediate dose of 275 mJ/cm^2 in the following discussion. This dose was also used in our previous works so that the results can be compared easily [12].

Fig. 4 shows the *C–V* characteristics of the three high-*k* samples before and after EUV irradiation. The shift and distortion of the *C–V* curves indicate the increment of trapped charges and interface traps. Hysteresis phenomenon is also observed on all of the high-*k* samples but is not shown in the figure. The hysteresis voltages (V_{hyst}) are listed in Table 2. It is clear that the chemical oxide interfacial layer can suppress the shift and distortion of the *C–V* characteristics effectively. The RTO interfacial layer has little improvement on the radiation hardness. The stretch-out of the *C–V* curve near accumulation reflects the generation of donor-like interface traps at the lower-half of the Si band gap. The energy distribution of the interface-state density (D_{it}) was extracted by typical high-frequency *C–V* method [13], and the results before and after EUV irradiation are shown in Fig. 5. It is

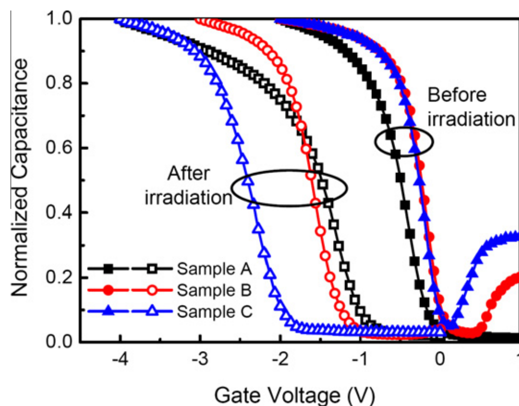

Fig. 4. Capacitance–voltage characteristics of the sample A, B, and C before and after EUV irradition. The irraidaiton dose is 275 mJ/cm^2 on all samples.

Table 2
Extracted hysteresis voltage (V_{hyst}) , increase of hysteresis voltage (ΔV_{hyst}), increase of oxide traps (ΔN_{ot}), and increase of interface traps (ΔN_{it}) after EUV irradiation of all samples prepared in this work.

Sample ID	R	A	B	C
Dose (mJ/cm^2)	440	275	275	275
V_{hyst} (mV)	~0	171	57	67
ΔV_{hyst} (mV)	18	143	138	451
ΔN_{ot} (cm^{-2})	1.13×10^{11}	3.80×10^{12}	5.55×10^{12}	7.88×10^{12}
ΔN_{it} (cm^{-2})	2.33×10^{11}	4.75×10^{12}	7.86×10^{11}	1.34×10^{12}

clearly observed that after EUV irradiation the D_{it} of all samples increases. Sample R received a much higher total dose but exhibits the lowest D_{it}. According to the *C–V* distortion in Fig. 4 and the D_{it} distribution in Fig. 5, it is confirmed that the interface traps generated by EUV irradiation are donor-like and locate at the lower-half of the energy gap of Si.

The oxide traps (N_{ot}) and interface traps (N_{it}) are separated by the mid-gap voltage (V_{mg}) method [14]. This method assumes that at the mid-gap voltage V_{mg}, when the Fermi level intersects the mid-gap energy at the silicon surface, the interface charge becomes zero. This assumption is confirmed by Fig. 5. According to this figure, the newly generated interface traps are lower than the Fermi energy at V_{mg}, thus the increase of N_{ot} (ΔN_{ot}) could be calculated from the shift of the V_{mg} (ΔV_{mg}). Since we have the D_{it} distribution in Fig. 4, the increase of N_{it} (ΔN_{it}) is calculated by integrating the difference in D_{it} before and after irradiation. The extracted increase of V_{hyst} (ΔV_{hyst}), ΔN_{ot}, and ΔN_{it} are listed in Table 2. Since the ΔN_{ot} of sample R is very low, the ΔN_{ot} of the HfO_2 samples should distribute in the HfO_2 layer. It is noticed that the ΔN_{it} of the sample B is 6 times lower than that of the sample A and is similar to that of the sample R. Sample B also exhibits less degradation of the hysteresis phenomenon. These results indicate that the chemical oxide interfacial layer improves radiation hardness effectively. There are two possible reasons. First, the growth of high quality ALD HfO_2 film requires OH surface group while the chemical oxide contains more OH groups [15]. Second, the low temperature growth of chemical oxide produces less interface stress and thus less strained Si–O bonds.

If the oxide trapped charges distribute in the gate dielectric, the threshold voltage shift (ΔV_{th}) due to ΔN_{ot} scales with T_{ox}^{-n}, where $n > 2$ for thin gate dielectric. According to the data of sample B in Table 2, the ΔV_{th} is expected to be less than 25 mV as the thickness of the HfO_2 layer reduces to 2 nm. To verify this prediction, the state-of-the-art MOSFET with Hf-based gate dielectric and TiN metal gate is fabricated and its radiation hardness is evaluated. Fig. 6 shows the cross-sectional TEM micrograph of the MOSFET. The gate stack consists of a 0.4-nm-thick interfacial oxide, a 2-nm-thick Hf-based dielectric, and a thin TiN metal gate. Above TiN, there are barrier metal and low resistivity metal. The effective oxide thickness is 0.8 nm. Fig. 7 shows the current–voltage (*I–V*) characteristics of a MOSFET before and after EUV irradiation to a dose of 580 mJ/cm^2. After EUV irradiation, the V_{th} decreases from 614 mV to 608 mV (~1%) but the subthreshold swing (SS) degrades from 69.9 to 74.2 mV/dec, i.e. about 6%. This result is consistent with the fact that the EUV generated interface traps are donor-like and distribute at the lower-half of the Si bandgap. The amount of the interface-state trapped charges changes with the surface potential as the device is in subthreshold region so that the SS degrades. At threshold voltage, all of the newly generated interface traps are neutral and do not affect the V_{th}. Only ΔN_{ot} would contribute to the ΔV_{th}. The Hf-based dielectric is only 2-nm-thick for this MOSFET, which is much thinner than the HfO_2 layer for the samples A, B, and C. In this case, the electron-hole pairs generated in the thin HfO_2-based dielectric may escape to gate electrode or Si

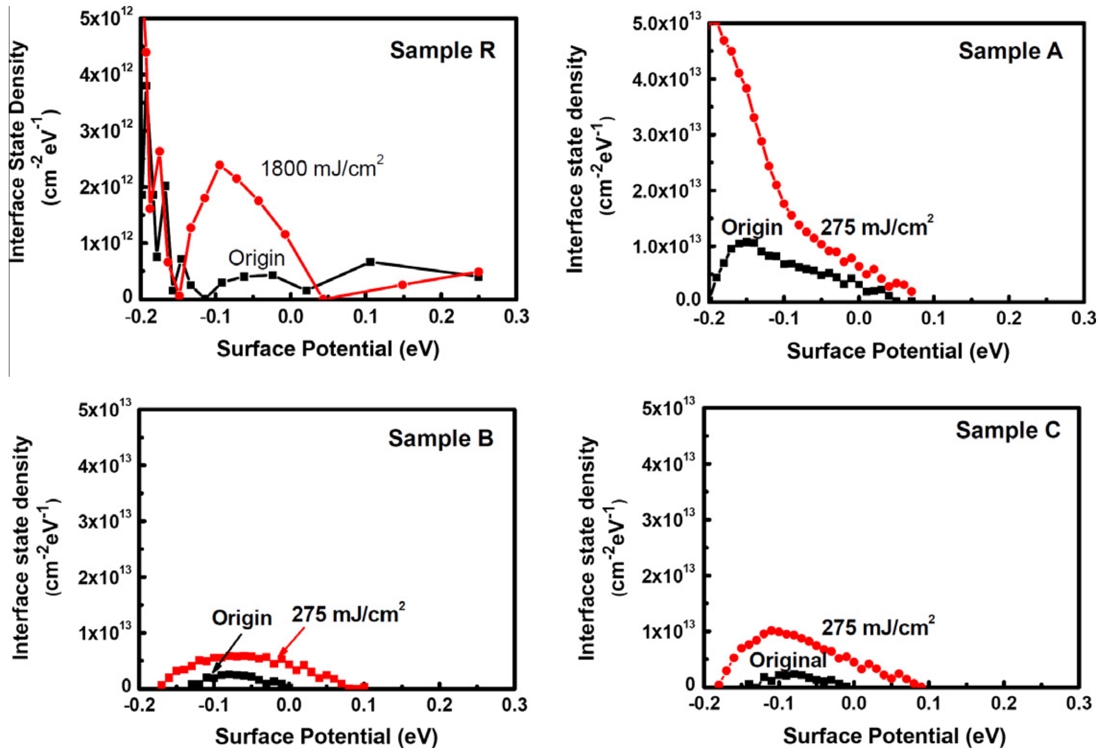

Fig. 5. Energy distribution of interface states extracted by the high frequency *C–V* method of the samples R, A, B, and C before and after EUV irradiation.

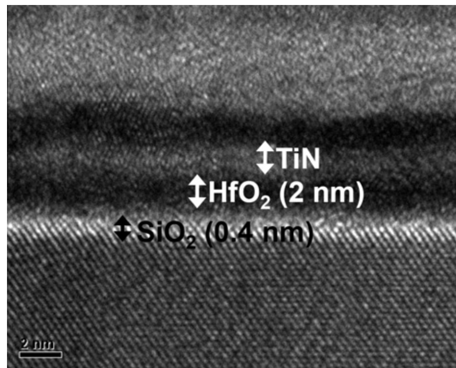

Fig. 6. High-resolution transmitted-electron-microscopic (HRTEM) image of the gate stack of the state-of-the-art MOSFET. The thickness of the interfacial chemical oxide is 0.4 nm, the thickness of the Hf-based gate dielectric is 2 nm. A 1.5 nm thick TiN is used to adjust the threshold voltage.

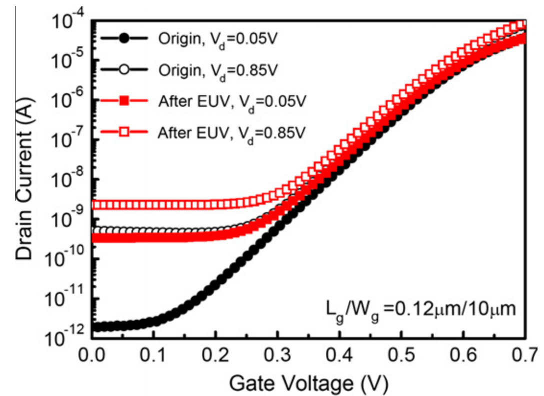

Fig. 7. Current–voltage characteristics of a MOSFET before and after EUV irradiation. The effective dose in HfO_2 is 580 mJ/cm^2. Slight but acceptable degradation is observed even at such a high irradiation dose.

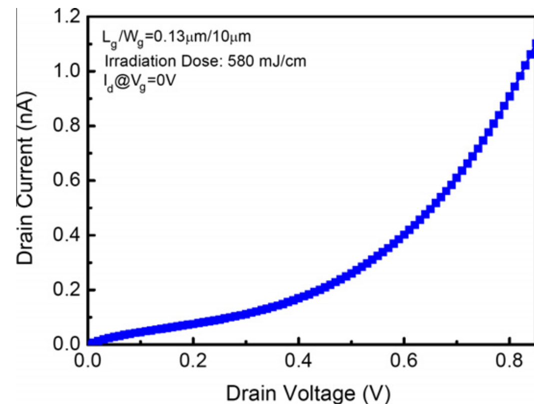

Fig. 8. Off-state leakage current as a function of drain voltage at VGS = 0 V. The non-linear *I–V* characteristic implies the leakage current is dominated by the surface generation current.

substrate so that the ΔV_{th} is much lower than that estimated from the MIS capacitors [16].

The increase of the off-state current comes from the leakage path due to the oxide traps and interface traps generated by EUV irradiation along the isolation edge [17,18]. There are two possible cases. If the Si surface under the isolation is inversed by the positive oxide charges due to the EUV irradiation, a resistive conduction path connects drain and source. In this case the off-state current would show a linear V_{DS} dependence. If the positive charges do not inverse the Si surface but the irradiation generate N_{it} at the isolation oxide/Si interface, the surface generation current arising from the interface states would show a $\sqrt{V_d}$ dependence. Fig. 8 shows the off-state leakage current as a function of V_d at $V_g = 0$ V. The non-linear characteristic implies that the increase of the off-state current is dominant by the surface genera-

tion current arising from the of the EUV irradiation generated interface states. This phenomenon does not occur in the conventional optical lithography process but should be considered if EUV lithography is used.

4. Conclusions

The effect of surface preparation on the radiation hardness of the HfO_2 gate dielectric is studied. Three kinds of surface preparation method, HF-last, chemical oxidation, and rapid thermal oxidation, are evaluated. Although EUV irradiation would generate oxide traps, border traps, and interface traps on all samples, the amount of each kind of traps strongly depends on the surface preparation method. Chemical oxide provides a low stress oxide/Si interface and sufficient OH surface groups so that the increase of interface traps and border traps is minimized. Therefore, using a high quality interfacial layer such as chemical oxide can significantly reduce the generation of border traps and interface traps during irradiation. Fortunately, chemical oxide is the standard interfacial layer used in current MOSFTEs with high-*k* gate dielectric. Finally, the state-of-the-art MOSFET with a thin high-*k* dielectric and a high quality SiO_2-like interfacial layer demonstrates acceptable radiation hardness. This is the first time to report the effect of EUV irradiation on the state-of-the-art MOSFET. However, EUV irradiation may generate oxide traps in the bulk of field oxide and interface traps at the field oxide/Si interface. These defects increase the off-state current apparently. This phenomenon does not occur in the conventional optical lithography process but should be considered if EUV lithography is used.

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References

[1] Ribes G, Mitard J, Denais M, Bruyere S, Monsieur F, Parthasarathy C, et al. Review on high-*k* dielectrics reliability issues. IEEE Trans Dev Mater Rel 2005;5(1):5–19.
[2] Kang AY, Lenahan PM, Conley Jr JF. The radiation response of the high dielectric-constant hafnium oxide/silicon system. IEEE Trans Nucl Sci 2002;49(6):2636–42.
[3] Felix JA, Fleetwood DM, Schrimpf RD, Hong JG, Lucovsky G, Schwank JR, et al. Total-dose radiation response of hafnium-silicate capacitors. IEEE Trans Nucl Sci 2002;49(6):3191–6.
[4] Felix JA, Shaneyfelt MR, Fleetwood DM, Schwank JR, Dodd PE, Gusev EP, et al. Charge trapping and annealing in high-*k* gate dielectrics. IEEE Trans Nucl Sci Dec. 2004;51(6):3143–9.
[5] Dixit SK, Zhou XJ, Schrimpf RD, Fleetwood DM, Pantelide ST, Choi R, et al. Radiation induced charge trapping in ultrathin HfO_2 –based MOSFETs. IEEE Trans Nucl Sci Dec. 2007;54(6):1883–90.
[6] Veloso A et al., Demonstration of scaled 0.099 μm 2 F in FET 6T-SRAM cell using full-field EUV lithography for Sub-22nm node single-patterning technology. In: IEDM tech dig; 2009. p.301–4.
[7] Nakamura N, Oda N, Soda E, Hosoi N, Gawase A, et al, Feasibility Study of 70 nm Pitch Cu/Porous Low-*k* D/D integration featuring EUV lithography toward 22 nm generation. In: IEDM tech dig; 2009. p. 875–8.
[8] Kim K, The future Si technology perspective: challenges and opportunities. In: IEDM Tech dig; 2010. p. 1–9.
[9] Wagner C, Bacelar J, Harned N, Loopstra E, Hendriks S, de Jong I, et al, EUV lithography at chipmakers has started: performance validation of ASML's NXE:3100. In: Proc of SPIE. 2011; 7969. p. 79691F–1∼79691F-12.
[10] Vandeweyer T De Backer J, Versluijs J, Truffert V, Verhaegen S, Ercken M, et al., Patterning challenges in setting up a 16 nm node 6T-SRAM device using EUV lithography. In: Proc of SPIE; 2011 7969. p. 79691K–1∼79691K-12.
[11] Tsui BY, Yen CC, Li PH, Lai JY. Effects of extreme ultra-violet irradiation on poly-Si SONOS non-volatile memory. IEEE Electron Dev Lett 2011;32(5):614–6.
[12] Tsui BY, Li PH, Yen CC. Observation of extreme ultra-violet irradiation induced damages on high-dielectric constant dielectrics. IEEE Electron Dev Lett 2011;32(11):1594–6.
[13] Terman LM. An investigation of surface states at a silicon/silicon oxide interface employing metal–oxide–silicon diodes. Solid-State Electron 1962;5(5):285–2992.
[14] Winokur PS, Schwank JR, McWhorter PJ, Dressendorfer PV, Turpin DC. Correlating the radiation response of MOS capacitors and transistors. IEEE Trans Nucl Sci 1984;31:1453–60.
[15] Nyns L, Hall L, Conard T, Delabie A, Deweerd W, Heyns M, et al, Surface preparation techniques for the atomic layer deposition of hafnium oxide. in MRS proceedings 2006; p. 917.
[16] McWhorter PJ, Miller SL, Miller WM. Modeling the anneal of radiation-induced trapped holes in a varying thermal environment. IEEE Trans Nucl Sci Dec. 1990;37(6):1682–9.
[17] Shaneyfelt MR, Dodd PE, Draper BL, Flores RS. Challenges in hardening technologies using shallow-trench isolation. IEEE Trans Nucl Sci 1998;45(6):2584–92.
[18] Dodd PE, Shaneyfelt MR, Schwank JR, Felix JA. Current and future challenges in radiation effects on CMOS electronics. IEEE Trans Nucl Sci 2010;54(4):1747–63.