$In_{0.5}Ga_{0.5}$As-Based Metal–Oxide–Semiconductor Capacitor on GaAs Substrate Using Metal–Organic Chemical Vapor Deposition

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***Abstract*—We demonstrate the good-performance $In_{0.5}Ga_{0.5}$As-based metal–oxide–semiconductor capacitor (MOSCAP) on GaAs substrate using metal–organic chemical vapor deposition technique. $In_{0.5}Ga_{0.5}$As film grown on GaAs substrate is proved to be high quality with threading dislocation density as low as 10^6 cm^{-2}. The performance of the MOSCAPs is comparable to that of $In_{0.53}Ga_{0.47}$As/InP-based devices grown by molecular beam epitaxy technique. The devices show a nice capacitance–voltage response, with small frequency dispersion. The parallel conductance contours show the free movement of Fermi level with the gate bias. Acceptable interface trap density D_{it} values of $5 \times 10^{11}-2 \times 10^{12}$ eV$^{-1}\cdot$ cm^{-2} in the energy range of 0.64–0.52 eV above the InGaAs valence band maximum in $In_{0.5}Ga_{0.5}$As/GaAs MOSCAPs obtained by conductance methods were shown.**

***Index Terms*—Al_2O_3, InGaAs, metal–organic chemical vapor deposition (MOCVD), metal–oxide–semiconductor (MOS) capacitor (MOSCAP).**

I. Introduction

DUE TO THEIR high electron mobility and bandgap in the range of 0.36–1.42 eV, In_xGa_{1-x}As-based metal–oxide–semiconductor (MOS) devices are potentially suitable for application at low supply voltages [1]. Outstanding performance of $In_{0.53}Ga_{0.47}$As-based MOS capacitor (MOSCAP) devices on InP substrate grown by molecular beam epitaxy (MBE) has been achieved [2]–[4]. A major advantage of using InP as a substrate is that it is ideal for growing lattice-matched $In_{0.53}Ga_{0.47}$As/InP. However, InP substrates are more expensive, fragile, available in smaller sizes, and have less mature processing technology as compared to Si substrates [5]. Therefore, the integration of In_xGa_{1-x}As compound on Si substrates is desirable for future low-cost, light-weight, large-area, and high-performance low-power logic device [6], [7]. However, the large lattice mismatch and coefficient of thermal mismatch between In_xGa_{1-x}As compounds and Si substrate obstruct the growth of a high-quality epilayer, particularly by using metal–organic chemical vapor deposition (MOCVD). These difficulties have been addressed by using III–V materials (GaAs) [8], [9] or Si_xGe_{1-x} alloy [10] as buffers in order to reduce dislocation propagating to active layer. The first step toward the goal of III–V/Si is to obtain high-quality thin GaAs (or Ge) on Si substrate, creating the so-called alternative substrates; then, III–V materials will be grown on the alternative GaAs/Si substrates. Hence, exploring the growth and fabrication technique for In_xGa_{1-x}As $(x \approx 0.5)$-based MOSCAP devices on GaAs substrate is necessary, particularly the development carried out by MOCVD method, making them one step closer to future goal of large-scale integration of devices on Si substrate. In this paper, we demonstrate that good-performance $In_{0.5}Ga_{0.5}$As-based MOSCAP device on GaAs substrate using MOCVD method and its performance are comparable to those of $In_{0.53}Ga_{0.47}$As on InP substrate grown by MBE.

II. Experimental Procedure

$In_{0.5}Ga_{0.5}$As epifilm was grown on n-type epiready GaAs (001) substrates with 6° offcut [11] toward [110] direction in MOCVD (EMCORE D180) system using trimethylindium, trimethylgallium, and pure arsine (AsH_3) as group-III and group-V precursors, respectively. Monosilane (SiH_4) was used as n-type doping source. The total pressure in the reactor and the growth temperature were kept at 70 torr and 490 °C, respectively. The $In_{0.5}Ga_{0.5}$As/GaAs (henceforth, "MOCVD-InGaAs/GaAs MOSCAP") structure consists of 5.5-μm In_xGa_{1-x}As step-graded buffer layers followed by 1.5-μm $In_{0.5}Ga_{0.5}$As epilayer Si doped to 1×10^{17} cm^{-3} under optimized growth conditions similar to that described elsewhere [12]. For MOSCAP device fabrication, initial InGaAs/GaAs wafer was degreased in acetone and isopropanol for 2 min each. The sample was then dipped into HCl 4% solution for 2 min followed by rinsing in deionized water and N_2 blowing. It was then immediately loaded into the atomic layer deposition (ALD) chamber (Cambridge NanoTech Fiji 202 DSC). In ALD chamber, 10-trimethyl aluminum (TMA)/Ar pulses were

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TABLE I
PARAMETERS OF InGaAs USED IN DETERMINING THE TRAP LEVEL E_T

	$In_{0.53}Ga_{0.47}As$	$In_{0.5}Ga_{0.5}As$
σ (cm^2)	10^{-16}	10^{-16}
v_{th} (cm/s)	5.5×10^7	5.4×10^7
N (cm^{-3})	2.1×10^{17}	2.17×10^{17}
C_{ox} (nF/cm^2)	760	760
MOSCAPs area (cm^2)	1.33×10^{-4}	1.33×10^{-4}

used for precleaning [2], [13], followed by the deposition of 9-nm Al_2O_3 at 250 °C using TMA and water vapor as precursors. After that, the sample was treated by postdeposition annealing at 500 °C in N_2 for 5 min. Ni/Au gate metal was formed by lithography/e-beam evaporation/lift-off processes. The area of MOSCAPs is listed in Table I. Finally, Au/Ge/Ni/Au ohmic contact was deposited on backside using e-beam evaporation, followed by postmetal annealing at 300 °C in N_2 for 1 min. For comparison, MOSCAP structure was also fabricated on 100-nm MBE silicon-doped $(5 \times 10^{17}\ \text{cm}^{-3})$ n-$In_{0.53}Ga_{0.47}As$ on $hboxn^+$-InP substrate (henceforth, "MBE-InGaAs/InP MOSCAP") in the same process. Capacitance–voltage (C–V) and conductance–voltage (G–V) measurements were done by using an HP4284A LCR meter, and quasi-static C–V (QSCV) characterization was performed on an Agilent B1500A analyzer. The integration time for QSCV measurement was 500 ms. This integration time was confirmed long enough to get full thermal equilibrium in InGaAs MOSCAPs; longer integration time of 1 s was also performed, but the QSCV curve did not change.

III. RESULTS AND DISCUSSION

The structure parameters of the InGaAs epilayer were analyzed using D1-HRXRD system. Asymmetric rocking curve scans on (115) reflection of substrate were recorded in $\omega - 2\theta$ scans to determined indium composition and relaxation degree of $In_xGa_{1-x}As$ alloy on GaAs substrate. The indium composition (x) in $In_xGa_{1-x}As$ epilayer is obtained using Vegard's law [14]

$$x = \frac{a_f - a_s}{a_{\text{InAs}} - a_s} \tag{1}$$

where $a_s = 5.6533$ Å and $a_{\text{InAs}} = 6.0583$ Å are lattice constants of GaAs substrate and InAs, respectively. a_f is bulk equivalent or unstrained lattice constant defined by [14]

$$a_f = \frac{a_\perp - 2a_{//}\left(\frac{\nu}{1-\nu}\right)}{1 - 2\left(\frac{\nu}{1-\nu}\right)} \tag{2}$$

where ν is Poisson ratio and $a_{//}$ and $a_\perp$ are the in-plane and out-of-plane lattice parameters of $In_xGa_{1-x}As$ epilayer, respectively, and were calculated from Bragg law reflection position by

$$a_{//} = \frac{\lambda\sqrt{h^2 + k^2}}{2\sin\theta_B \sin\varphi} \tag{3}$$

$$a_\perp = \frac{\lambda l}{2\sin\theta_B \cos\varphi} \tag{4}$$

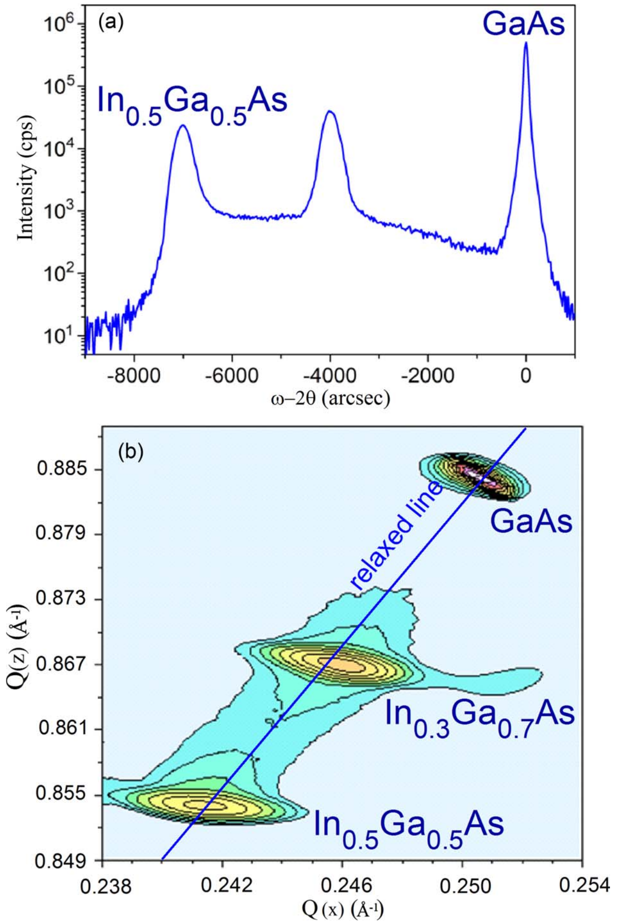

Fig. 1. (a) Asymmetric $\omega - 2\theta$ scan and (b) RSM of $In_{0.5}Ga_{0.5}As$/$In_{0.3}Ga_{0.7}As$ epilayers measured around the (115) lattice point of GaAs substrate.

where θ_B is Bragg angle; φ is the angle between the diffraction plane and the sample surface; h, k, and l are Miller indices of reflection plane, and λ is the wavelength of the X-rays ($\lambda = 1.5406$ Å).

Degree of relaxation R is defined by

$$R = \frac{a_{//} - a_s}{a_f - a_s} 100\%. \tag{5}$$

Fig. 1(a) shows the asymmetric scan for (115) reflection obtained from 1.5- and 3.3-μm $In_{0.5}Ga_{0.5}As$ and $In_{0.3}Ga_{0.7}As$ epilayers on GaAs substrate, respectively. Bragg angle was determined from the peak position of $In_{0.5}Ga_{0.5}As$ epilayer, and the in-plane and out-of-plane lattice parameters of $In_{0.5}Ga_{0.5}As$ were calculated to respective values of $a_\parallel = 5.8542$ ($\pm$0.001) and $a_\perp = 5.8562$ ($\pm$0.001) Å. The unstrained lattice parameter of the epilayer was estimated $a_f = 5.8554$ Å on average by using (2). In this calculation, we assumed that the Poison ratio of $In_{0.5}Ga_{0.5}As$ was -0.33. From (1) and (5), the indium composition and relaxation degree of the epilayer were defined as $x = 0.5 \pm 0.05$ and $R = 99\%$, respectively. The relaxation degree of $In_{0.5}Ga_{0.5}As$ epilayer was also investigated by tripe-axis X-ray measurement. The reciprocal space map (RSM) for (115) reflection [Fig. 1(b)] shows the $In_{0.5}Ga_{0.5}As$ peak almost lied on the fully relaxed line, which indicates that the

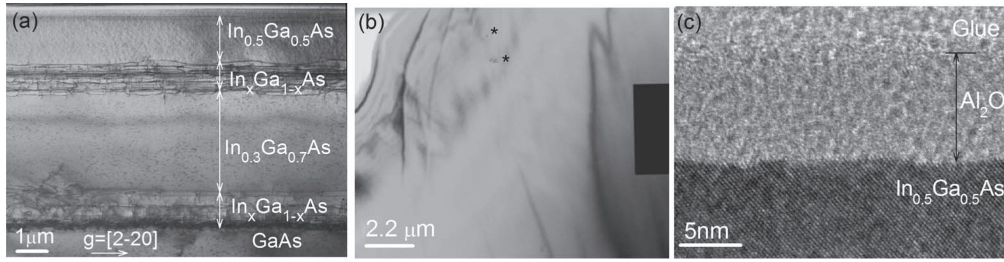

Fig. 2. (a) Cross-sectional two-beam bright-field TEM image and (b) plan-view bright-field TEM of $In_{0.5}Ga_{0.5}As$ film grown on 6° offcut toward [110] GaAs substrate using $In_xGa_{1-x}As$ buffer layers. (c) Cross-sectional HR-TEM image of Al_2O_3/MOCVD-$In_{0.5}Ga_{0.5}As$/GaAs MOSCAP.

epilayer was nearly fully relaxed on GaAs substrate. The results show the good agreement between calculation and experiment methods.

Transmission electron microscopy (TEM) measurement was performed to determine the material quality, thickness of Al_2O_3 layer, and interfacial property between the oxide and the $In_{0.5}Ga_{0.5}As$ semiconductor in MOSCAP structure. A cross-sectional two-beam bright-field TEM image taken near the [110] zone axis with $g = [2\bar{2}0]$ of GaAs substrate of the structure is shown in Fig. 2(a). It is clear that a threading dislocation (TD) was blocked and contained in within the graded buffer layers, resulting in almost no TD extension into $In_{0.5}Ga_{0.5}As$ epifilm on top. The plan-view TEM [Fig. 2(b)] shows only two TDs (appear near two stars masked in the figure) on a large area of 200 μm^2, which indicates that the TD density in the epifilm was about 1×10^6 cm^{-2}. Cross-sectional high-resolution TEM (HR-TEM) image was taken at the interface of $In_{0.5}Ga_{0.5}As$ semiconductor and Al_2O_3 oxide layer as shown in Fig. 2(c). The growth of lattice-mismatch InGaAs on GaAs substrate caused the rougher surface of $In_{0.5}Ga_{0.5}As$ epilayer [15] in comparison to that of lattice-match $In_{0.53}Ga_{0.47}As$/InP [3], [4]. However, it is shown that the InGaAs surface oxide layer was completely removed.

Fig. 3(a) and (b) shows the multifrequency C–V responses of MOCVD-InGaAs/GaAs MOSCAPs and MBE-InGaAs/InP MOSCAPs, respectively. These two types of MOSCAPs show a similar performance with distinct accumulation, depletion, and inversion regions. The C–V behavior of MOCVD-InGaAs/GaAs MOSCAPs is also similar to high-k/MBE-$In_{0.53}Ga_{0.47}As$/InP MOSCAPs reported by other groups [16], [17]. The frequency dispersion in accumulation regime of MOCVD-InGaAs/GaAs MOSCAP is slightly higher than MBE-InGaAs MOSCAPs (2.95% per decade compared with 2.26% per decade). This difference might come from the different series resistances since the substrates of MBE and MOCVD MOSCAPs are different. The difference in depletion capacitance between these two MOSCAPs is due to the difference in doping concentrations in MOCVD-InGaAs and MBE-InGaAs active layers [16]–[18].

To study in detail the performance of MOCVD-InGaAs /GaAs MOSCAPs, conductance and simulation methods were performed. The normalized parallel conductance $(G_p/\omega qA)$ was determined from the measured impedance by [19]

$$\frac{G_p}{\omega qA} = \frac{1}{qA} \times \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \tag{6}$$

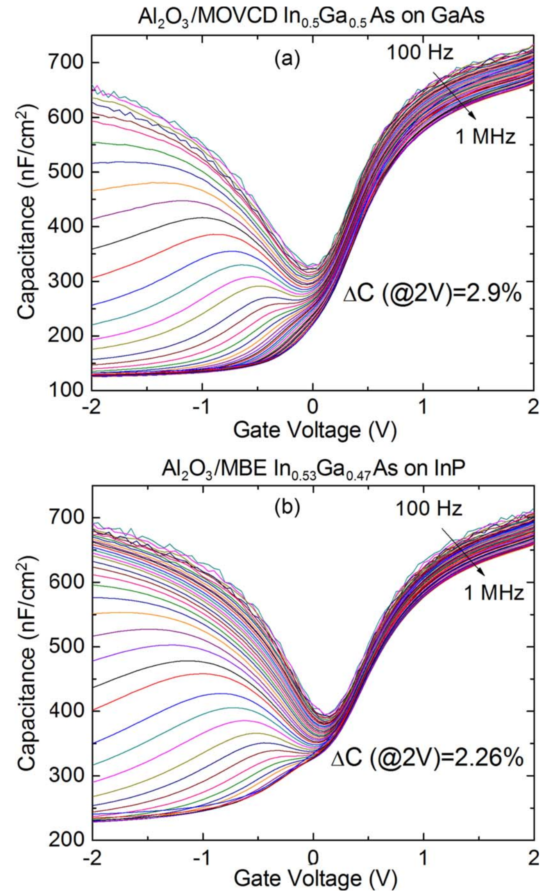

Fig. 3. Multifrequency C–V curves of (a) 9-nm Al_2O_3/MOCVD n-$In_{0.5}Ga_{0.5}As$ on GaAs and (b) 9-nm Al_2O_3/MBE n-$In_{0.53}Ga_{0.47}As$ on InP MOSCAPs.

where A is area of the MOSCAPs, $\omega = 2\pi f$, q is the elementary charge, C_{ox} is the oxide capacitance, C_m is the measured capacitance, and G_m is the measured conductance. The 2-D contour plot of parallel conductance as a function of bias voltage and measurement frequency [20] of the sample is shown in Fig. 4. From the figure, the conductance peak maximum can shift to a frequency of lower than 1 kHz which indicates that the movement of Fermi level into lower part of InGaAs bandgap is possible [20]. However, to claim this issue, future work on the MOCVD InGaAs/GaAs p-MOSCAPs is needed. This will allow to produce the conductance map that shows clearly the free movement of Fermi level in the lower part of InGaAs bandgap [22]. The interface traps density D_{it} is estimated by

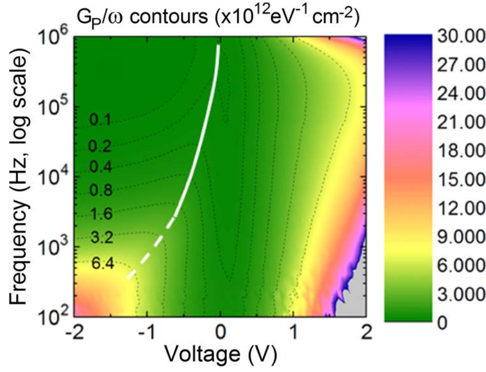

Fig. 4. Characteristics of MOCVD n-$In_{0.5}Ga_{0.5}As$/GaAs MOSCAP: Conductance contours show clearly the (white lines) trace of free movement of the Fermi level.

multiplying the normalize conductance peak value with a factor of 2.5 [19]

$$D_{\mathrm{it}} = 2.5 \times \left(\frac{G_p}{\omega q A}\right)_{\max}. \tag{7}$$

The trap level E_T is estimated from the trap response time $\tau = 2\pi/\omega$, which is given by Shockley–Read–Hall statistic [23]

$$\tau = \frac{1}{\sigma v_{\mathrm{th}} N} \exp\left(\Delta E/kT\right) \tag{8}$$

where ΔE is the energy difference between trap level E_T and majority carrier band edge energy, σ is the capture cross section of the trap, v_{th} is average thermal carrier velocity, N is the effective density of state in the majority carrier band, k is the Boltzmann constant, and T is temperature. The value of the capture cross section $\sigma = 1 \times 10^{-16}$ cm^2 was taken [21]. We admit that the real value of the capture cross section would be different from this value. The real positions of trap level would shift to about 0.06 eV for each order that is different from this 10^{-16} cm^2. Other values of the materials listed in Table I were taken from [24]. The calculation also took into account the limitation of conductance method that the value of D_{it} is reasonable only if $C_{\mathrm{ox}} > qD_{\mathrm{it}}$ [25]. The D_{it} distribution of the two samples estimated by conductance method is shown in Fig. 5(b) (line plus solid symbols).

Fig. 5(a) shows the measured quasi-static and simulated C–V curves of the samples. The low-frequency CV was performed by self-consistent solution of Schrodinger–Poisson equations, similar to the approach in [26]. From the solution of Schrodinger–Poisson equation of ideal MOS structure, the semiconductor capacitance C_S was extracted. The capacitance due to interface traps C_{it} was then calculated from equation given by [19]

$$C_{\mathrm{it}} = \frac{C_{\mathrm{ox}} C_{\mathrm{QS}}}{C_{\mathrm{ox}} - C_{\mathrm{QS}}} - C_S \tag{9}$$

where C_{ox} is the oxide capacitance and C_{QS} is experimental quasi-static capacitance. This would allow extracting the simulated CV curve and again comparing with experimental QSCV data. The parameters of the MOSCAPs such as flatband voltage (V_{FB}) and charge neutral level (E_{CNL}) were modulated by simulation, and the D_{it} profile was extracted until the best fit between simulated and experimental C–V curves was obtained.

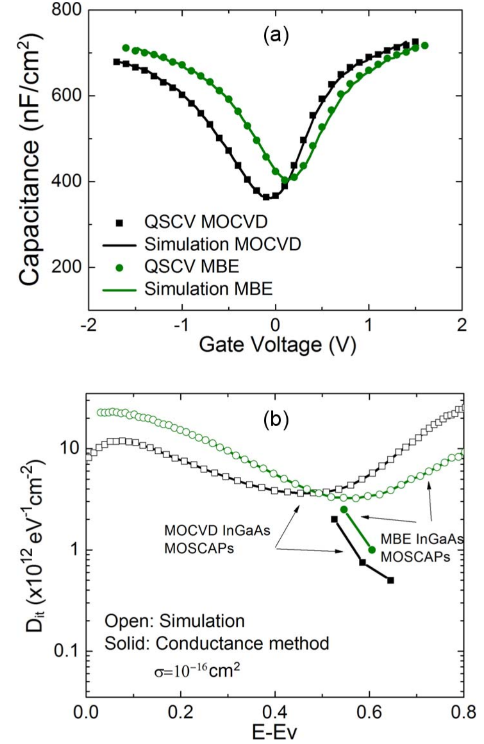

Fig. 5. Characteristics of MOCVD n-$In_{0.5}Ga_{0.5}As$/GaAs and MBE n-$In_{0.5}Ga_{0.5}As$/InP MOSCAPs: (a) (symbols) Experimental quasi-static and (line) simulated C–V curves; (b) D_{it} profiles extracted by simulation and conductance methods.

The wave function penetration into the dielectric layer was not taken into account. The wave function penetration would be more pronounced for the case of 1.5–2-nm thin oxide film, in which the leakage current becomes significant [27]. The trap energy level E was determined from the surface potential φ_s according to the equation [26]

$$E - E_V = E_F - q\varphi_s \tag{10}$$

where E_F is Fermi level and E_V is valence band maximum level. The surface potential was determined from gate bias V_g, which is defined by

$$V_g = V_{\mathrm{FB}} + \varphi_s - \frac{Q_s + Q_{\mathrm{it}}}{C_{\mathrm{ox}}} \tag{11}$$

where Q_s is the semiconductor charge of ideal MOSCAP and Q_{it} is interface charge. The experimental and simulated C–V curves were well fitted to each other. The D_{it} profiles of the two samples extracted by simulation are shown in the Fig. 5(b) as well (line plus open symbols). From the figure, the D_{it} profiles of the two samples extracted by each method are similar. For MOCVD-InGaAs/GaAs MOSCAPs, the D_{it} values of 5×10^{11}–2×10^{12} $\mathrm{eV}^{-1} \cdot \mathrm{cm}^{-2}$ in the energy range of 0.64–0.52 eV above the InGaAs valence band maximum are obtained by conductance method. These values are also comparable to those from other reports [18], [21]. The values of D_{it} obtained by simulation (in the range of 3×10^{12}–2×10^{13} $\mathrm{eV}^{-1} \cdot \mathrm{cm}^{-2}$) are higher than those obtained by conductance method. This difference is because the conductance method only represents *fast* interface traps while low-frequency C–V simulated (QSCV) represents both *fast and slow* interface traps.

IV. Conclusion

In summary, metamorphic epitaxy layer n-$In_{0.5}Ga_{0.5}As$ has been successfully grown on GaAs substrate. TDs have been well confined and blocked within designed graded strained $In_xGa_{1-x}As$ buffer layers, resulting in the TD density of 1×10^6 cm^{-2} in the $In_{0.5}Ga_{0.5}As$ epifilm. The high-quality $In_{0.5}Ga_{0.5}As$/GaAs epifilm allowed us to fabricate good-performance MOSCAP devices on the structure. The performance of MOSCAP devices fabricated on MOCVD $In_{0.5}Ga_{0.5}As$/GaAs wafer is comparable to MBE-$In_{0.53}Ga_{0.47}As$/InP-based MOSCAPs. The devices show nice C–V response, with acceptable frequency dispersion value of 2.9%. The conductance map indicated that the Fermi level could move freely with the gate bias. Good Al_2O_3/InGaAs interface with acceptable D_{it} value of 5×10^{11}–2×10^{12} $eV^{-1} \cdot cm^{-2}$ by conductance method has been obtained. The MOSCAP devices on GaAs substrate in this work can be combined with GaAs/Si growth technique for the future fabricating CMOS devices on Si substrate.

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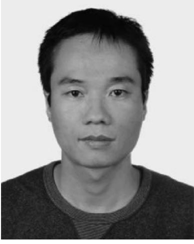

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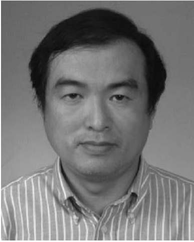

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