Microelectronic Engineering 109 (2013) 302–305

Contents lists available at SciVerse ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

The intrinsic parameter fluctuation on high-κ/metal gate bulk FinFET devices

Yiming Li *, Hsin-Wen Su, Yu-Yu Chen, Sheng-Chia Hsu, Wen-Tsung Huang

Parallel and Scientific Computing Laboratory, Department of Electrical and Computer Engineering, National Chiao Tung University, 1001 Ta-Hsueh Road, Hsinchu 300, Taiwan

ARTICLE INFO

Article history:
Available online 25 March 2013

Keywords:
Random discrete dopant
Random interface trap
Random work function
Characteristic fluctuation
16-nm-gate
Bulk FinET
Statistical 3D device simulation

ABSTRACT

In this work, based on the experimentally calibrated 3D device simulation, we for the first time estimate the impact of intrinsic parameter fluctuation on the electrical characteristic of 16-nm-gate TiN/HfO_2 bulk FinFETs. The sources of intrinsic parameter fluctuation include the random discrete dopants, interface traps and work function differences, simultaneously. The full 3D simulated threshold voltage fluctuation, induced by the aforementioned random sources simultaneously, is 26.2 mV for the N-type bulk FinFET (and is 55.5 mV for the planar N-MOSFET). For the N-type bulk FinFET, the statistical sum of these fluctuations is 9.5% (and is 12.3% for the planar device) overestimation, compared with the full 3D simulation. One of the main reasons is the independence assumption on these random variables is destroyed owing to interactions to different extents among RDs, ITs and WKs. The coupled surface potentials cannot be simply estimated by using their statistical sum of individual random source. Under the same threshold voltage, compared with the result of the planar MOSFETs, more than 50% reduction on the threshold voltage fluctuation of the explored bulk FinFETs is observed owing to the benefit of 3D structural nature.

1. Introduction

Innovation of fabrication process, device material, and vertical channel structure benefits the production of CMOS devices. It continues to support and energize the performance projection of Moore's law [1]. Performance improvement of nanometer scale CMOS devices requires not only overcoming a variety of fabrication challenges but also suppressing systematic variation and random effects [2]. Except the process variation effects, the random effects including random dopants (RDs), interface traps (ITs) and work-functions (WKs) are crucial for device characteristics of nanometer scale planar and vertical silicon channel field effect transistors [3]. DC/AC characteristic fluctuations induced by RDs (RDF), ITs (ITF) and WKs (WKF) on high-κ/metal gate (HKMG) planar MOSFET devices and various circuits were modeled and simulated by using different simulation techniques, recently [4–12]. Studies on the characteristic fluctuation of the bulk and SOI FinFET devices resulting from individual (or pair-wised) random factors have also been reported [13–15]. It will be an interesting topic for us to explore the RDF, ITF, and WKF at the same time on the HKMG bulk FinFETs.

In this study, we estimate the aforementioned three random factors simultaneously on the characteristic fluctuation of 16-nm-gate TiN/HfO_2 bulk FinFETs by using experimentally calibrated 3D quantum-mechanically-corrected device simulation. Full fluctuations are further compared with their statistical sum with respect to planar MOSFETs as well as bulk FinFET devices in the unified analyzing methodology. More than 50% reduction on the threshold voltage fluctuation of the explored 16-nm-gate HKMG bulk FinFETs could be estimated, compared with the result of the planar MOSFETs. The findings of this study indicate that the coupling effect of surface potentials resulting from aforementioned random factors cannot be simply calculated by using their statistical sum of individual random source.

This paper is organized as follows. In the Section 2, we brief the statistical 3D device simulation methodology. In the Section 3, we discuss the simulation results. Finally, we draw conclusions and suggest future work.

2. The statistical device simulation methodology

The devices we studied are the 16-nm-gate bulk FinFETs with AR2. The AR2 is defined by the quotient: AR2 = Fin height/Fin width = 32/16 = 2. The simulated devices are with amorphous-based TiN/HfO_2 gate stacks and an EOT of 0.8 nm. An illustration of the simulated diagram for the 16-nm-gate TiN/HfO_2 bulk FinFET devices is shown in Fig. 1(a). Without the loss of generality, we adopt the structure of AR1 as an example to brief the settings of the 3D statistical device simulation. Fig. 1(b) shows the settings for the RDF in the N-type devices which mainly follows our recent work [8] for the planar MOSFET devices. Notably, we generate 1327 dopants randomly in a large cube of $(96\ nm)^3$ and the equivalent doping concentration is $1.5 \times 10^{18}\ cm^{-3}$. The large cube is partitioned into sub-cubes. The number of dopants in the sub-cubes may vary from 0 to 14, and the average dopant number is 6. These sub-cubes are then mapped into the device channel

* Corresponding author. Tel.: +886 3 5712121x52974; fax: +886 3 5726639.
E-mail address: ymli@faculty.nctu.edu.tw (Y. Li).

0167-9317/$ - see front matter © 2013 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.mee.2013.03.076

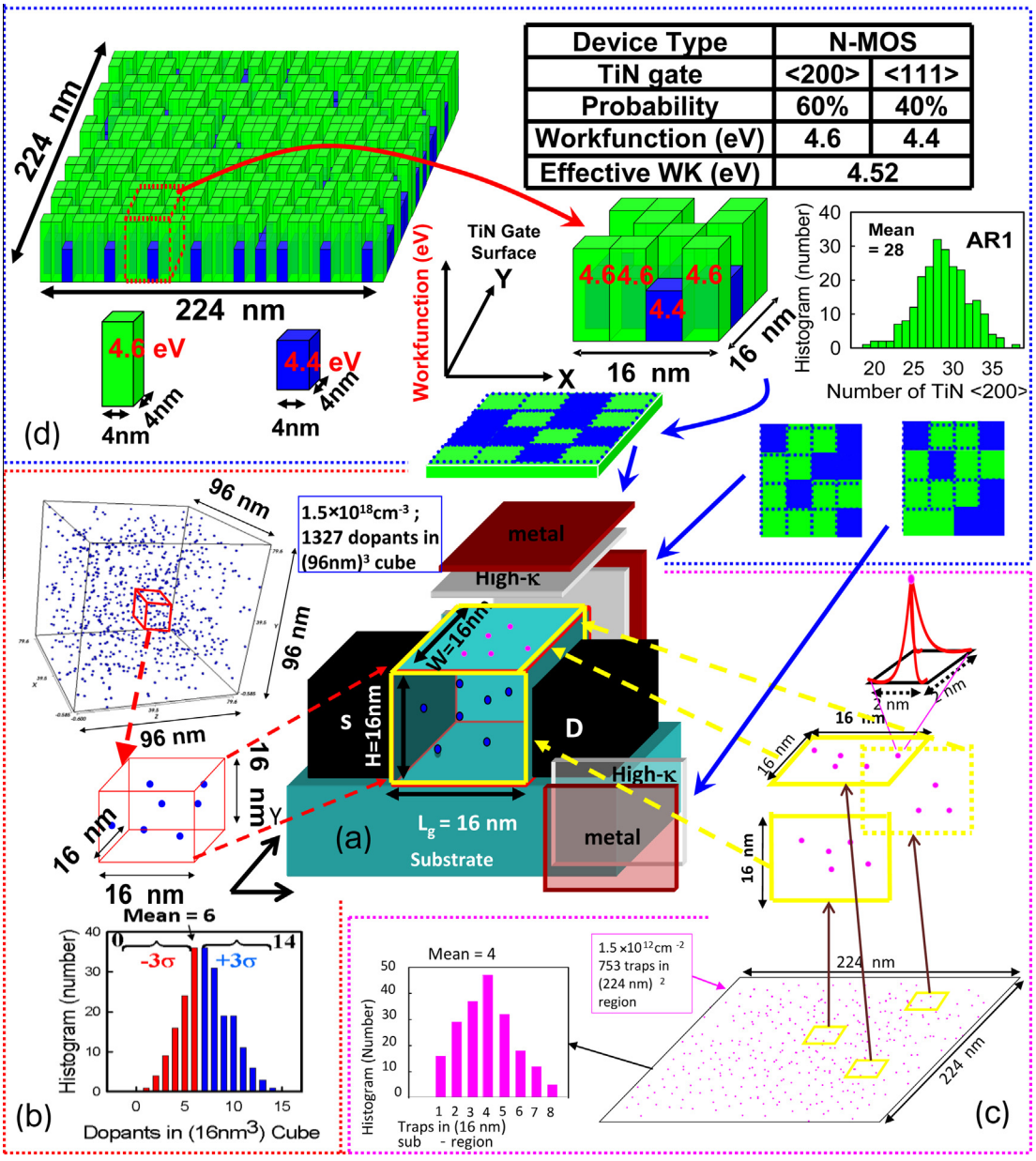

Fig. 1. (a) The diagram of the studied HKMG bulk FinFET with AR1 (AR1 = Fin height/Fin width = 1). The generated devices are with considering RDF, ITF, and WKF, simultaneously. The blue dots are discrete dopants inside the channel and the pink dots are interface traps at the HfO_2/Si interface; the square patterns with green and blue colors are TiN ⟨200⟩ and ⟨111⟩ orientations. (b) 1327 dopants are randomly generated in a large cube of $(96\ nm)^3$, in which the equivalent doping concentration is $1.5 \times 10^{18}\ cm^{-3}$. The large cube is partitioned into sub-cubes which are then mapped into the device channel region for the 3D device simulation. The number of dopants in the sub-cubes may vary from 0 to 14, and the average dopant number is 6. (c) For the settings of ITF, we first generate 2259 acceptor-like traps marked as pink dots in three large 2D planes where the trap's concentration in the large plane is around $1.5 \times 10^{12}\ cm^{-2}$ based upon experimental characterization. Notably, the total number of generated traps follows the Poisson distribution. Then, the statistically random generated large 2D plane is partitioned into many sub-planes, where the number of traps in the sub-planes varies from 1 to 8 and the average number of interface traps is 4. (d) For the settings of WKF, we generate 3136 metal grains randomly in a large area $(224\ nm)^2$, where the grain size are $(4\ nm)^2$ from the empirical data. The work function of each sub-region is totally random according to the material property in the inset table. The number of ⟨200⟩ and ⟨111⟩ orientations is generated with 60% and 40% probabilities.

region. As shown in Fig. 1(c), for the simulation of ITF, we first generate 2259 acceptor-like traps marked as pink dot in three large 2D planes, as shown in Fig. 1(c), where the trap's concentration in the large plane is around $1.5 \times 10^{12}\ cm^{-2}$, based upon experimental characterization, and the total number of generated traps follows the Poisson distribution. Then, the statistically random generated large 2D plane is partitioned into many sub-planes, where the number of traps in the sub-planes varies from 1 to 8 and the average number of interface traps is 4. The energy of each random trap on a sub-plane is random assigned independently. Thus, each trap's density is estimated according to randomly assigned trap's energy [6,7]. As shown in Fig. 1(d), to perform the WKF simulation, we directly partition the metal gate's area into 48 sub-regions following Gaussian distribution, where the number of generated grains in the top and two lateral gates are 16. Note that the variation range of TiN grain's size is dozens of nanometers and we first assume it is equal to $(4\ nm)^2$ according to experimental data [5,15]. The randomly generated small squares approximate arbitrary shape of grains well. According to metal material's property, in our WKF simulation the TiN has two different orientations: ⟨200⟩ and

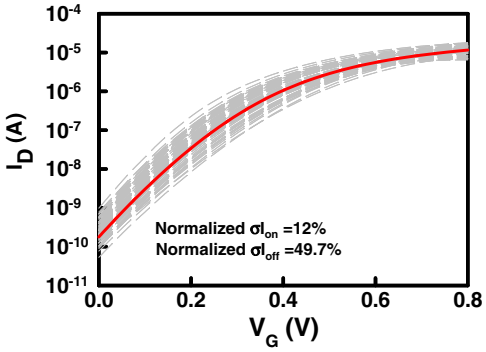

Fig. 2. The I_D–V_G characteristic fluctuated by **ALL** fluctuation factors of the 16-nm-gate HKMG bulk FinFETs with the case of AR2. The red line is the nominal data. The normalized σI_{on} and σI_{off} are 12% and 49.7%, respectively.

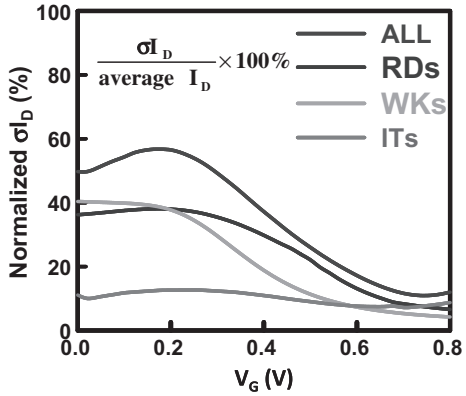

Fig. 3. The normalized σI_D vs. V_G among different random factors. The inset equation is used to calculate the normalized σI_D, where these fluctuations are within 15% when device is operated at high gate bias.

⟨1 1 1⟩ orientations with 60% and 40% generated probabilities where the associated probabilities of WKs are 4.4 eV (blue color) and 4.6 eV (green color) for the N-type bulk FinFETs. Consequently, for the simulation of combined RDF, ITF and WKF, the aforementioned statistical procedure for RDs, ITs, and WKs is first performed respectively and then randomly positioned into the silicon channel, the HfO_2/Si interface, and the gate area of each device simultaneously. For the simulation of characteristic fluctuation of the 16-nm-gate TiN/HfO_2 MOSFET devices, we follow the procedure appearing in the reference [8].

3. Results and discussion

The I_D–V_G resulting from total fluctuations (considering RDs, ITs, and WKs at the same time; denoted as **ALL**) is shown in Fig. 2. The red line is the nominal data. The normalization of σI_{on} and σI_{off} are 12% and 49.7% respectively. The fluctuation of off-state current is directly propositional to the fluctuation of threshold voltage, so the σI_{off} is significant for devices operated at low gate bias owing to significant fluctuation of threshold voltage; nevertheless, it could be suppressed for devices operated at the high gate bias. Fig. 3 shows the normalized σI_D vs. V_G; among fluctuations; the fluctuation sources RDs, WKs, and **ALL** affect the subthreshold region of the device and the normalized drain current fluctuations decrease drastically as the gate bias increases except ITs because the screening effect is weakened with respect to the random ITs appearing on the HfO_2/Si interface. The devices with random ITs appearing on the HfO_2/Si interface have relatively larger normalized drain current fluctuation among three random factors at the high gate bias. However, they could be ignored when the device operates in the condition of strong inversion. For the same threshold voltage, Fig. 4 further shows the σV_{th} induced by RDs, ITs, WKs, **ALL**, and **SUM**, for the 16-nm-gate planar and bulk FinFET devices, respectively. The **SUM** is calculated by the statistical summation of the variances among the three random variables RDs, ITs, and WKs as expressed in the inset formula. The main assumption to this calculation replies on the identically independent distribution (iid) for these three random variables: RDs, ITS, and WKs. The **ALL** is that 3D device simulation of fully coupled with considering RDs, ITs and WKs at the same time. The assumption of iid to RDs, ITs, and WKs has resulted in overestimation on the threshold voltage fluctuation because it does not consider the surface potential's interaction among the three random variables. On the contrary, the results of **ALL**, based upon the unified 3D device simulation, find 12% and 8.7% overestimations of the threshold voltage fluctuations calculated by the statistical sum of the variances of RDs, ITs, and WKs on the 16-nm planar MOSFETs and bulk FinFETs. Notably, the results of characteristic fluctuation of the 16-nm-gate TiN/HfO_2 MOSFET devices are directly from our recent study in [8]. The difference between the ALL and SUM of It is because that the **ALL** calculation simulates the device characteristic suffering from fully coupled random sources at the same time. Consequently, both the enhanced and/or cancelled out interactions of surface potentials resulting from various random natures such as the random location, random number, random energy, and random orientation of the RDs, ITs, and WKs are simultaneously considered.

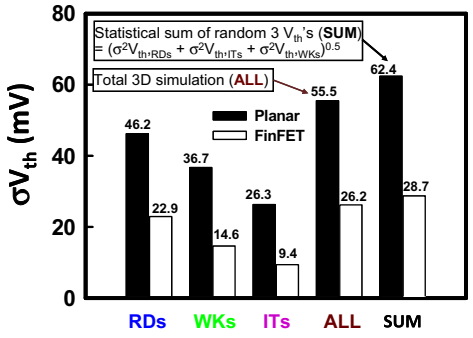

Fig. 4. The σV_{th} for the 16-nm-gate HKMG planar MOSFETs and the 16-nm-gate HKMG bulk FinFET devices induced by the RDs, ITs, WKs, **ALL**, and **SUM**, respectively. Benefiting from the structural nature, the bulk FinFET has more than 50% reduction on the threshold voltage fluctuation, compared with the result of planar MOSFET, when device suffer **ALL** fluctuations.

The significant interaction among RDs, ITs, and WKs could be explained, as shown in Fig. 5, where the nominal V_{th} = 250 mV. The simulated surface current densities and potential profiles (from the source (S) to the drain (D)) are with respect to statistically generated patterns of RDs, ITs, WKs, and **ALL**, respectively. As shown in Fig. 5a–c, simply considering individual random source may overestimate (or underestimate) the amplitude of V_{th}. We firstly examine each fluctuated surface potential resulting from the RDS, ITs, and WKs, respectively. We then observe that device suffers from **ALL** random sources possesses much smoother surface potential, as shown in Fig. 5d. Considering **ALL** factors within a device, the amplitude of V_{th} = 252.2 mV is similar to the value of the nominal V_{th} owing to canceling effect the random interactions.

4. Conclusions

We used an experimentally validated 3D device simulation to study the characteristic fluctuation of the 16-nm-gate TiN/HfO_2

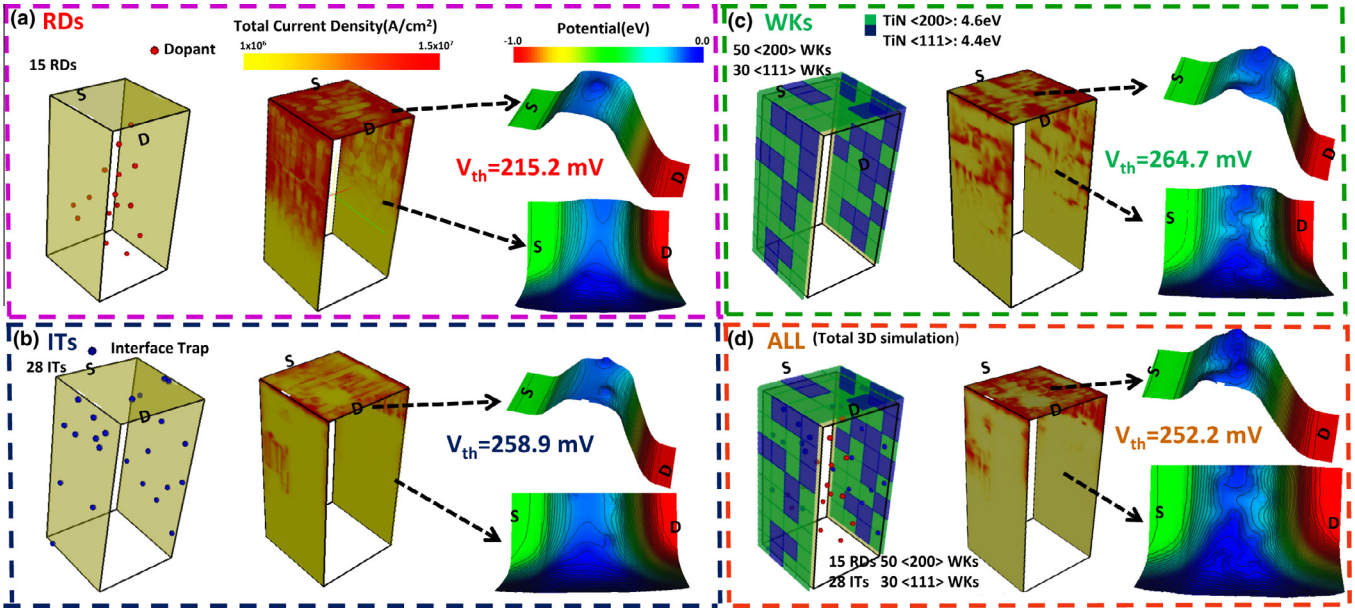

Fig. 5. (a–d) are the devices (nominal V_{th} = 250 mV) with statistically generated random patterns, the simulated surface current densities and potential profiles (from the source (S) to the drain (D)) with respect to RDs, ITs, WKs, and ALL, respectively. Surface potential's interaction is observed from the top gate and one of the lateral gates for device suffers from **ALL** random sources which shows different potential profiles compared with RDs, ITs, and WKs.

bulk FinFET devices. We have explored the difference of fluctuations induced by RDs, ITs and WKs. We have further estimated the characteristic fluctuation by using a statistical sum of three random fluctuation sources and fully coupled simulation for all factors. More than 50% σV_{th} reduction on the threshold voltage fluctuation of the simulated bulk FinFETs has been observed, compared with the result of the planar MOSFETs. The coupling effect of surface potentials resulting from different random sources cannot be directly summated together. Thus, the full 3D simulated threshold voltage fluctuation is 26.2 mV for the N-type bulk FinFET. However, a statistical sum of these fluctuations is 9.5% overestimation owing to the invalid independence assumption on the random variables. The dependency is affected to different extents by what the random interactions among RDs, ITs and WKs. Devices' variability is affected to different extents by their structure, dimension, and existing random factors. It is necessary to investigate the characteristic fluctuation by simulating fully coupled random sources simultaneously.

Acknowledgements

This work was supported in part by National Science Council (NSC), Taiwan under Contract No. NSC 101-2221-E-009-092 and by tsmc, Hsinchu, Taiwan under a 2012–2013 grant.

References

[1] K.J. Kuhn, U. Avci, A. Cappellani, M.D. Giles, M. Haverty, S. Kim, R. Kotlyar, S. Manipatruni, D. Nikonov, C. Pawashe, M. Radosavljevic, R. Rios, S. Shankar, R. Vedula, R.Chaul. Young, IEDM Tech. Dig. (2012) 171–174.
[2] K.J. Kuhn, M.D. Giles, D. Becher, P. Kolar, A. Kornfeld, R. Kotlyar, S.T. Ma, A. Maheshwari, S. Mudanai, IEEE Trans. Electron Devices 58 (2011) 2197–2208.
[3] Y. Li, C.-H. Hwang, T.-Y. Li, M.-H. Han, IEEE Trans. Electron Devices 57 (2010) 437–444.
[4] Asenov, S. Roy, R.A. Brown, G. Roy, C. Alexander, C. Riddet, C. Millar, B. Cheng, A. Martinez, N. Seoane, D. Reid, M.F. Bukhori, X. Wang, U. Kovac, IEDM Tech. Dig. (2008) 1–4.
[5] X. Zhang, J. Li, M. Grubbs, M. Deal, B. Magyari-Kope, B.M. Clemens, Y. Nishi, IEDM Tech. Dig. (2009) 57–60.
[6] P. Andricciola, H.P. Tuinhout, B. De Vries, N.A.H. Wils, A.J. Scholten, D.B.M. Klaassen, IEDM Tech. Dig. (2009) 711–714.
[7] H.-W. Cheng, F.-H. Li, M.-H. Han, C.-Y. Yiu, C.-H. Yu, K.-F. Lee, Y. Li, IEDM Tech. Dig. (2010) 379–382.
[8] Y. Li, H.-W. Cheng, Y.-Y. Chiu, C.-Y. Yiu, H.-W. Su, IEDM Tech. Dig. (2011) 107–110.
[9] Y. Li, S.-M. Yu, J.-R. Hwang, F.-L. Yang, IEEE Trans. Electron Devices 55 (2008) 1449–1455.
[10] Y. Li, C.-H. Hwang, IEEE Trans. Microwave Theory Tech. 56 (2008) 2726–2733.
[11] Y. Li, C.-H. Hwang, T.-Y. Li, IEEE Trans. Electron Devices 56 (2009) 1588–1597.
[12] Y. Li, H.-W. Cheng, M.-H. Han, IEEE Trans. Semicond. Manuf. 23 (2010) 509–516.
[13] X. Wang1, A.R. Brown, B. Cheng, A. Asenov, IEDM Tech. Dig. (2011) 103–106.
[14] H.-W. Cheng, Y. Li, C.-Y. Yiu, H.-W. Su, IEEE Int.l Conf. Simul. Semicond. Processes Devices (2011) 287–290.
[15] T. Matsukawa, Y. Liu, W. Mizubayashi, J. Tsukada, H. Yamauchi, K. Endo, Y. Ishikawa, S.-I. O'uchi, H. Ota, S. Migita, Y. Morita, M. Masahara, IEDM Tech. Dig. (2012) 175–178.