On the Origin of Gate-Induced Floating-Body Effect in PD SOI p-MOSFETs

Chih-Hao Dai, Ting-Chang Chang, An-Kuo Chu, Yuan-Jui Kuo, Fu-Yen Jian, Wen-Hung Lo, Szu-Han Ho, Ching-En Chen, Wan-Lin Chung, Jou-Miao Shih, Guangrui Xia, Osbert Cheng, and Cheng-Tung Huang

***Abstract*—This letter systematically investigates the origin of gate-induced floating-body effect (GIFBE) in partially depleted silicon-on-insulator p-type MOSFETs. The experimental results indicate that GIFBE causes a reduction in the electrical oxide field, leading to an underestimate of negative-bias temperature instability degradation. This can be partially attributed to the electrons tunneling from the process-induced partial n^+ polygate. However, based on different operation conditions, we found that the dominant origin of electrons was strongly dependent on holes in the inversion layer under source/drain grounding. This suggests that the mechanism of GIFBE at higher voltages is dominated by the proposed anode electron injection model, rather than the electron valence band tunneling widely accepted as the mechanism for n-MOSFETs.**

***Index Terms*—EVB tunneling, gate-induced floating-body effect (GIFBE), negative-bias temperature instability (NBTI), silicon-on-insulator (SOI).**

I. Introduction

SILICON-ON-INSULATOR (SOI) CMOS devices are attractive since they provide high current drivability and reduced junction capacitance when compared to bulk-Si devices [1]. However, for partially depleted (PD) SOI devices, due to their relatively thick thin films, the impact-ionization mechanism near the drain will cause the ionization charges to accumulate in the neutral region, leading to the instability of body potential [2]. With aggressive scaling of the gate oxide, the floating-body (FB) potential is controlled not only by well-known impact-ionization mechanisms but also by a gradual increase of the tunneling current. This new FB effect, called gate-induced FB effect (GIFBE), has been observed in both PD SOI MOSFETs [3], [4] and fully depleted transistors [5]. Although this FB effect can be used in digital designs to enhance the drain current, owing to the reduction in threshold voltage, analog designs are restricted when the operation point is near the kink region. Therefore, to prevent GIFBE, body-tied-with-T-gate configurations for PD SOI devices have been used widely [6]–[8]. However, due to the disappearance of the FB effect, the promotion of drain current is strongly limited in digital designs. Therefore, the body-tied devices are usually operated in FB or ground-body (GB) situations for analog and digital designs, respectively.

In addition, GIFBE has been reported to reduce negative-bias temperature instability (NBTI) degradation for PD SOI p-MOSFETs with FB condition [9], [10]. The electrons generated by NBTI stress accumulate in the body, resulting in a decrease in electrical oxide field, owing to the increase of the body potential. However, the origin of these electrons is not clear yet due to the fact that the electron concentration is insufficient in the p^+ polygate of p-MOSFETs. To the best of our knowledge, several studies consider that the model of electron valence band (EVB) tunneling should be responsible for the GIFBE in SOI n-MOSFETs [3]–[5]. However, there are a few studies confirming the validity of this mechanism for p-MOSFETs. Therefore, the aim of this work is to clarify the origin of electrons on the GIFBE in PD SOI p-MOSFETs by adopting systematical operation conditions. The experimental results reveal that the GIFBE in p-MOSFETs can be partially attributed to the process-induced partial n^+ polygate of body-tied devices. However, the major electron source generated by NBTI stress is significantly related to the inversion channel supplied from the source and drain. Therefore, we propose the anode electron injection (AEI) model, which is similar to the anode hole injection (AHI) model [11], to explain how this main electron origin is generated during NBTI.

II. Experiment

Using 65-nm SOI CMOS technology, PD SOI p-MOSFETs with p^+ polygate are employed in a T-gate structure to investigate the GIFBE mechanism. The top view of the body-tied device is shown in the inset of Fig. 1. The distance from the body contact to the active region is 0.35 μm. The silicon film and buried oxide thicknesses for the devices are 75 and 145 nm, respectively. The gate oxide with a thickness of 12 Å was grown by *in situ* steam generation, with the channel doping concentration about 3×10^{18} cm^{-3}. The channel current flows in the $\langle 110 \rangle$ direction on the (100) substrate. In this work, devices with channel lengths (L) and widths (W) both in the range of 1 μm–65 nm were selected. To confirm the FB effect on NBTI degradation, the body-tied devices were subject to

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C.-H. Dai, A.-K. Chu, and Y.-J. Kuo are with the Department of Photonics, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan.

T.-C. Chang is with the Department of Photonics, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan. He is also with the Department of Physics, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan, and also with the Center for Nanoscience and Nanotechnology, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan (e-mail: tcchang@mail.phys.nsysu.edu.tw).

F.-Y. Jian, S.-H. Ho, and C.-E. Chen are with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan.

W.-H. Lo, W.-L. Chung, and J.-M. Shih are with the Department of Physics, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan.

G. Xia is with the Department of Materials Engineering, The University of British Columbia, Vancouver, BC V6T 1Z4, Canada.

O. Cheng and C.-T. Huang are with the Device Department, United Microelectronics Corporation, Tainan 744, Taiwan.

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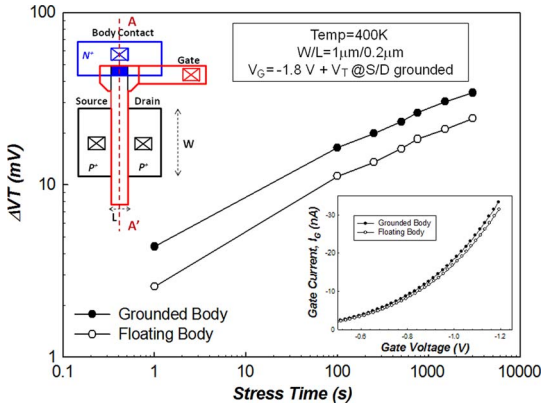

Fig. 1. NBTI-induced threshold voltage shift versus stress time for SOI p-MOSFETs under GB and FB operations. The inset shows the top view of the T-gate structure and the gate current comparison of GB and FB devices.

NBTI test under FB and GB conditions. A gate voltage of $-1.8\ \text{V} + V_T$ was applied to the gate electrode at 400 K during NBTI, while the source and drain electrodes were grounded. The threshold voltage (V_T) was defined as the gate voltage for which the drain current is equal to 70 nA $\times$ (W/L) in the linear region. All electrical characteristics were measured using an Agilent B1500 semiconductor parameter analyzer.

III. Results and Discussion

Fig. 1 shows the NBTI-induced V_T shift for the PD SOI p-MOSFETs under FB and GB operations. It can be clearly observed that the NBTI degradation under the FB condition is less than that under the GB condition. This can be attributed to the electron accumulation in the body, which effectively lowers the oxide field for FB devices during stress, thereby reducing NBTI degradation. That the lowering of the electrical oxide field is induced by electron accumulation can be supported by the reduction in the gate leakage current (I_G) under FB condition, as shown in the inset of Fig. 1.

To examine these additional carriers (electrons), Fig. 2 shows I_G and the body current (I_B) versus the gate voltage (V_G) for different p^+ polygate areas (1–0.2 μm^2), while the source/drain (*S/D*) and body are grounded. It can be seen that I_B has a significant enhancement as I_G increases, which means that the source of I_B is strongly dependent on I_G. In addition, regardless of the different polygate areas, I_B always shows a linear increase until about $V_G = -1$ V and then shows an exponential increase beyond that point. This phenomenon implies that the two mechanisms closely related to the gate leakage current should be responsible for these two respective I_B stages. It has been reported that I_G consists of the following components as shown in the inset of Fig. 2: 1) hole tunneling from the valence band (HVB); 2) electron tunneling from the valence band (EVB); and 3) electron tunneling from the conduction band (ECB) [12], [13]. Both ECB and EVB tunneling components can be observed from the body terminal. The two stages of increase in I_B seem to be contributions from these respective tunneling currents. The ECB tunneling first occurs as a gate bias is applied. Then, when the gate bias is large enough, the EVB tunneling induces additional electrons, leading to the second increase of I_B. However, due to the negligible electron concentration in the p^+ polygate, it is impossible for ECB tunneling to occur from this region and result in the pronounced

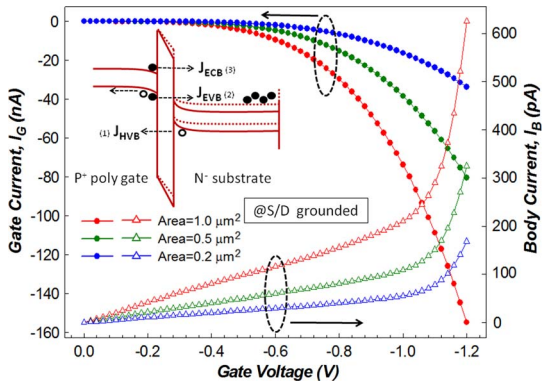

Fig. 2. I_G–V_G and I_B–V_G curves for different p^+ polygate areas. The inset shows the schematic diagrams of the different gate tunneling components in an ultrathin-gate-oxide p-MOSFET.

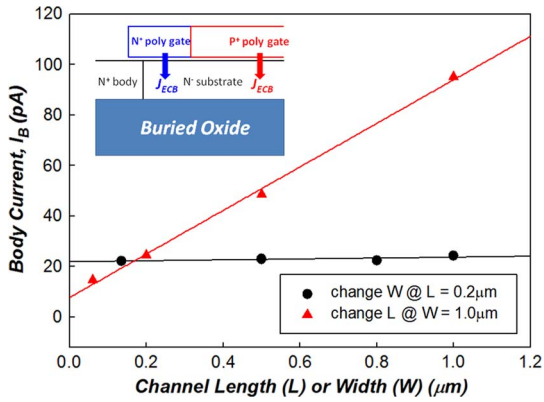

Fig. 3. I_B for various W and L dimensions. I_B is obtained from the gate voltage of -0.5 V while *S/D* is grounded. The inset shows the cross-sectional view taken from line A$-$A$'$ in the top view of the T-gate structure, illustrating the p^+ polygate, the partial n^+ polygate, and the n^- substrate.

I_B increase as the gate bias is applied. The possible region providing sufficient electrons can be attributed to the partial n^+ polygate area of body-tied devices.

By cutting the T-gate structure along A–A$'$ as shown in Fig. 1, a cross-sectional structure can be obtained and is shown in the inset of Fig. 3. It can be observed that part of the polygate area near the body contact has been covered by an n^+ implant to produce the extra body terminal. Therefore, the ECB tunneling current becomes significant between the n^+ portion of the polygate and the n-substrate, resulting in the gradual increase of I_B as the gate bias is applied. This can be confirmed by examining devices of various widths and lengths, as shown in Fig. 3. The result indicates that the first stage of I_B has only linear dependence with length, rather than width, which verifies that these electrons are tunneling from a partial area of the polygate, corresponding to the blue region in the top view of the T-gate structure.

However, the exponential increase of I_B beyond V_G of -1 V indicates that the larger number of electrons induces the FB effect to become more pronounced. According to the I_G tunneling model, this would seem to be caused by the EVB tunneling mechanism, as shown in the inset of Fig. 2. Under a sufficiently large vertical electric field, electrons tunnel from the valence band of the polygate Si to the Si substrate conduction band. However, it has been reported that EVB tunneling current only occurs when the gate bias is larger than -1.1 V in order to make

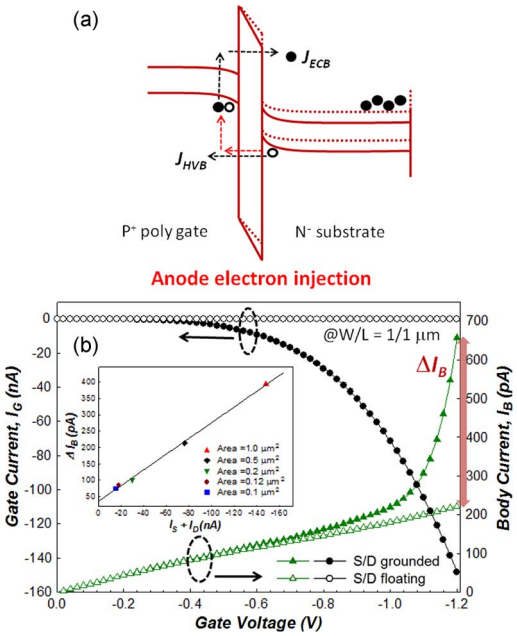

Fig. 4. (a) Schematic diagram of the AEI model for an ultrathin gate oxide in PD SOI p-MOSFETs. (b) I_G–V_G and I_B–V_G characteristics for PD SOI p-MOSFETs under *S/D* floating and grounded operations. The inset shows the linear relationship between ΔI_B and $I_S + I_D$ from the different p^+ polygate areas. I_S and I_D are measured under the grounded *S/D* condition while $V_G = -1.2$ V. ΔI_B is obtained by subtracting the ECB component from the second increase of I_B.

the valence band energy level in the Si substrate align with the gate conduction band [12]. Therefore, we propose another possible mechanism that is similar to the AHI model, i.e., that of AEI, shown in Fig. 4(a), to explain this exponential increase of I_B. In AEI, if the gate oxide is thin enough, holes can still tunnel from the inversion layer to the polygate (anode) and generate hot electrons by impact ionization in the polydepletion region. Then, these hot electrons can inject over or through the anode/oxide interface energy barrier and traverse the oxide layer to the body (cathode).

To further confirm the validity of this mechanism, two operation conditions are performed to distinguish the different sources of I_G that result in electron accumulation. We measured I_G and I_B versus V_G of the device under floating and grounded *S/D* operations. The result under *S/D* floating operation is shown in Fig. 4(b), where it can be clearly observed that the gate leakage current becomes insignificant because the *S/D* cannot supply sufficient minority carriers (holes) to the inversion layer. In addition, under this operation, I_B exhibits only the linear component of the ECB tunneling as discussed earlier. On the contrary, under grounded *S/D* operation, I_G shows a very pronounced increase, as well as the appearance of the second increase of I_B. This proves that the exponential increase of I_B can be attributed to the holes in the inversion layer supplied from the *S/D* rather than the electron–hole pair separated in the valence band of the p^+ polygate. In addition, our experimental results from the different p^+ polygate areas indicate that the AEI-induced electron current has a linear dependence on the hole current tunneling from the inversion layer, as shown in the inset of Fig. 4(b). $I_S + I_D$ depicts the hole tunneling current from the inversion layer. ΔI_B is the pure AEI-induced electron current, which is obtained by subtracting the ECB component from the second increase of I_B. This relationship is consistent with that in the AHI model [11], which means that AEI indeed exists and is the dominant mechanism responsible for the GIFBE in PD SOI p-MOSFETs.

IV. Conclusion

This letter has investigated the origin of electron accumulation on the GIFBE in PD SOI p-MOSFETs. These additional electrons induce oxide field lowering and cause a reduction of NBTI degradation. They can be attributed to two mechanisms corresponding to the stages of the increase in I_B. The first stage is induced by ECB tunneling from the partial n^+ polygate area of the body-tied device. Based on systematic operation conditions, the exponential increase in I_B has been found to be due to the holes of the inversion layer supplied from the *S/D*. This demonstrates that the GIFBE in p-MOSFETs is dominated by the AEI model at higher voltages, rather than the EVB tunneling which is widely accepted for n-MOSFETs.

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References

[1] J. C. Sturm, K. Tokunaga, and J. P. Colinge, "Increased drain saturation current in ultra-thin silicon-on-insulator (SOI) MOS transistors," *IEEE Electron Device Lett.*, vol. 9, no. 9, pp. 460–463, Sep. 1988.

[2] S. Abo, M. Mizutani, K. Nakayama, T. Takaoka, T. Iwamatsu, Y. Yamaguchi, S. Maegawa, T. Nishimura, A. Kunomura, Y. Horino, and M. Takai, "Instability study of partially depleted SOI-MOSFET due to floating body effect using high energy nuclear microprobes," in *Proc. Conf. Ion Implantation Technol.*, 2000, pp. 285–288.

[3] A. Mercha, J. M. Rafi, E. Simoen, E. Augendre, and C. Claeys, ""Linear kink effect" induced by electron valence band tunneling in ultrathin gate oxide bulk and SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 7, pp. 1675–1682, Jul. 2003.

[4] J. Pretet, T. Matsumoto, T. Poiroux, S. Cristoloveanu, R. Gwoziecki, C. Raynaud, A. Roveda, and H. Brut, "New mechanism of body charging in partially depleted SOI-MOSFETs with ultra-thin gate oxides," in *Proc. ESSDERC*, 2002, pp. 515–518.

[5] M. Casse, J. Pretet, S. Cristoloveanu, T. Poiroux, C. Fenouillet-Beranger, F. Fmleux, C. Raynaud, and G. Reimbold, "Gate-induced floating-body effect in fully depleted SOI MOSFETs with tunneling gate oxide and back-gate biasing," *Solid State Electron.*, vol. 48, no. 7, pp. 1243–1247, Jul. 2004.

[6] H. Lin, J. Lin, and R. C. Chang, "Inversion-layer induced body current in SOI MOSFETs with body contacts," *IEEE Electron Device Lett.*, vol. 24, no. 2, pp. 111–113, Feb. 2003.

[7] W. C. Lo, S. J. Chang, C. Y. Chang, and T. S. Chao, "Impacts of gate structure on dynamic threshold SOI nMOSFETs," *IEEE Electron Device Lett.*, vol. 23, no. 8, pp. 497–499, Aug. 2002.

[8] C. Y. Chang, S. J. Chang, T. S. Chao, S. D. Wu, and T. Y. Huang, "Reduced reverse narrow channel effect in thin SOI nMOSFETs," *IEEE Electron Device Lett.*, vol. 21, no. 9, pp. 460–462, Sep. 2000.

[9] R. Mishra, D. E. Ioannou, S. Mitra, and R. Gauthier, "Effect of floating-body and stress bias on NBTI and HCI on 65-nm SOI pMOSFETs," *IEEE Electron Device Lett.*, vol. 29, no. 3, pp. 262–264, Mar. 2008.

[10] G. Nayereh, A. K. Ali, and A. S. Ebrahim, "Modeling of floating-body effect on negative bias temperature instability degradation of double-gate MOSFETs," in *Proc. ICEE*, 2010, pp. 356–361.

[11] K. F. Schuegraf and C. Hu, "Hole injection SiO_2 breakdown model for very low voltage lifetime extrapolation," *IEEE Trans. Electron Devices*, vol. 41, no. 5, pp. 761–767, May 1994.

[12] W. C. Lee and C. Hu, "Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence-band electron and hole tunneling," *IEEE Trans. Electron Devices*, vol. 48, no. 7, pp. 1366–1373, Jul. 2001.

[13] J. W. Yang, J. G. Fossum, G. O. Workman, and C. L. Huang, "A physical model for gate-to-body tunneling current and its effects on floating-body PD/SOI CMOS devices and circuits," *Solid-State Electron.*, vol. 48, no. 2, pp. 259–270, Feb. 2004.