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Package routability- and IR-drop-aware finger/pad planning for single chip and stacking IC designs

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ABSTRACT

Due to the increasing complexity of the design interactions between the chip and package, it is necessary to consider them at the same time. In order to simultaneously handle chip and package performances, co-design of chip and package is a widely adopted solution, particularly because the finger/pad locations significantly affect IR-drop of the core and the package routing. In this paper, we develop chip-package co-design techniques to determine the locations of the fingers/pads for package routability and signal integrity concerns in IC designs, this method can be used in the 2-D and stacking IC design. Our finger/pad assignment is a two-step method: we first solve the wire congestion problem in package routing, and then try to minimize the IR-drop violation and the length of the bonding wires under a compact IR-drop model. The experimental results are encouraging. Compared with the randomly optimized method, on average, our approaches reduce the maximum package density by 42% and 68% for both technologies, IR-drop by 10.61% and 4.58%; and the bonding wires is reduced by 15.66% if we use stacking chips.

Introduction

As VLSI technology enters the nanometer era, chips contain more functions and are expected to have much better performance. At the same time, finger/pad (finger is called landing pad in some parts of package papers and patents) counts are continually increased. This adds up to more routing complexity in the package design. In early package technologies, the number of available finger/pads was small, such as Dual In-line Package (DIP) or Pin Grid Array (PGA). Ball Grid Array (BGA) is a popular package technology for modern package design because it can handle high finger/pad counts to connect to the Printed Circuit Board (PCB). The package design flow can be divided into several parts, as shown in Fig. 1(A). Among the major design problems in package design, routing should be paid more attention.

Many researchers [20,10,14,16] have proposed various approaches to solving the routing problem in package design. Using finger/pad assignments to improve the package routing is another alternative. In [9,15,1], the authors proposed numerous assignment algorithms to improve the routing problem. Because these methods can only handle a small finger count (<20) and the finger count of a modern chip is more than 100, we cannot utilize previous methods to improve the package routing in modern chip designs.

In addition, most package designers only consider the package issue when they plan the finger/pad locations. In reality, the finger/pad not only affects the package routing, but also impacts the noise margin of the core. In modern chip designs, supply voltages continue to drop. This condition helps to reduce power dissipation, but also decreases the noise margin of devices. Noise margin interference will sometimes lead to erroneous chip functions, seriously reducing chip performance. As a result, the integrity problem has become one of the major factors affecting chip yield. Basically, integrity issues can be categorized into signal integrity problems and power integrity problems. IR-drop is one of the important factors in power integrity. Many researchers have proposed various approaches to solving this problem in every design stage. A power/ground (P/G) network design [18,4] is an effective way to address IR-drop problems. IR-drop can be greatly improved by a better P/G network with minimal penalty costs. Besides planning the power/ground (P/G) network, adjusting the power pad location is a common approach to reducing IR-drop noise. In [3], the authors proposed a pad assignment method to improve IR-drop.

On the other hand, stacking style Integrated Circuit (IC) is another solution when we want to develop a high-density high-performance IC. Stacking technology is used to stack a die (chip, wafer) over another die (chip, wafer). Compared with a 2-D IC, when stacking ICs, the total wire length and size of the chip

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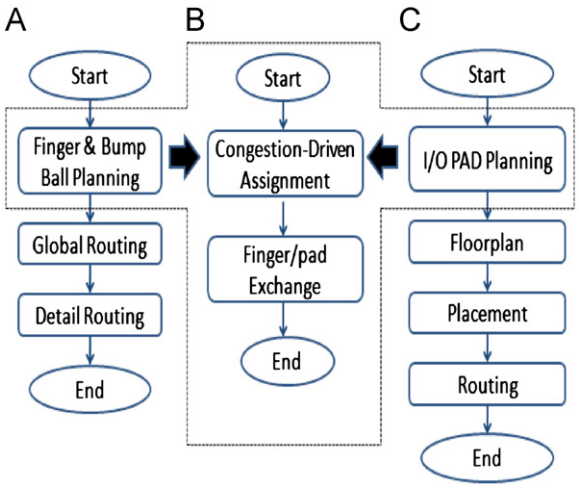

Fig. 1. The traditional flow of package design is shown in (A) and physical design is shown in (C). We propose a method to simultaneously improve package and core performances, and shorten the turn-around time, as shown in (B).

shrinks because of the vertical interconnections. Because the resistance of the total wire length is decreased, the performance and power consumption can be greatly improved. Although stacking ICs have many advantages, the package of a stacking IC is more complex than a 2-D IC. A better planning method, which can handle a large number of finger/pads and the stacking factor, is needed in modern package design.

This paper enhances the proposed method in [12] to simultaneously improving the package congestion, the length of bonding wires, and IR-drop of the core at the finger/pad assignment step for 2-D and stacking ICs. This approach includes one congestion-driven assignment and one finger/pad exchange approach, as shown in Fig. 1(B). Our contributions in this paper are summarized as follows:

- We present a finger/pad assignment method to minimize the maximum wire congestion, and propose a finger/pad exchange method to improve IR-drop of the core in a stacking IC design. The assignment result can certainly lead to a legal routing solution.
- We propose an efficient estimation to obtain the wire congestion map before routing. This method does not need to analyze the whole substrate, and it can directly find the most congested region.
- We developed a co-design methodology to simultaneously improve the problems with the package and core in (stacking) ICs. The turn-around time for the chip design can be greatly shortened.

The rest of this paper is organized as follows. Section 2 describes the package architecture in 2-D and stacking ICs, finger/pad assignment design with congestion and IR-drop consideration, and the problem formulation. Section 3 presents two congestion-driven assignment methods and one finger/pad exchange method to improve package problems and IR-drop. Section 4 shows experimental results, and Section 5 presents conclusions.

Congestion and IR-drop violation minimization in finger/pad planning

As VLSI technology enters the nanometer era, chips contain more and more functions. To deliver great data, finger/pad counts are continually increased and the complexity of package routing is greatly raised. In addition, the IR-drop issue seriously impacts the performance for the chip. The finger/pads not only affect the package routing, but also impact IR-drop of the core. This section focuses primarily on these problems. We first introduce our package model, and then the problems of the package routing and IR-drop are described. Finally, we formulate the target problem in this work.

Architecture and routing of BGA Package

Based on modern package technology, we can utilize multiple layers for package routing. In our package model, there are two layers for routing, the die on the top layer of the substrate, and the bump balls on the bottom layer of the substrate. The fingers are to deliver data from the pad to the package substrate, and these are placed as a rectangle on Layer 1. The pads are connected to the fingers by wire-bond and flip-chip [6] technologies. Here we adopt the wire-bonding technology to connect the die and the package substrate in our package module due to the design cost. The detailed architecture is shown in Fig. 2. Fig. 2(A) shows the vertical view and (B) is the profile. Bump balls, which are connected to the printed circuit board, are uniformly distributed on Layer 2. The net between the finger and the bump ball is implemented within a package substrate on Layer 1 and Layer 2. The function of the via is to connect a wire on Layer 1 and another wire on Layer 2, as shown in Fig. 2(B). In addition, we partition the package area into four parts and solve the package problems individually (as used in [10]). We also assume that the finger order and the pad order are the same.

Because the number of vias affects the performance and the area of the package, we stipulate that the number of vias for each net can be no greater than one in our package routing. In addition, the candidate locations for the vias are around the bump ball. The number of vias between four adjacent bump balls is at most one.

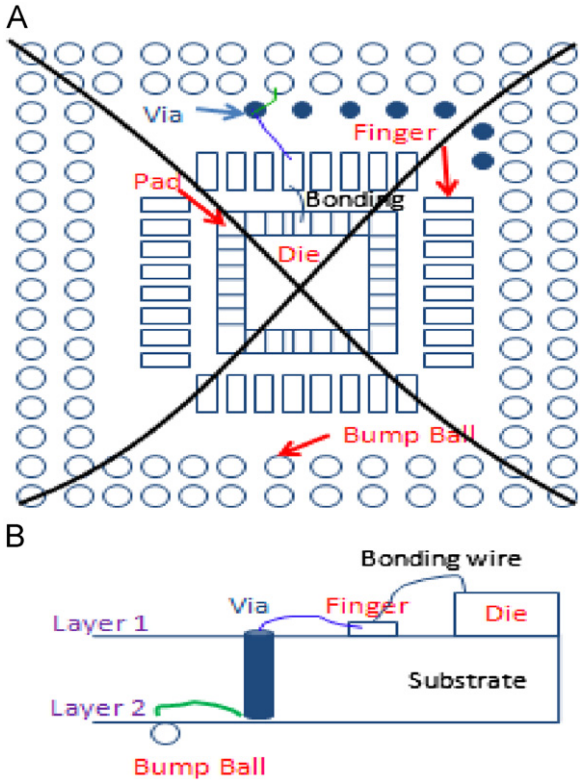

Fig. 2. The architecture of the two-layer ball grid array package used in this paper. (A) is the vertical view and (B) is the profile. We partition the package area into four parts, and solve the package problems individually.

In [10], the authors proposed a global routing method to plan the via location and the net path, and the routing result complies the monotonic characteristic. The monotonic characteristic is that the net from the finger to the bump ball intersects every horizontal grid line only once. Therefore, the detour routing would not occur and the wire length can be reduced. We adopt the idea of [10] to plan the via location and the routing path for the same purposes.

Architecture and influence of BGA package in stacking ICs

Stacking ICs in modern researches are sometimes called Three-dimensional (3-D) ICs [8] or referred as System in Package (SiP) [11]. Stacking ICs can be classified into four types: (1) package stacking; (2) chip stacking; (3) wafer stacking; (4) device stacking. The differences between each type are shown in Fig. 3. The chip in package stacking is packaged before stacking, as Fig. 3(A) illustrates. Chip stacking ICs [19] stack dies before packaging, as Fig. 3(B) shows. Wafer stacking fabrication [5,2] stacks the wafers before cutting, as Fig. 3(C) shows. A wafer stacking IC is smaller than a chip stacking IC. The size and the performance of device stacking ICs are better than wafer stacking ICs, their architecture is shown in Fig. 3(D). In this paper, we propose methods to plan the finger/pad locations for alternative stacking ICs.

Compared our rather alternative stacking IC with 2-D IC, the architectures of the bonding wires are different, as shown in Fig. 4. If the stacking effect is ignored (as shown in Fig. 4(A)), the chip performance would be worsened because the bonding wires are longer and resistances and inductances are inversely proportional to the wire length. In addition, the bonding wire yield is lower if the distance between the finger and connected pad is longer. Fig. 4(B) shows the optimal result for the finger/pad planning. To achieve this target, we need to consider the stacking factor in the finger/pad planning method.

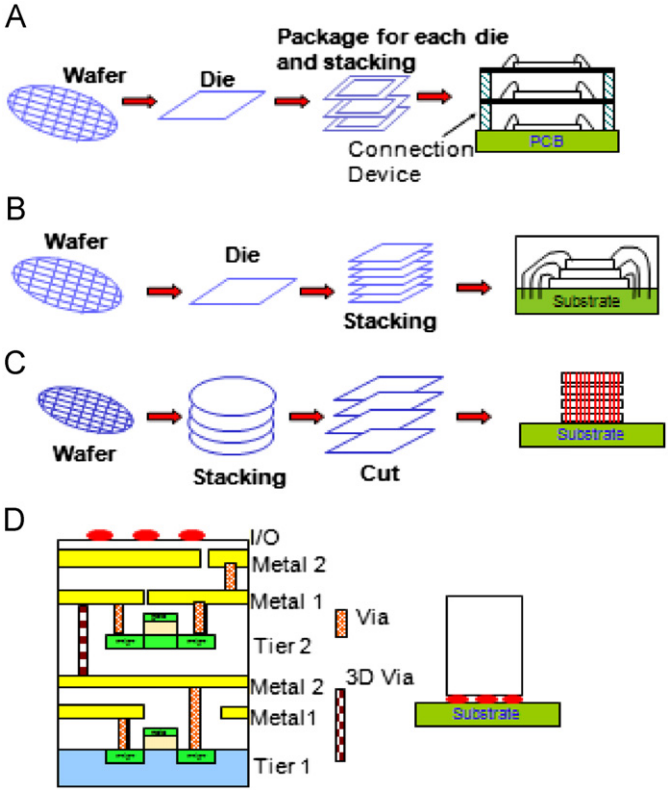

Fig. 3. The architectures of Stacking ICs: (A) package stacking; (B) chip stacking; (C) wafer stacking; (D) device stacking, which is only made in the laboratory.

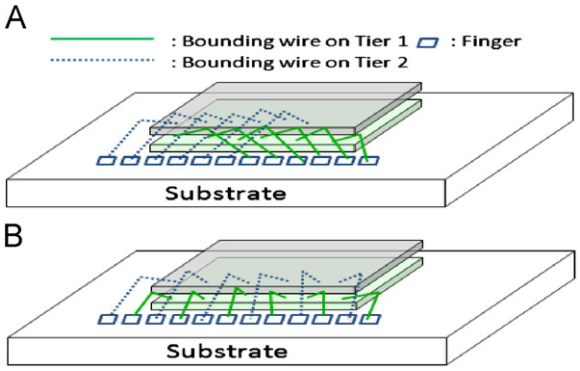

Fig. 4. The finger/pad planned results. If we use the 2-D method to plan the finger/pads in a stacking IC, the bonding wires are longer, as shown in (A). The ideal planning result is shown in (B). To achieve this target, the stacking effect needs to be computed in the finger/pad planning.

The impact of finger/pad locations on wire congestion

The vias are evenly distributed on the substrate in our package architecture. We compute the wire count between two continuous vias to denote the density. If the density is higher, it indicates that too many wires pass through a narrow range. Therefore, a violation of design rules probably occurred. To improve this problem, it is essential to develop a good method to control the density. The relationship between the density, via location and routing method is detailed in [10]. This work focuses on the relationship between the density and the finger/pad locations.

A good finger/pad assignment can help to reduce the density of the package routing. We can use an example to explain the relationship between the density and the finger/pad assignments. To display the importance of the finger/pad assignments, the via location and routing method is fixed in the example. In Fig. 5(A), we use a random method to generate the finger order, 10,1,2,3,11,6,9,4,5,8,7,0. In Fig. 5(B), a congestion-driven assignment method is used to generate a new finger order, 10,11,1,2,6,3,4,9,5,7,8,0. Compared Fig. 5(B) with (A), the maximum density can be reduced 50% when we merely change the finger order.

The impact of finger/pad locations on IR-drop violation

IR-drop is the unavoidable waste of electric charge when the circuit obtains energy from power pads. Compared wire-bond packaging with flip-chip packaging, the IR-drop problem of a wire-bond package is worse than a flip-chip package. The main reason is that the distance from the power pad to the module in a flip-chip package is shorter than in a wire-bond package. However, as we move into the nanometer regime, the resistance of the connection wire would consume the supply energy. If the power pad cannot supply enough energy, the voltage drop might exceed the lower boundary constraint. In this paper, we modify the location of each power pad to improve the resistance of the connection wire. Further, IR-drop can be improved. We use a true chip design and commercial tools to support this idea. The simulated result is shown in Fig. 6. Compared Fig. 6(B) with (A), IR-drop can be greatly improved by just changing the pad locations.

To improve IR-drop of the core, we need a good and efficient model for IR-drop analysis. This is usually done after floorplanning and placement [22,21], and the results are shown to be close to the results from SPICE simulation. In [17], authors proposed an analytical model for use before floorplanning. Since the finger/pad assignment problem is resolved before floorplanning, we adopt the model in [17] to obtain the IR-drop map. Since this model should be used before the planning of the core, it is not very

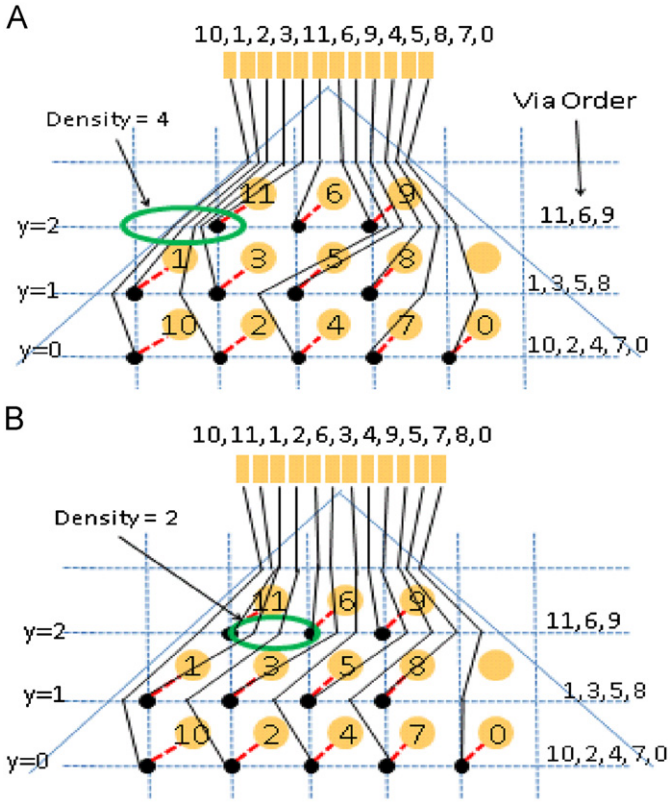

Fig. 5. The relationship between the density and the finger/pad locations. (A) uses a random method to generate a finger order and the maximum density is 4. (B) uses a congestion-driven assignment method to obtain a different finger order and the maximum density is 2.

accurate. The power grid model of [17] is shown in Fig. 7. The authors assumed that the power consumption of all the grids are the same, and proposed the following equation to calculate IR-drop of each point:

$$\frac{V_{IR}(x,y)-V_{IR}(x+\Delta x,y)}{R_{sx}\frac{\Delta x}{\Delta y}}+\frac{V_{IR}(x,y)-V_{IR}(x,y+\Delta y)}{R_{sy}\frac{\Delta y}{\Delta x}} +\frac{V_{IR}(x,y)-V_{IR}(x-\Delta x,y)}{R_{sx}\frac{\Delta x}{\Delta y}}+\frac{V_{IR}(x,y)-V_{IR}(x,y-\Delta y)}{R_{sy}\frac{\Delta y}{\Delta x}} =-J_0\cdot\Delta x\cdot\Delta y \quad (1)$$

where $V_{IR}(x,y)$ is the voltage of a point (x,y), J_0 is the current density, Δx and Δy are the incremental changes for the location of power, and R_{sx} and R_{sy} are the resistances in the x and y directions. According to Eq. (1), we can exchange power pad locations to minimize Δx and Δy to improve IR-drop. Later in experimental results, we show that this equation can be used in the real chip design for estimation.

2.5. Problem formulation

We have detailed the relationships between the wire congestion, IR-drop and finger/pad locations in 2-D and stacking ICs. Since the issues related to the wire congestion on a substrate, IR-drop of the core and bonding wires of stacking ICs are becoming more and more serious, the goal of this work is to assign nets on regular finger/pad locations to improve these issues. The problems can be formulated as follows:

Input: The locations of the fingers/pads, $F_1,F_2,\ldots,F_\alpha$ from the left to the right, the set of the net names, $N_1,N_2,\ldots,N_\beta$ and the type of each net, the locations of the bump balls, $B_{1,1,1},B_{2,1,2},\ldots,B_{\gamma,\delta,\epsilon}$, where δ,ϵ denote the coordinates of the bump ball, γ denotes the net name, β denotes the total net count, and α denotes the total finger/pad count. In addition, we must set the number of tiers, ψ, and the number of pads for each tier.

Output: The assignment of net $N_b, 1\le b\le\beta$ to finger/pad locations $F_a, 1\le a\le\alpha$.

Objective: Improve the maximum density of the package routing and the voltage drop of the core, and the length of the bonding wires.

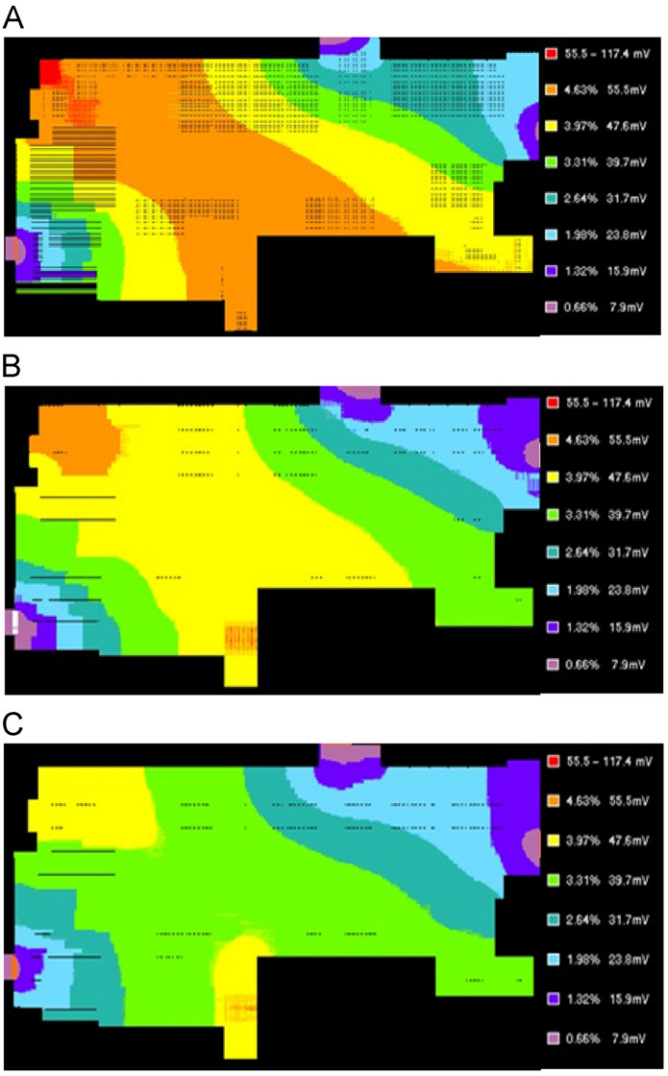

Fig. 6. The simulation results of IR-drop. Circuit in (A) and Circuit in (B) are the same, we only change the pad locations. In (A), the power pads are randomly planned. In (B), the power pads are regularly planned. This shows that pad locations critically affect IR-drop of chips. (C) shows our proposed approach which obtains better than regular pad plan.

Congestion-driven finger/pad assignment with IR-drop improvement

To improve the density, IR-drop and bonding wires, we propose a two-step methodology at the finger/pad planning level, as Fig. 1(B) illustrates. We first propose two congestion-driven finger/pad assignment methods to improve the package density; the idea is to calculate the ideal density and compute a suitable

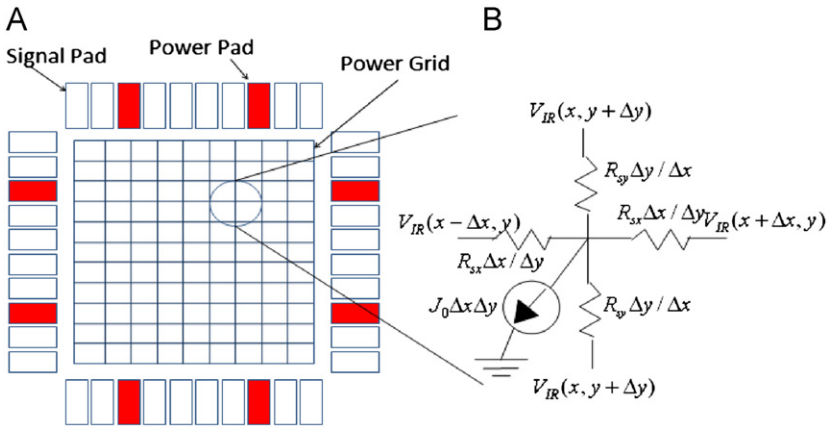

Fig. 7. The analysis model for IR-drop. (A) I/O Pad locations and the power distribution grid of the chip. (B) A node model for the grid. Using this model and EQ(1), we can compute the voltage drop in the chip.

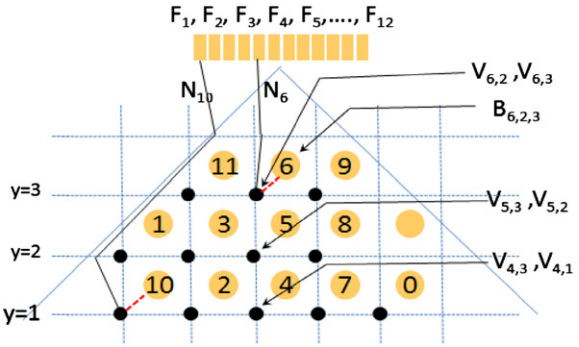

Fig. 8. The relation between notations and the package model: F_x denotes the finger location. $(V_{b,x},V_{b,y})$ denotes the via coordinate and the connected wire is N_b. $B_{b,x,y}$ denotes the bump ball coordinate and the connected wire is N_b.

finger/pad order and locations. We then present a finger/pad exchanging approach to improve IR-drop. This exchange approach will simultaneously consider the density, IR-drop and bonding wires.

Congestion-driven finger/pad assignment

The monotonic routing [10] is a popular method in the package design that guarantees a high-quality routing result. This paper adopts this routing principle to verify the effect of the assignment method. Based on the monotonic characteristic, [10] proposed an assignment rule of vias. For each finger F_a, the target bump ball is $B_{b,x,y}$, the net name is N_b, and the connected via is V_b. The coordinates of V_b are $(V_{b,x},V_{b,y})$. We randomly choose two nets N_{b1} and N_{b2}. The connected finger/pad locations are F_{a1} and F_{a2} and the connected via locations are $(V_{b1,x},V_{b1,y})$ and $(V_{b2,x},V_{b2,y})$. If $V_{b1,x} < V_{b2,x}$ and $V_{b1,y} = V_{b2,y}$, $a1$ is certainly smaller than $a2$. In other words, the via order and the displayed sequence of the finger order are the same. The map between these notations to the package module is shown in Fig. 8.

An example can help to explain the rule. In Fig. 5(A), the finger locations from the left to the right are $F_1,F_2,\ldots,F_{12}$, and the finger order is _,11,_,_,6,_,_,9,_,_,_,_. The via order in $y=2$ is 11,6,9. If the via order conforms to this rule, a legal monotonic routing certainly exists in this package. In this paper, without the loss of generality, we assume that the connected via is fixed at the bottom-left corner of the bump ball, and use the routing method from [10] to show the effectiveness of the finger/pad assignment. To improve the maximum density, a better finger/pad assignment method is needed. Here we propose two congestion-driven finger/pad assignment approaches: Intuitive-Insertion-Based Finger/Pad Assignment and Density-Interval-Based Finger/Pad Assignment.

Intuitive-Insertion-Based Finger/Pad Assignment
1. **For** each horizontal line (y=n to 1, y--)
2. m = bump ball number in this horizontal line
3. **If** (y=n)
4. for (x = 1 to m)
5. net name on bump ball, $B_{i,x,y}$ assigns into F_x
6. **else**
7. net name on F_x moves to F_{x+1}, 1 <= x <= α
8. net name on $B_{i,1,y}$ assigns into F_1
9. **For** (x = 2 to m-1)
10 net name on $B_{i,x,y}$ assigns into F_{b-1},
11 F_b denotes the location of (x-1)th bump ball on the (y+1) line
12. **End For**
13. net name on $B_{i,m,y}$ assigns into the last finger location
14. **End If**
15. **End For**

Fig. 9. The pseudocode of the Intuitive-Insertion-Based Finger/Pad Assignment method.

Intuitive-insertion-based finger/pad assignment (IFA)

This method depends on the inserted characteristic to avoid the illegal monotonic rule. The pseudo code is shown in Fig. 9. For each horizontal line (line 1), we must calculate the number of bump balls (line 2). For the first horizontal line ($y=n$, n is the highest horizontal line), the net name of each bump ball $B_{i,x,y}$ is directly assigned on F_x (lines 3–5). For other horizontal lines ($y=n-1$ to 1), the net name of the first bump ball $B_{i,1,y}$ assigns into F_1 and the net name of bump balls ($x=2$ to $m-1$) is assigned at F_{b-1}, where F_b denotes the $(x-1)_{th}$ bump ball location in the $(y-1)_{th}$ horizontal line (lines 7–11). The net name of the last bump ball is directly inserted into the last finger location (line 13). The time complexity for IFA is $O(n^2)$.

We use an example to explain the IFA flow. In this example, the locations of the bump balls and nets are the same as in Fig. 5. An illustration of the IFA is shown in Fig. 10(A) and the routing

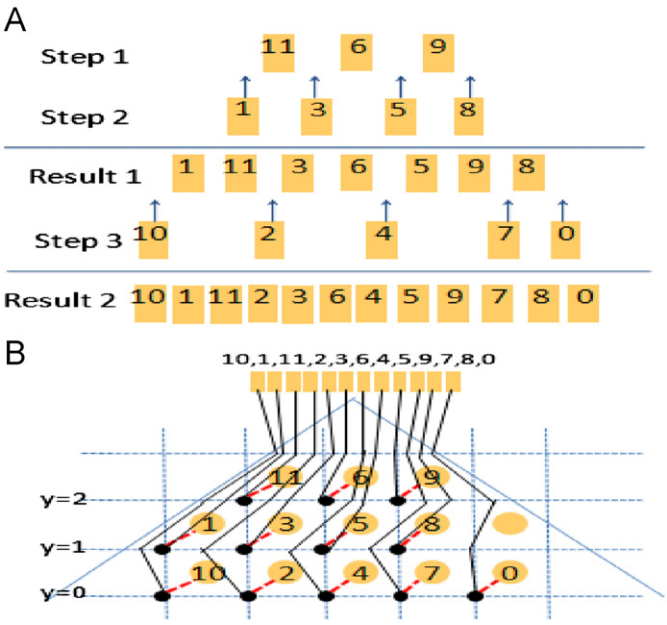

Fig. 10. The IFA result is shown in (A), the routing result is shown in (B). The maximum density in the routing result is 2. Compared this result with Fig. 5(A), the maximum density has decreased by 50%.

result is shown in Fig. 10(B). In Fig. 10(A), because nets 11, 6, and 9 are set at the highest horizontal line($y=3$), step 1 assigns these three nets into finger locations F_1,F_2, and F_3. Step 2 inserts nets 1, 3, 5, and 8($y=2$) into suitable finger/pad locations. Net **1** is set at $B_{i,\mathbf{1},y}$; we assign net 1 into F_1 and the other nets on the finger move to the next finger location. For net 3, the bump ball location is $B_{3,2,1}$. The net name on $B_{i,2,1+1}$ is "Net 6". Therefore, net 3 is inserted before net 6. Net 5 uses the same method to obtain a suitable finger/pad location. Net 8 is inserted into the last location because it is the last net on this line. Step 3 repeats step 2 to insert remaining nets. The final finger order is 10,1,11,2,3,6,4,5,9,7,8,0. The routing result is shown in Fig. 10(B) and the density is 2.

Density-interval-based finger/pad assignment (DFA)

If IFA is applied to a two-level BGA package, the routing result is very good. If IFA is applied to a BGA package with three or more levels, the result is imperfect because the insertion method of IFA only considers two horizontal lines. We propose another method, Density-interval-based Finger/pad Assignment (DFA), to solve this problem. This method would consider all of the bump ball locations when the nets seek the better finger/pad locations. The pseudocode is shown in Fig. 11.

We first determine a processing priority based on the coordinates of all the horizontal lines(line 1). For each horizontal line, we calculate the number of bump balls (line 2). Then, the density interval (DI) is computed (line 3), where "Total Non-allocated Net" denotes the number of nets not connected to the via, "Total Via Number" denotes the number of vias on the horizontal line, and "Used Via Number" denotes the via used on the horizontal line, which means the vias already used for assigned pads. "(Total Via Number+n)" denotes the segment in this horizontal line. If we do not care the congestion at the cut-line, n can be set at 1. Because our package is cut into four triangles and each triangle is assigned independently, the congestion along the diagonal cut-lines is ignored. Actually, two neighboring triangles contributes to the congestion along the cut-line. To solve this problem, the value of n must be more than 2. Therefore, the most right and most left segments can be treated one segment.

Density-Interval-Based Finger/Pad Assignment

1. **For** each horizontal line (y=n , y--)
2. m = bump ball number in this horizontal line
3. compute the density interval :

$$DI = \frac{\text{Total Non-allocated Net} - \text{Used Via Number}}{\text{Total Via Number} + n}, n \geq 1$$

4. **For** (x=1 to m)
5. compute the empty number : EN = $\lfloor x * DI \rfloor$
6. net name on $B_{i,x,y}$ assigns into the (EN+1)th unassigned finger/pad location
7. **End For**
8. **End For**

Fig. 11. The pseudocode of the Density-Interval-Base Finger/Pad Assignment (DFA) method. This method can be applied to a multi-layer BGA package and the time complexity is $O(n)$.

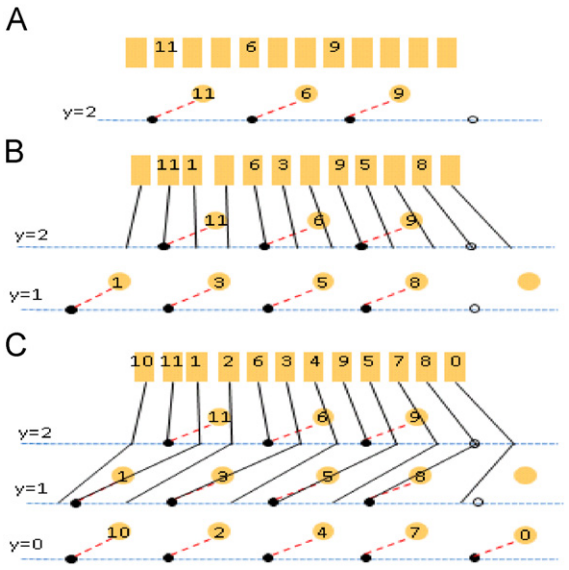

Fig. 12. The illustration of the Density-Interval-Based Finger/Pad Assignment method. For each horizontal line, the net names are averagely assigned into the finger/pad locations, the routing path of all nets can be averagely planned into the whole substrate.

After DI is obtained, we should determine the finger/pad locations of each bump ball on this horizontal line. For each bump ball ($B_{i,x,y}$, $1 \leq x \leq m$), we calculate the empty number (EN) and insert the net name into the $(EN+1)_{th}$ location (lines 4–7), where EN denotes the empty slot in the finger location. The time complexity for DFA is $O(n)$.

We use the same example to show the effectiveness of DFA. An illustration of DFA is shown in Fig. 12. In this case, we ignore the congestion at the cut-line. Because nets 11, 6, and 9 are set at the highest horizontal line ($y=3$), the first step is to decide on the finger locations of these three nets. According to the input information, the bump balls of these three nets are $B_{11,1,3}$, $B_{6,2,3}$ and $B_{9,3,3}$. The Total Non-allocated Net is 12, Total Via Number is 4 and Used Via Number is 3. $DI=(12-3)/(4+1)=1.8$. For net 11, $EN=\lfloor 1*1.8 \rfloor=1$. It is because EN=1, we try to assign this net to the next location due to density concern. Therefore, net 11 is inserted into F_2 For net 6, $EN=\lfloor 2*1.8 \rfloor=3$. Because F_2 is occupied, F_1,F_3, and F_4 are unassigned spaces, and net 6 is assigned to the $(3+1)_{th}$ unassigned space, F_5. Using the same method, all of the nets can be inserted into suitable finger/pad locations. The final order of the nets is 10,11,1,2,6,3,4,9,5,7,8,0, as shown in Fig. 12(C), and the routing result is shown in Fig. 5(B).

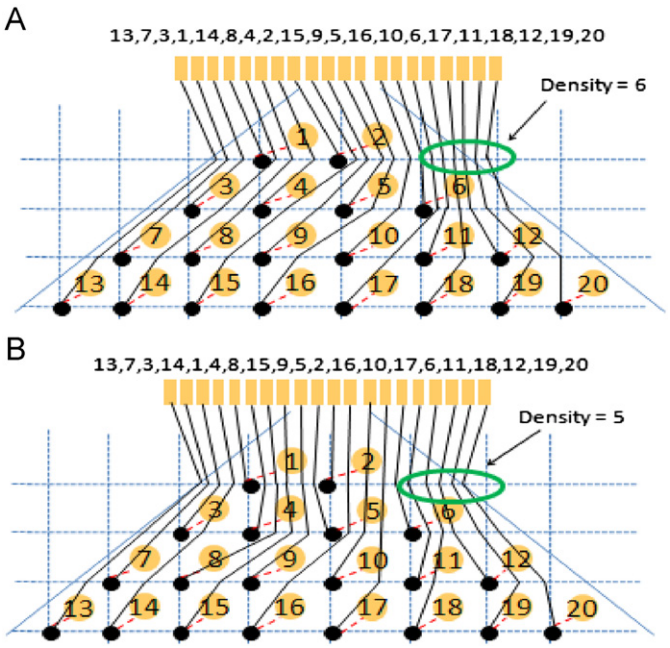

Fig. 13. (A) uses IFA to generate a finger order and the maximum density is 6 in one grid (between assigned and unassigned vias). (B) use DFA to obtain a better finger order and the maximum density is 5.

DFA can obtain a better finger order when the number of finger and the bump-level is large. We use another example to show that DFA is better than IFA. The nets and bump ball locations are shown in Fig. 13. If IFA is used to plan these nets, the finger order is 13,7,3,1,14,8,4,2,15,9,5,16,10,6,17,11,18,12,19,20, and the density of package routing is 6, as shown in Fig. 13(A). If we adopt DFA to plan, the finger order of nets is 13,7,3,14,1,4,8,15,9,5,2,16,10,17,6,11,18, 12,19,20, and the density is 5, as shown in Fig. 13(B).

Finger/pad exchange of 2-D and stacking ICs for IR-drop and bonding wire improvement

After obtaining an initial net order for finger/pad locations, this order can be changed to improve IR-drop of the core. If we directly use Eq. (1) to calculate IR-drop, the analysis time for the chip is very long. The main reason is that there is a large number of analysis points and power pads. To improve this problem, an efficient method for quickly analyzing IR-drop is needed. In this paper, we compute the variation of Δx and Δy to be the IR-drop improvement when the location of the power pad is exchanged. This method would cause high-density routing in a package design because the density problem is ignored in this computation. Here we propose a method to improve IR-drop while simultaneously suppressing the density.

Section 3.1 has introduced the monotonic order. If our exchange method ignores this principle, the monotonic routing result is non-existent in the package. To maintain this property, we add a range constraint in our exchange method. The key idea for the range constraint is to map the monotonic order of vias [10] above the finger locations. We choose three bump balls $B_{b1,x1,y1}$, $B_{b2,x2,y2}$ and $B_{b3,x3,y3}$, and the connected fingers are F_{a1}, F_{a2} and F_{a3}. If $x1<x2<x3$ and $y1=y2=y3$, we have this order: $F_{a1}<F_{a2}<F_{a3}$. we formulate the constraint. In Fig. 5(B), net 6 is assigned at F_5, and the exchange range of net 6 is between F_3 and F_7. If the exchange range is without the limit, we must pay a higher cost to find a suitable connected via to build the monotonic routing.

When the finger/pads are exchanged, the package density needs to be controlled at the same time. Here we propose a control method. After the congestion-driven assignment step, the initial order of the nets on the finger/pad locations is determined. The bump ball locations should be recorded when they are planned at the highest horizontal line. This recording is needed because the monotonic rule is used in our package routing. The monotonic characteristic is that the net from the finger to the bump ball intersects every horizontal grid line only once. The detour routing would not occur. Therefore, the density of the high horizontal line is higher than the density of the low horizontal line. Based on this characteristic, we have an efficient method to estimate the package congestion. We only oversee the density in the highest horizontal line. If the recorded number is x, nets could be divided into $x+1$ sections, S_c, $0\le c\le x+1$. For each section, we should record the interval number I_c^{ini},$1\le c\le x+1$. When the nets are exchanged, the interval number would be changed. These numbers are called I_c^{new},$1\le c\le x+1$. Therefore, the increased density (ID) can be computed as follows:

$$ID=\max(I_c^{new}-I_c^{ini}),\quad 1\le c\le x+1 \tag{2}$$

The package density is inversely proportional to the value of ID.

The impact of bonding wires should be considered in the finger/pad exchange method when the architecture is stacking IC (tier number is not less than one; $\psi\ge 2$). We propose a method to improve bonding wires; the idea is to averagely plan pads of different tiers. According to the number of tiers, ψ, we make an unique parameter for each tier, UP_d,$1\le d\le\psi$. This unique parameter has ψ bits. One bit denotes one tier. We can use an example to explain the method for making this parameter. If the tier number is 3, the parameters from Tier 1 to Tier 3 are "001", "010" and "100". Every finger has one bonding wire to connect to the pad. The pad is set at Tier d,$1\le d\le\psi$, and Tier d has one unique parameter, UP_d. Therefore, we set the parameter of the fingers that connect to Tier d as UP_d. The set of finger locations, $F_1,\ldots,F_\alpha$, are divided into $\lceil\alpha/\psi\rceil$ groups, $G_1,G_2,\ldots,G_\eta$,$1\le\eta\le\lceil\alpha/\psi\rceil$. Every group most has ψ members and least has 1 member. For each group, all members should utilize the unique parameter to perform the union operation. Finally, we have to sum up the count of the zero bit, ω, from G_1 to G_η. If the value of ω is more smaller, it indicates that the pads of different tiers are more equidistant planed.

We use an example to explain this operation. In Fig. 4, the number of tiers is 2, UP_1 is "01" and UP_2 is "10". The total finger number is 12. Therefore, these finger can be divided into $\lceil 12/2\rceil=6$ groups. Every group has two members. F_1 and F_2 are assigned into the same group. Other group member are showed as follow: (F_3,F_4), (F_5,F_6), (F_7,F_8), (F_9,F_{10}), (F_{11},F_{12}). We first compute the number of 0 s for G_1. In Fig. 4(A), F_1 and F_2 both connect to the Tier 2. Therefore, the UP value of F_1 and F_2 are both "10". The union result of G_1 is $10\cup 10=10$. The numbers of 0 s of G_1 is 1. The numbers of 0 s from G_1 to G_6 are 1,1,1,1,1,1 and the total number of 0 s, ω, is 6. We use the same method to compute ω of Fig. 4(B). The result is 0. Compared Fig. 4(A) and (B), the bonding wire connection of (B) is better than (A). Therefore, we hope ω value is smaller in all chip designs.

Finally, we integrate the improvement methods for IR-drop, package density, and bonding wires into one finger/pad exchange method. The cost function in our exchange method is shown as follows:

$$Cost=\lambda\cdot\Delta_{IR}+\rho\cdot ID+\varphi\cdot\omega \tag{3}$$

where Δ_{IR} denotes the total variation of Δx and Δy and, λ, ρ and φ denote the weights in our cost function. Based to the cost function, switching constraint and the SA (Simulated Annealing) [7] algorithm, we propose a power-supply noise-driven exchange

```
Finger/Pad Exchanging Method
Objective : Improve IR-drop, the length of bounding wires
            and suppress the increase of package density
1. Begin
2.   Initial Cost ; Temperature; Final_Temperature;
3.  while Temperature > Final_Temperature
4.      If Tier number, ψ > 1
5.          Random choose one pad, F_a ;
6.      else
7.          Random choose one power pad, F_a ;
8.      Switch (F_a , F_a+1) or Switch (F_a , F_a-1)
9.      Using EQ(3) to compute the new cost
10.      If ( New Cost < Old Cost)
11.          Accept new net order
12.      else if Random (0,1) > exp(-ΔC / Temperature)
13.          Accept new net order
14.     end if
15.     Cooling (Temperature)
16.  End while
17. End
```

Fig. 14. The pseudo code of our finger/pad exchange method for 2-D and stacking IC architectures. This method can simultaneously improve IR-drop and bonding wires, and suppress the package density.

algorithm, as illustrated in Fig. 14. After the congestion-driven finger/pad assignment, the initial net order is obtained. Therefore, we can use Eq. (3) to compute the initial cost. In addition, the initial values for two annealing temperature parameters are set (line 2). We randomly choose one net to switch and use Eq. (3) to compute the switching cost (lines 4–8). If the new cost is smaller than the old cost, it means that a better net order is obtained and we would adopt this result to be our order (lines 10–11). If not, we randomly decide that the original net order must be replaced by the new net order (lines 12–14). Finally, the temperature is cooled (line 15).

Experimental results and discussions

This paper implements IFA, DFA, and the finger/pad exchanging approach using C++ language on an AMD 3200 computer with 1G memory. Five simplified industrial circuits are used to test the performance of proposed methodology. The runtimes for all cases are within seconds. In test circuits, the via diameter is set at 0.1 μm and the diameter of BGA bump ball is set at 0.2 μm. The number of the horizontal (vertical) line in the bottom (left) and top (right) part in of package architecture is set at 4; others are shown in Table 1. The second column denotes the total count of finger/pads. The third column denotes the minimal space between two continual bump balls. The width and height of the finger are shown in the third and fourth column. The last column denotes the minimal space between two continual fingers.

Table 2 compares our methods with a random method. The wirelengths are calculated from the direct flylines between pads/vias. The random method denotes that the assignment order conforms the monotonic rule and other factors are ignored. In the last row, we compare the average ratio of the maximum density. We set the average density of the random method is 100%. The average densities for IFA and DFA are 63% and 36%. Compared the random method with DFA, the average density improves 64%. In addition, the total wire length of the package routing could be improved. The improved reason is that the routing path is near to the straight line. Fig. 15 shows the routing results of Circuit 2. The results conform the monotonic characteristic. In Fig. 15(A), the routing path of most wires is the broken line. In the DFA result, the routing path of most wire is near to the straight line. Therefore, the result of DFA is better than the random method.

Table 1
The experimental data of test circuits.

Input case	Finger/pad counts	Bump ball space (μm)	Finger width (μm)	Finger height (μm)	Finger space (μm)
Circuit 1	96	2	0.025	0.4	0.025
Circuit 2	160	1.4	0.006	0.3	0.1
Circuit 3	208	1.2	0.006	0.2	0.007
Circuit 4	352	1.2	0.1	0.2	0.12
Circuit 5	448	1.2	0.1	0.2	0.12

Table 2
This shows the maximum density and the total wire length in our test circuits. The DFA method shows the best result. Compared DFA with the random method, the maximum density decreases 64%.

Input case	Max density			Wire length (μm)		
	Random	IFA	DFA	Random	IFA	DFA
Circuit 1	11	8	6	42,844	38,376	37,230
Circuit 2	12	8	5	48,197	45,403	42,583
Circuit 3	13	8	4	67,837	58,934	55,311
Circuit 4	15	8	4	74,212	64,576	60,137
Circuit 5	13	8	4	79,470	68,033	62,544
Average	1	0.63	0.36	1	0.88	0.82

After DFA, an initial net order for finger/pad locations can be obtained. We then use the proposed finger/pad exchange method to improve IR-drop and bonding wires. Table 3 shows the experimental result of the finger/pad exchange. ψ denotes the number of tiers. If the value of ψ is 1, the test circuits are 2-D IC. If ψ more than 1, the test circuits are Stacking IC. We use [17] method to calculate the maximum value of IR-drop. The value of IR-drop before finger/pad exchanging is called IR_{before}, and the value of IR-drop after finger/pad exchanging is called IR_{after}. The computation of improved IR-drop is $(IR_{after}/IR_{before}) \times 100\%$. In 2-D IC, the average improvement of IR-drop is 10.61%. The last column denotes the improved ratio of bonding wires. The computed method is to calculate the difference for "0" bit count between the DFA step and the finger/pad exchange step. Based on this result, our finger/pad exchange method can be used in 2-D and Stacking IC. In addition, IR-drop and bonding wires can be improved at the same time.

Finally, we use a real chip design to support our method, as shown in Fig. 6. This design has 138 finger/pads and the gate count is 2.3 million, and we use DFA and our finger/pad exchange method to obtain the pad order. The simulation result is shown in Fig. 6(C). In Fig. 6(A) and (B), maximum IR-drop are 117.4 mV and 77.3 mV. In Fig. 6(C), maximum IR-drop has only 55.2 mV, which shows that IR-drop in the chip design can be improved by our method.

Note that our intention in this work is to try to bring up the signal integrity awareness issues during chip-package codesign for different configurations, thus the chip floorplanning and placement are ignored. Instead we use a model [17] to consider chip planning, therefore it will inevitably degrade a bit on the solution quality in physical design stages. We can use more accurate model for chip performance, however, the tradeoff for efficiency exists.

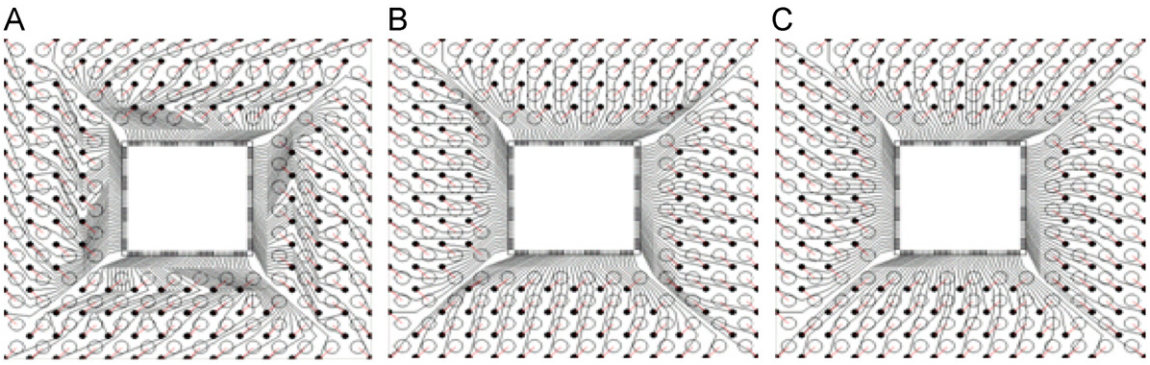

Fig. 15. The routing results of Circuit 2. We use the same routing algorithm to realize the package routing. (A) The random assignment result. (B) The IFA result. (C) The DFA result. The maximum density and the wire length of DFA is better than others.

Table 3
This table shows that the improved ratio of IR-drop and bonding wires. ψ denotes the number of tiers. If ψ is 1, it indicated that test circuits are 2-D IC. If ψ is more than 1, test circuits are Stacking IC. The experimental result proves that the finger/pad exchange method can be successfully used in 2-D IC and sacking IC and the performance is good.

Input case	2-D IC($\psi=1$)			Stacking IC($\psi=4$)			
	Max density		Improved	Max density		Improved	Improved
	After DFA	After exchanging	IR-drop (%)	After DFA	After exchanging	IR-drop (%)	Bonding wire (%)
Circuit 1	6	8	27.36	6	7	7.39	10.81
Circuit 2	5	8	9.43	5	7	5.75	12.54
Circuit 3	4	7	5.89	4	7	2.9	18.22
Circuit 4	4	7	6.92	4	6	4.7	17.27
Circuit 5	4	7	3.45	4	7	2.2	19.46
Average improvement			10.61			4.58	15.66

5. Conclusion

In the modern chip design, finger/pad counts continue to increase due to the more function of chips. This adds up more complexity in the chip design. The finger/pad location not only affects the package design, but also impacts IR-drop of the core. In this work we propose techniques to allocate finger/pads for package routability and core signal integrity concerns, which are the primary metrics in system design. Experimental results show the effectiveness of our approaches.

In modern chip design, floorplan technology is frequently used to increase the performance and functions. In [13], the author proposed a planning method to plan pads and modules in stacking ICs. Therefore, a concurrent process for floorplan and package problems will be explored to further improve the turn-around time for the chip design and increase the yield of stacking ICs.

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