Current Applied Physics 13 (2013) 1459–1462

Contents lists available at SciVerse ScienceDirect

Current Applied Physics

journal homepage: www.elsevier.com/locate/cap

Room-temperature flexible thin film transistor with high mobility

Hsiao-Hsuan Hsu [a], Chun-Yen Chang [a], Chun-Hu Cheng [b,*]

[a] Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, ROC
[b] Department of Mechatronic Technology, National Taiwan Normal University, Taipei 106, Taiwan, ROC

ARTICLE INFO

Article history:
Received 5 February 2013
Received in revised form
10 April 2013
Accepted 26 April 2013
Available online 6 May 2013

Keywords:
InGaZnO (IGZO)
Thin film transistor (TFT)
Y_2O_3
TiO_2

ABSTRACT

We report a room-temperature and high-mobility InGaZnO thin-film transistor on flexible substrate. To gain both high gate capacitance and low leakage current, we adopt stacked dielectric of $Y_2O_3/TiO_2/Y_2O_3$. This flexible IGZO TFT shows a low threshold voltage of 0.45 V, a small sub-threshold swing of 0.16 V/decade and very high field-effect mobility of 40 cm^2/V. Such good performance is mainly contributed by improved gate stack structure and thickness modulation of IGZO channel that reduce the interface trap density without apparent mobility degradation.

1. Introduction

Zinc oxide-based thin film transistors (TFTs) have been studied extensively due to promising application on low-cost large-area display. Compared to poly-Si TFTs with high thermal budget for channel activation, the amorphous InGaZnO (α-IGZO) [1–9] channel layer has the opportunity to achieve a high performance TFT at low temperature by offering better film uniformity and less transistor characteristics variation. Furthermore, α-IGZO TFTs with high mobility has the potential for the fabrication of high-resolution and low-temperature flexible displays. However, recently reported IGZO TFTs on flexible substrate [10–12] showed large operating voltage, high sub-threshold swing and low device mobility. Although the operating voltage can be lowered by means of integrating high-κ gate dielectrics, common metal oxides that deposit at low temperature tend to form defect-rich dielectric and then results in low κ value and large gate leakage. Besides, the device mobility and sub-threshold leakage are most critical for the low-temperature and high-resolution flexible TFT.

To address these key issues at low-temperature flexible device, we demonstrate a high performance IGZO TFT utilizing tri-layer gate dielectric of $Y_2O_3/TiO_2/Y_2O_3$ and IGZO thickness modulation on flexible substrate. The novel flexible TFT fabricated at room temperature (RT) shows a small sub-threshold swing of 0.16 V/decade, a low threshold voltage of 0.45 V, and a high field-effect mobility of 40 cm^2/V under a drive voltage below 2 V.

2. Experimental procedure

The bottom gate TFT was fabricated on the 300-nm-thick insulating SiO_2 grown on a flexible PC (polycarbonate) substrate. A 35-nm-thick TaN gate electrode was formed by sputtering. Subsequently, the optimized Y_2O_3 (105 nm) and $Y_2O_3/TiO_2/Y_2O_3$ (22 nm/60 nm/22 nm) were deposited using electron beam evaporation at room temperature. Such a physical vapor deposition process is preferred for formation of the gate dielectric of TFTs because of its low thermal budget, especially when plastic substrates are used [13]. Then the 25- and 50-nm-thick IGZO active layers were deposited using radio frequency (RF) sputtering from an IGZO target with a gas mixture of oxygen and argon. Finally, 300-nm-thick Al was thermally evaporated and patterned to form source and drain contact electrodes, where the channel size was 521 μm × 32 μm.

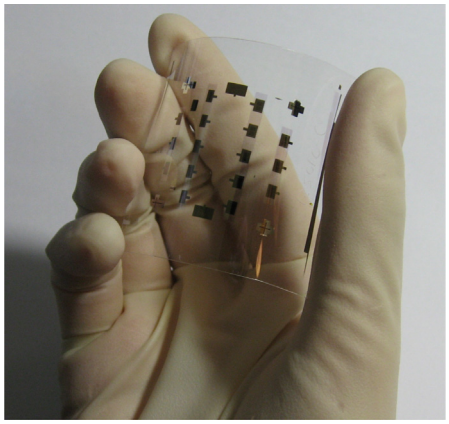
The gate stacks were characterized by atomic force microscopy (AFM), grazing incidence X-ray diffraction (GIXRD) and transmission electron microscopy (TEM). The TFT devices were characterized by current–voltage (I–V) and capacitance–voltage (C–V) measurements using an HP4156C semiconductor parameter analyzer and an HP4284A precision LCR meter, respectively.

3. Results and discussion

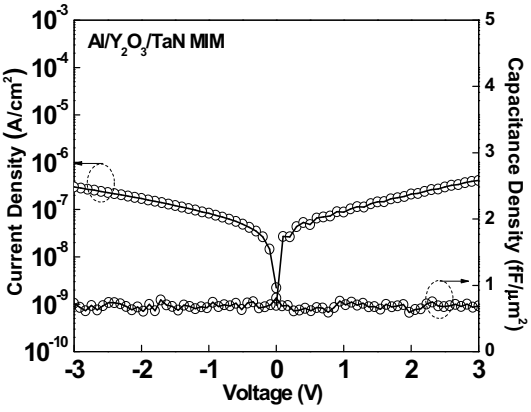
To fabricate high performance and low temperature flexible TFT, we use transparent plastic PC as the substrate. As seen in Fig. 1(a),

* Corresponding author. Tel.: +886 2 7734 3514; fax: +886 2 2358 3074.
E-mail address: chcheng@ntnu.edu.tw (C.-H. Cheng).

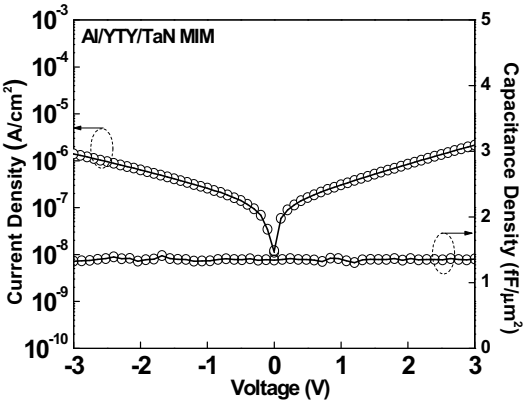
1567-1739/$ – see front matter © 2013 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.cap.2013.04.026



(a)



(b)

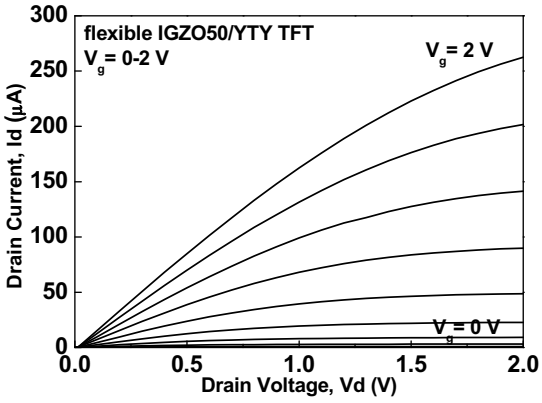


(c)

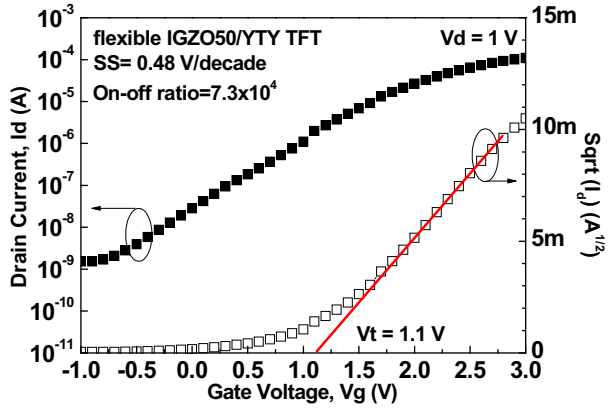
Fig. 1. (a) Photograph of flexible and transparent IGZO TFTs. *C*–*V* and *I*–*V* characteristics of (b) Al/Y_2O_3/TaN and (c) Al/YTY/TaN MIM capacitors on flexible PC substrates.

the photograph of flexible and transparent IGZO TFT which has been successfully fabricated on PC substrate. The *C*–*V* and *I*–*V* characteristics of metal–insulator–metal (MIM) capacitors using single-layer Y_2O_3 and stacked Y_2O_3/TiO_2/Y_2O_3 (YTY) dielectrics on flexible PC substrates are shown in Figs. 1(b) and(c), respectively. The gate leakage current of 4.1 $\times$ 10^{-7} A/cm^2 at 3 V is measured in Al/Y_2O_3/TaN MIM capacitor with a capacitance density of 0.8 fF/μm^2 at 100 kHz. The extracted κ-value of 9.5 is reasonable due to RT film deposition without an additional thermal budget. However, to reduce drive and turn-on voltage effectively, it is necessary to increase capacitance density utilizing higher-κ Y_2O_3/TiO_2/Y_2O_3 dielectric. Unfortunately, the TiO_2 would bring unwanted gate leakage current due to narrow band gap of 3.05 eV and small conduction band offset (ΔE_C is only 0.05 eV) [14]. Thus, the buffered Y_2O_3 layer with large band gap of 6 eV [14] plays an important role for suppressing leakage current. In Fig. 1(c), the tri-layer YTY MIM capacitor with a similar film thickness shows a much higher capacitance density of 1.4 fF/μm^2 that is beneficial to obtain higher drive current at a lower operating voltage, compared to single-layer Y_2O_3 one. The increased MIM capacitance density can be ascribed to the introduction of TiO_2 dielectric with very high-κ value of 60–110 [15,16]. From the measured *I*–*V* characteristic in tri-layer MIM capacitor, the higher gate leakage of 2.2 $\times$ 10^{-6} A/cm^2 at 3 V is further supported by 43% increase on capacitance density. Furthermore, these MIM capacitor results confirm that the tri-layer gate dielectric has a more favorable tradeoff between capacitance density and gate leakage current under a RT TFT process.

From the AFM analyses, the surface roughness (Rms = 1 nm) for tri-layer YTY dielectric is only slightly higher than that single-layer Y_2O_3 one (Rms = 0.8 nm), which explains the feasibility of TiO-based stacked dielectric on flexible substrate. Although high-κ TiO_2 can gain larger capacitance density for high drive current, titainum-terminated surface may contribute to high interface traps and large leakage current at RT flexible process. Thus, the large band gap Y_2O_3 as top and down buffer layer can be used to lower gate leakage current due to large potential barrier formed at top IGZO/Y_2O_3 and bottom Y_2O_3/TaN interfaces. To perform a deep investigation on MOSFET



(a)



(b)

Fig. 2. (a) I_d–V_d and (b) I_d–V_g characteristics of flexible YTY TFT with 50-nm-thick IGZO channel layer.

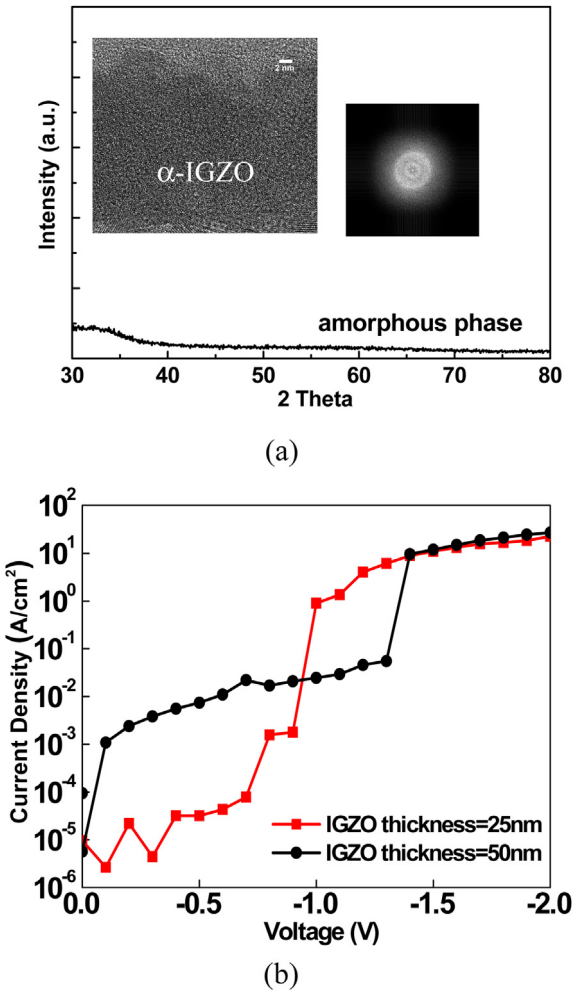


Fig. 3. (a) XRD spectrum of IGZO channel layer and (b) I–V characteristics of Al/IGZO/TaN MIM capacitors with different IGZO thicknesses. The high-resolution TEM and FFT images of IGZO channel were inserted in Fig. 4(a).

characterizes, we first fabricated IGZO TFT using YTY gate dielectric and 50-nm-thick IGZO channel layer (IGZO50) on flexible PC. The output I_d–V_d and transfer I_d–V_g characteristics were shown in Fig. 2(a) and (b), respectively. In addition to low operating voltage of 3 V, large sub-threshold swing (SS) of 0.48 V/decade, I_{on}/I_{off} ratio of 7.3×10^4, threshold voltage (V_t) of 1.1 V and high field-effect mobility (μ_{FE}) of 42.8 cm^2/V are also reached. The channel carrier density of 1.9×10^{16} cm^{-3} can be extracted by the equation: $N_{ch} = V_t \times C_{HK}/(q \times t_{ch})$, where q is the electric charge (1.6×10^{-19} C), t_{ch} is the thickness of channel layer, V_t is the threshold voltage of the device, and C_{HK} is the capacitance density of the high-κ dielectric. The change of channel resistance is dominated by the vacancies in IGZO channel with the dependence of oxygen concentration, as seen in the equation: $V^{2+}_{InGaZn-O_x} + 2e^- + InGaZn{-}O_x \rightarrow InGaZn{-}O_x^*$. Here, the $V^{2+}_{InGaZn-O_x}$ is the oxygen vacancy in IGZO, which is responsible for channel carrier concentration and device mobility.

Fig. 3(a) shows the XRD spectrum of IGZO channel layer. The inserted TEM image is cross-sectional view of IGZO layer. The sputtered IGZO film reveals an amorphous state examined by Fast Fourier Transform (FFT) technique. Also, the leakage currents of IGZO channel with different thicknesses are also carried out via MIM capacitor in Fig. 3(b). For thinner 25-nm-thick IGZO, the leakage current of 3.2×10^{-5} A/cm^2 at −0.5 V is much smaller than that of 50-nm-thick IGZO by two orders of magnitude. In general, a low channel leakage (high channel resistivity) at low field was used to achieve a low off-state current and high on–off ratio. It follows that the IGZO thickness modulation to suppress sub-threshold leakage is very important, especially for enhanced mode TFT with fully RT process. According to this, we also fabricated fully-RT IGZO TFT with thin 25-nm-thick IGZO (IGZO25) on PC substrate. The I_d–V_d and I_d–V_g characteristics of IGZO25/YTY flexible TFT are shown in Fig. 4(a) and (b), respectively. The low sub-threshold swing of 0.16 V/decade, small V_t of 0.45 V, I_{on}/I_{off} ratio of 4.5×10^5, and high field-effect mobility of 40 cm^2/V for IGZO25/YTY TFT is much better than reported flexible IGZO TFT [10–12]. Such small gate swing is further supported by low drive voltage (V_g–V_t) below 2 V, which is important for flexible display applications with a low operation power.

As we know that the sub-threshold swing is relevant to the interface trap density (D_{it}) calculated based on the equation: $SS = kT/q \times \ln 10 \times (1 + (C_b + C_{it})/C_{HK})$, where C_b is the depletion capacitance density of IGZO, and C_{it} ($=qD_{it}$) is the capacitance density from charged interface traps. By neglecting C_b, the D_{it} for IGZO25/YTY and IGZO50/YTY TFTs are 1.5×10^{12} and 6.2×10^{12} cm^{-2} eV^{-1}, respectively. In addition, the carrier density of 1.6×10^{16} cm^{-3} is also obtained from thin IGZO25 channel layer. Compared to IGZO50/YTY TFT offering 4× higher interface state and 1.2× higher carrier concentration, the IGZO25/YTY one exhibits better transistor characteristics including much lower SS and V_t after optimizing channel thickness. Such good performance at RT without apparent mobility degradation is not also ascribed to stacked YTY dielectric for enhancing capacitance density, but also supported by channel thickness modulation scheme for controlling densities of channel carrier and interface traps that is dominated by oxygen vacancies in IGZO.

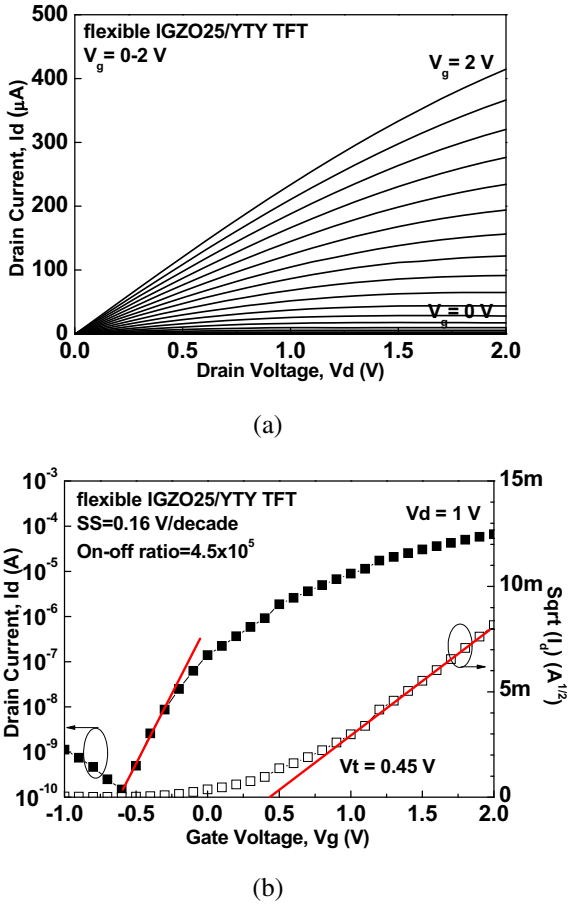


Fig. 4. (a) I_d–V_d and (b) I_d–V_g characteristics of flexible YTY TFT with 25-nm-thick IGZO channel layer.

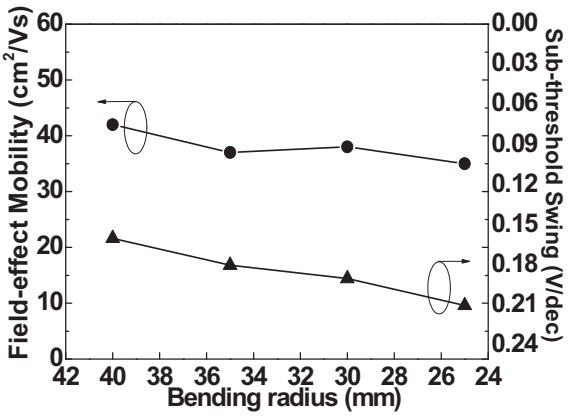


Fig. 5. Field-effect mobility and sub-threshold swing as a function of bending radius for IGZO/YTY TFT.

To evaluate bending flexibility of TFT device on flexible PC, we perform bending test with the radius from 40 mm to 25 mm, as shown in Fig. 5. The *SS* and device mobility under bending only shows slight degradation that demonstrates the feasibility of IGZO/YTY TFT for flexible display application.

4. Conclusions

Our study offers a simple and effective solution to fabricate low-power and high-mobility TFT at RT on flexible substrate. The flexible IGZO TFT using improved gate stack and optimized channel thickness can reach good transistor characteristics including a low V_t of 0.45 V, a small *SS* of 0.16 V/decade and a high μ_{FE} of 40 cm^2/V at a very low drive voltage below 2 V.

References

[1] N.C. Su, S.J. Wang, Albert Chin, IEEE Electron Device Lett. 30 (2009) 1317.
[2] N.C. Su, S.J. Wang, C.C. Huang, Y.H. Chen, H.Y. Huang, C.K. Chiang, Albert Chin, IEEE Electron Device Lett. 31 (2010) 680.
[3] T. Aoi, N. Oka, Y. Sato, R. Hayashi, H. Kumomi, Y. Shigesato, Thin Solid Films 518 (2010) 3004.
[4] P. Barquinha, A.M. Vila, G. Goncalves, L. Pereira, R. Martins, J.R. Morante, E. Fortunato, IEEE Trans. Electron Devices 55 (2008) 954.
[5] K.S. Son, T.S. Kim, J.S. Jung, M.K. Ryu, K.B. Park, B.W. Yoo, K.C. Park, J.Y. Kwon, S.Y. Lee, J.M. Kim, Electrochem. Solid-State Lett. 12 (2009) H26.
[6] M. Kim, J.H. Jeong, H.J. Lee, T.K. Ahn, H.S. Shin, J.S. Park, J.K. Jeong, Y.G. Mo, H.D. Kim, Appl. Phys. Lett. 90 (2007) 212114.
[7] L. Pereira, P. Barquinha, E. Fortunato, R. Martins, D. Kang, C.J. Kim, H. Lim, I. Song, Y. Park, Thin Solid Films 516 (2008) 1544.
[8] S.I. Kim, C.J. Kim, J.C. Park, I. Song, D.H. Kang, H. Lim, S.W. Kim, E. Lee, J.C. Lee, Y. Park, IEDM Tech. Dig. 583 (2007).
[9] L.A. Majewski, R. Scheoder, M. Grell, Adv. Mater. 17 (2005) 192.
[10] E. Fortunato, N. Correia, P. Barquinha, L. Pereira, G. Goncalves, R. Martins, IEEE Electron Device Lett. 29 (2008) 988.
[11] D.H. Kim, N.G. Cho, H.G. Kim, I.D. Kim, Electrochem. Solid-State Lett. 12 (2009) H198.
[12] C.D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, J.M. Shaw, Science 283 (1999) 822.
[13] C.H. Cheng, F.S. Yeh, A. Chin, Adv. Mater. 23 (2011) 902.
[14] J. Robertson, J. Non-Cryst. Solids 303 (2002) 94.
[15] C.H. Cheng, S.H. Lin, K.Y. Jhou, W.J. Chen, C.P. Chou, F.S. Yeh, J. Hu, M. Huang, T. Arikado, S.P. McAlister, A. Chin, IEEE Electron Device Lett. 30 (2008) 845.
[16] G.D. Wilk, R.M. Wallace, J.M. Anthony, J. Appl. Phys. 89 (2001) 5243.