Test and Analysis of the ESD Robustness for the Diode-Connected a-IGZO Thin Film Transistors

Ya-Hsiang Tai, Hao-Lin Chiu, and Lu-Sheng Chou

Abstract—In this work, wafer level TLP testing is applied to amorphous indium–gallium–zinc–oxide (a-IGZO) thin-film transistors (TFTs) to study the factors of their electrostatic discharge (ESD) robustness. Two kinds of TFTs with N_2O and O_2 treatments are subject to the ESD test. It is found that the contact resistance of the TFTs, instead of the channel quality, dominates the ESD power for them to be damaged.

Index Terms—Amorphous Indium–Gallium–Zinc Oxide thin film transistor (a-IGZO TFT), electrostatic discharge (ESD).

I. INTRODUCTION

A MORPHOUS Indium–Gallium–Zinc Oxide (a-IGZO) thin-film transistors (TFTs) have attracted more attention as one of promising candidates for next generation active matrix flat-panel displays driving element owing to their high mobility, excellent uniformity, and good applicability for low-temperature process [1]–[5]. Since the TFTs are fabricated on the glass substrates in the most applications, the electrostatic discharge (ESD) [6] is an important issue for the fabrication and reliability [7]. TFT LCDs are built from a multi-layer structure on a glass substrate to the whole product module. Most of the processes in the production combine movement, separation and friction. The different ESD types could happen in the production process. For example, some process of the friction may cause the mechanical mode (MM) ESD. The assembly process of glass and driving board may cause the chip-level charge device model (CDM) ESD [8], [9]. Besides, any movement with the human contact may cause the human body mode (HBM) ESD [10].

The transmission line pulsing (TLP) system is commonly used for CMOS device level ESD robustness testing in Integrated Circuits (ICs) is applied in this paper to simulate HBM ESD event [11]. There are a few papers using TLP to study the ESD issues of amorphous and polycrystalline silicon TFTs [12]–[20]. However, there is yet no related report regarding the effect of ESD on a-IGZO TFTs. In this work, the ESD robustness of a-IGZO TFTs in the connection of the diode-connected
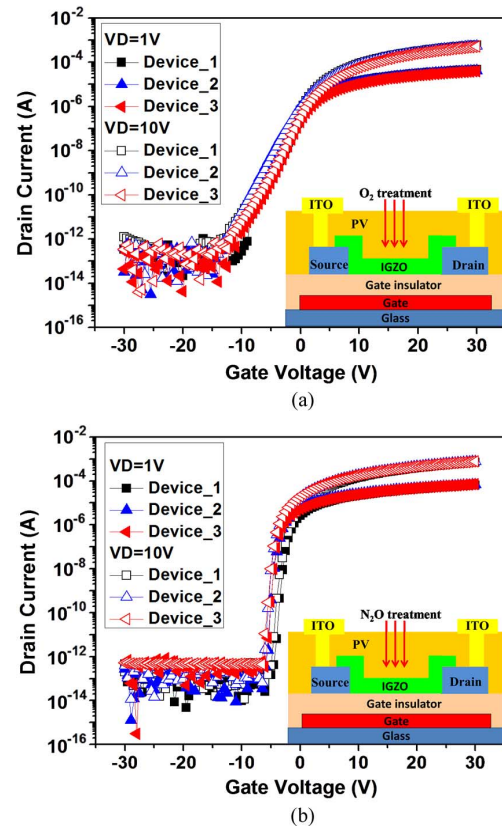
Fig. 1. I_D–V_G transfer characteristics of a-IGZO TFTs with treatment of (a) O_2 and (b) N_2O and their correspondent cross-section schematics.

type with different W/L fabricated on glass substrate is evaluated by the TLP measured secondary breakdown current (It2) and the breakdown voltage (V_{BD}) corresponding to it [21], [22]. Moreover, the ESD effects on the different a-IGZO TFTs with O_2 and N_2O treatment are discussed.

II. DEVICE FABRICATION

The experimental work was based on the bottom-gate TFT devices of co-planar structure with symmetrical Source/Drain (S/D) fabricated on the glass substrate. Shaped Ti/Al/Ti (50/200/50 nm) gate electrodes were capped with 400-nm-thick SiNx gate dielectric, which was deposited by plasma enhanced chemical vapor deposition (PECVD) at 370 °C. The S/D metals were deposited by DC sputtering system at room temperature with Ti/Al/Ti (50/200/50 nm). Then active layer of 30-nm-thick a-IGZO film was deposit by DC magnetron sputtering system using a target of In : Ga : Zn = 1 : 1 : 1 in atomic ratio with the O_2/Ar ratio about 7%. Both N_2O and O_2 treatments were conducted by PECVD at 170 °C with 1500 mTorr for 20 s after
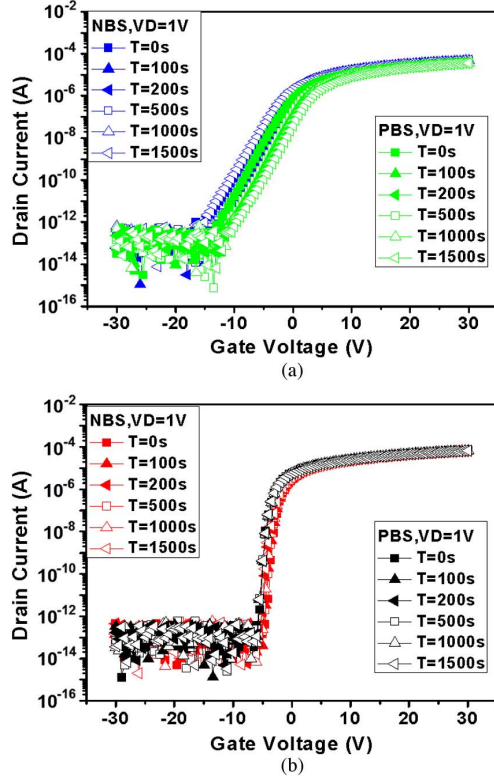
Fig. 2. I_D–V_G transfer curves evolution with gate bias stress for the devices with (a) O_2 treatment and (b) N_2O treatment.

Fig. 3. V_T shift versus stress time under NBS and PBS.
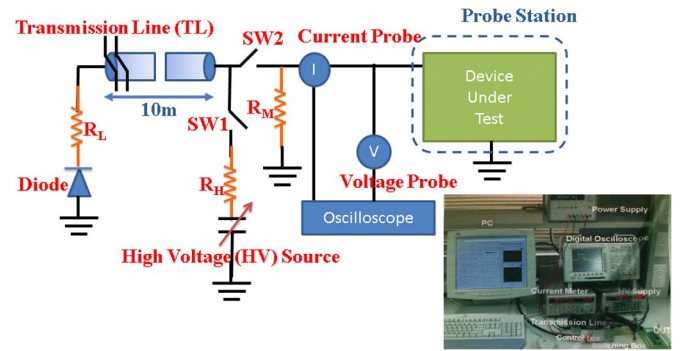
Fig. 4. Configuration of TLP system used in this paper.

the formation of IGZO thin film to obtain the different electrical characteristics for the later discussions in comparison. Both treatments were conducted at the same chamber where to form the passivation without breaking the vacuum.

After that, the devices are capped with 100 nm thick SiOx at 200 °C as protection layer to avoid the disturbance of outside surrounding. Then the via holes and ITO were patterned and shaped for device measurement. The final annealing step was conducted at 330 °C for 2 hours in the oven. The electrical characteristics are measured by Agilent 4156-C system at 25 °C in dark under 1 atmosphere pressure. The threshold voltage (V_T) is defined by the gate voltage (V_G) when the size-normalized drain current I_D reaches 10^{-9} A. The subthreshold swing (S.S) and effective field mobility (μ_{eff}) are extracted at drain voltage $V_D = 1$ V.

III. DEVICE CHARACTERISTICS

Fig. 1 shows the cross section and initial transfer characteristics of fabricated devices with the two different treatments. The values of V_T, μ_{eff} and S.S for the devices with N_2O treatment are -3.93 V, 18.13 cm^2/V·s, and 0.88 V/dec, accordingly, while those for O_2 treated samples are -2.29 V, 10.32 cm^2/V·s, and 1.77 V/dec, correspondingly. It can be seen that the devices with N_2O treatment have better electrical performance than O_2 treated devices do. The worse initial electrical characteristics of O_2 treated device may come from the reason that the O_2 treatment is a process which can generate the n-type oxygen vacancies to increase the conductivity of the device back channel as the situation in ZnO TFTs [23].
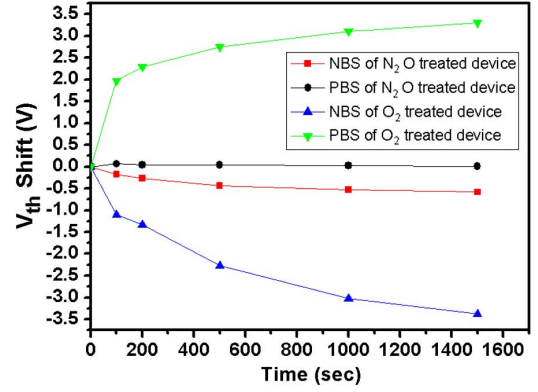
For the electrical stability, the two kinds of device with different treatment were stressed with positive bias stress (PBS) of 30 V and negative bias stress (NBS) of -30 V separately. Fig. 2(a) and (b) shows the I_D–V_G curves of the devices with different treatments before and after stress 1500 s. The trends of V_T shifting value versus time for the two kinds of devices under PBS and NBS are shown in Fig. 3. It is shown that devices with N_2O treatment have better electrical stability than devices with O_2 treatment during the DC stress. The stress result is quite consist with previous report that devices with N_2O treatment have better electrical stability [24]–[26] owing to the effect of repairing of device back channel defect [27], [28].

IV. ESD TESTING AND RESULTS

The configuration of TLP system is shown in Fig. 4 [11]. In this work, the diode-connected IGZO TFTs of different width/length (W/L) with grounded source node are subject to the ESD test as the DUTs. The TLP energy is injected from the gate/drain node to the source node, which means that the diode-connected IGZO TFT is under forward TLP stress. The failure criterion is defined when the permanent damage is observed to cause open characteristic on the TFT or the abnormal turn on resistance is observed on the TLP-measured I–V curve. At this moment, the device is expected to be permanently damaged. Fig. 5(a) shows the TLP system measurement results of the DUTs. One pair of It2 and V_{BD} is indicated for the better illustration. One of the I_D–V_G curves for the damaged TFT is shown in Fig. 5(b) and
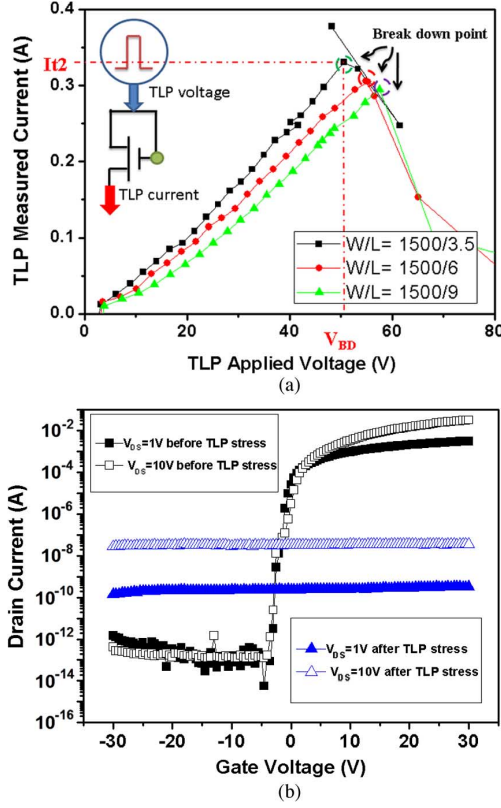
Fig. 5. TLP system measured $I-V$ curves of the a-IGZO TFTs. (b) One of the TLP system measured device's I_D-V_G transfer curve before and after ESD testing.

compared to its initial characteristic to convince the failure of the device.

Fig. 6(a) and (b) shows the dependence of the TLP-measured It2 and V_{BD} of several diode-connected devices, correspondingly. It is found that with increasing W, the value of It2 gets higher while the V_{BD} becomes lower. On the other hand, with increasing L, the value of It2 becomes lower while the V_{BD} becomes higher, as shown in Fig. 7(a) and (b), respectively. It is further observed that the It2 of O_2-treated devices are always higher than the N_2O-treated devices. Fig. 8 plots the multiplication of It2 and V_{BD}, which reflects the breakdown power of ESD for the devices with different W/L. Obviously, the devices with O_2 treatment can sustain higher ESD power than those with N_2O treatment. It hints that there might be a common mechanism resulting in the difference of the treatment effect on the devices in both ESD robustness and performance.

V. ANALYSIS

The optical microscopic (OM) observation and scanning electron microscopic (SEM) graphs of the device damaged by ESD testing are shown in Fig. 9. It is observed that the apparent damage happens not only in the channel but also the contact region, which seems even more damaged.

Fig. 10 illustrates the layout of the TFT testkey and the X marks which denote that the possible weak spots randomly distributed along the width. In the way of layout, the contact area scales with W. If these spots burned out at the very same moment, the ESD power should increase with W for the more
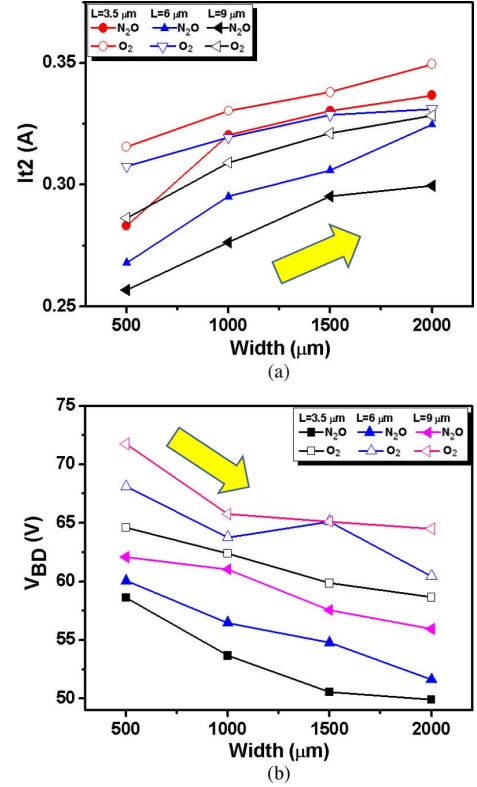

Fig. 6. (a) It2 and (b) V_{BD} versus W for the same L.

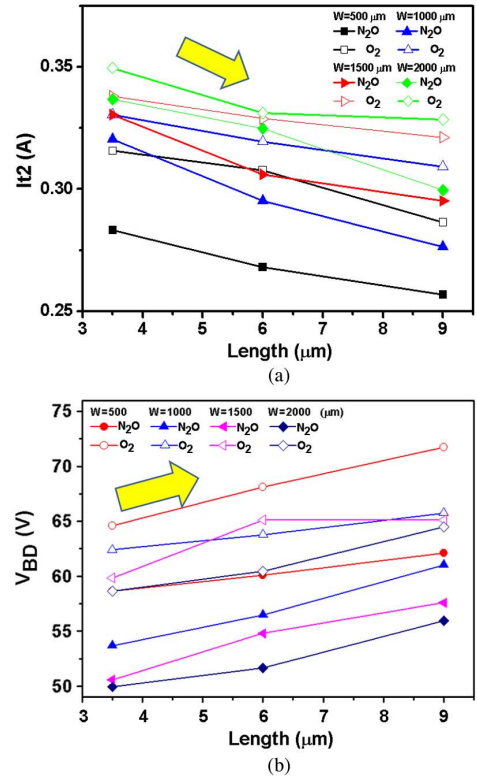Fig. 7. (a) It2 and (b) V_{BD} versus L for the same W.

breakdown area. However, as shown in Fig. 8, the ESD power is independent of W. It depicts that it is the first breakdown of the weakest spot dominates the ESD power where V_{BD} and It2
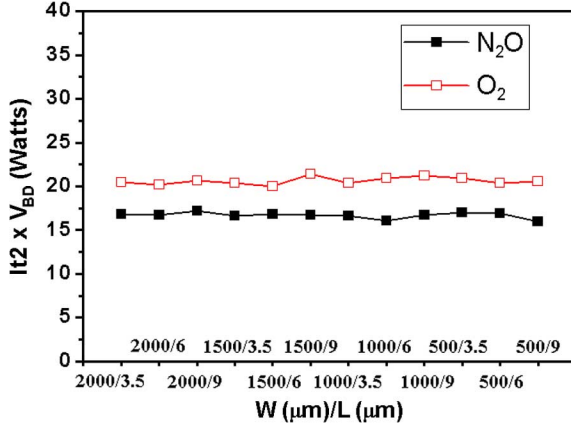
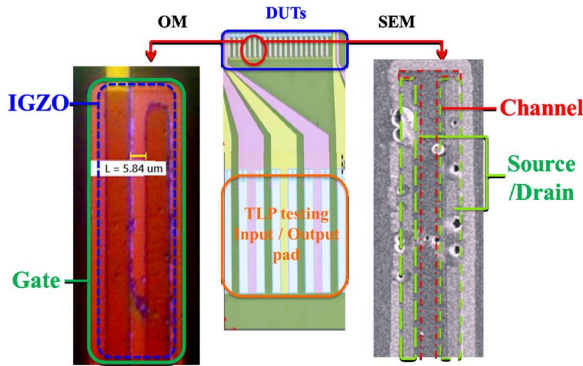Fig. 8. ESD power for the devices with different W/L.

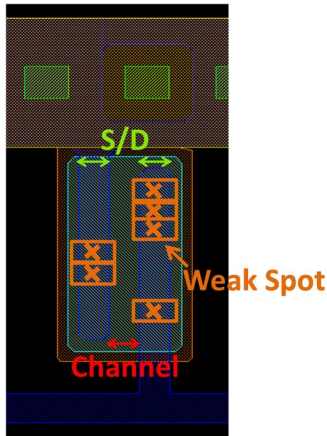Fig. 9. OM and SEM observation of the device after the ESD testing.

Fig. 10. Possible weak spots on the layout of the TFT testkey.

happen. After that, the measured TLP current corresponding to the larger TLP voltage pulse is no more significant since the device has already been damaged.

On the other hand, the contact design for the device with different L is identical. It leads us to think that the ESD power may be more related to the contact region than the channel region, which is consistent with the OM and SEM. Thus, we further analyze the devices with different treatments in the aspect of the contact resistances.

The parasitic contact resistances [29]–[31] are extracted by the measurement of $I_D - V_G$ curves at $V_{DS} = 0.1$ V with dif-
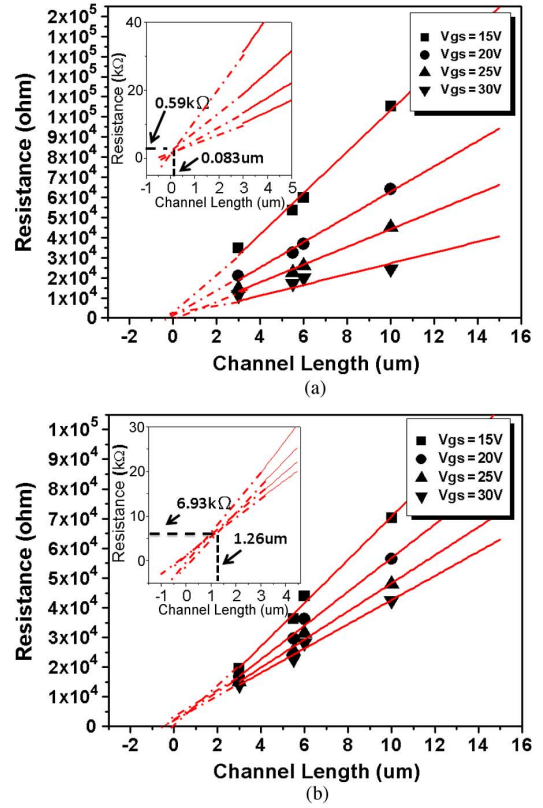

Fig. 11. Parasitic resistance extraction for a-IGZO TFTs of (a) O_2 treatment and (b) N_2O treatment.

ferent channel length [32]–[34], where the ON resistance of TFT (R_{total}) is represented as (1)

$$R_{Total} = \frac{V_{DS}}{I_{DS}} = R_D + R_S + R_{ch} \cdot L \qquad (1)$$

where R_{ch} is the channel resistance per unit channel length, R_s and R_d denote the source and drain resistance, respectively. With the field-effect mobility μ_{eff}, the gate insulator unit capacitor C_{OX}, and the threshold voltage V_{th}, R_{ch} can be represented as (2)

$$R_{ch} = \frac{1}{[\mu_{eff} C_{OX} W (V_G - V_{th} - 0.5 V_D)]} \qquad (2)$$

By substituting (2) into (1), the contact resistances $(R_s + R_d)$ of TFTs with different treatment can be extracted, as shown in Fig. 11. The extraction results of the contact resistance for the TFTs with O_2 and N_2O treatment are 0.588 KΩ and 6.88 KΩ, respectively. The devices with N_2O treatment have much higher contact resistance than those with O_2 treatment.

It implies that the contact resistance plays a role in the ESD robustness. The Emission Microscope (EMMI/InGaAs) observation of the devices under the gate bias of 40 V and drain bias of 20 V is further conducted to check the heat distribution. Fig. 12 shows the heat distribution of devices with O_2 and N_2O treatments on the left and right, respectively. It is found that the hottest area of the N_2O treated device is around the contact area, while that in the O_2 treated device is around the channel.

Such difference depicts that the current dissipates around contact area may be larger than the devices with lower contact resistance under the same applied G/D voltages. Even with better
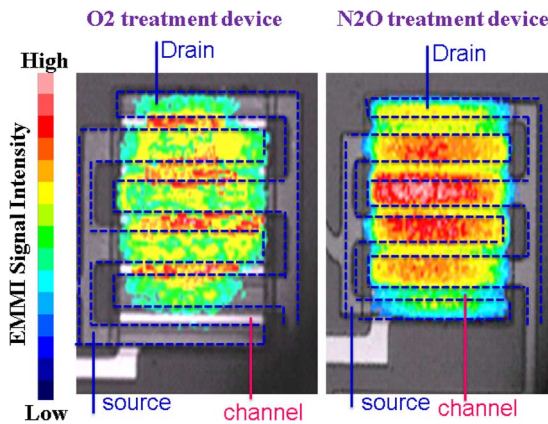
Fig. 12. EMMI/InGaAs observation of the devices with (a) O_2 treatment and (b) N_2O treatment under gate bias of 40 V and drain bias of 20 V.

performance and stability, the device having higher contact resistance can be less robust to ESD. Since the only differences between the two kinds of devices are the channel and contact resistances, we come to a conclusion that the contact resistance is the dominate factor that affects the ESD robustness.

VI. CONCLUSION

In this work, the ESD robustness of the diode-connected IGZO TFT is studied by the wafer level TLP testing. The experiment result shows that the ESD protection ability of the co-planar type diode-connected device varies with different W/L, while the multiplication of breakdown voltage and the It2 is constant. This multiplication value is corresponding to the ESD power and mainly affected by the contact resistance, instead of the active area quality. Even with the worse device performance, the devices having the lower contact resistance may sustain higher applied ESD testing voltage.

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