ECS Journal of Solid State Science and Technology, **2** (9) Q187-Q191 (2013)
2162-8769/2013/2(9)/Q187/5/$31.00 © The Electrochemical Society

Anomalous Gate Current Hump after Dynamic Negative Bias Stress and Negative-Bias Temperature-Instability in p-MOSFETs with $Hf_xZr_{1-x}O_2$ and HfO_2/Metal Gate Stacks

Szu-Han Ho,[a] Ting-Chang Chang,[b,c,z] Chi-Wei Wu,[a] Wen-Hung Lo,[b] Ching-En Chen,[a] Jyun-Yu Tsai,[b] Hua-Mao Chen,[d] Guan-Ru Liu,[b] Tseung-Yuen Tseng,[a] Osbert Cheng,[e] Cheng-Tung Huang,[e] Daniel Chen,[e] and Simon M. Sze[a,b,f]

[a]*Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan*
[b]*Department of Physics, National Sun Yat-Sen University, Kaohsiung 804, Taiwan*
[c]*Advanced Optoelectronics Technology Center, National Cheng Kung University, Tainan, Taiwan*
[d]*Department of Photonics & Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan*
[e]*Device Department, United Microelectronics Corporation, Tainan Science Park, Taiwan*
[f]*Department of Electronics Engineering, Stanford University, Stanford, California 94305, USA*

In this study, the authors investigated an anomalous gate current hump after dynamic negative bias stress (NBS) and negative-bias temperature-instability (NBTI) in $Hf_xZr_{1-x}O_2$ and HfO_2/metal gate p-channel metal-oxide-semiconductor field-effect transistors. This result is attributed to hole trapping in high-k bulk. Measuring gate current under initial through body floating and source/drain floating conditions indicates that holes flow from source/drain to gate. The fitting of the gate current-gate voltage characteristic curve demonstrates that Frenkel-Poole mechanism dominates the conduction under initial. Next, fitting the gate current after dynamic NBS and NBTI indicates Frenkel-Poole then tunneling mechanisms, finally returning to the Frenkel-Poole mechanism. These phenomena can be attributed to hole trapping in high-k bulk and the formula $E_{high\text{-}k}\ \varepsilon_{high\text{-}k} = Q + E_{sio2}\varepsilon_{sio2}$. To further understand the gate current hump, both Zr-undoped and 8 ∼ 10% Zr-doped in high-k bulk devices were used for comparisons. These results indicate that initial gate current is also a significant factor in generating the anomalous gate current hump, and all results obey the hump generation condition of $J_{Tunneling} \ll J_{Frenkel\text{-}Poole}$.
 [DOI: 10.1149/2.027309jss]

Manuscript submitted April 24, 2013; revised manuscript received June 24, 2013. Published July 30, 2013.

As metal-oxide semiconductor field-effect transistors (MOSFETs) continue to shrink, the scaling of SiO_2 gate dielectrics is reaching its critical limit of only a few atomic layers thick. This scale causes an increase in gate current, a rise in power dissipation, and degradation in performance. After many years of research and development, one valid way to solve these problems is by replacing conventional SiO_2 gate dielectric with high-k dielectric, especially with HfO_2 gate dielectric. HfO_2 gate dielectrics have been successfully implemented at the 32 nm technology node and smaller. Furthermore, high-k gate dielectric can be integrated with strained-silicon,[1,2] silicon on insulator (SOI)[3,4,5], and multi-gate techniques to improve device characteristics. High-k dielectric also can be combined with thin-flim transistor device[6–10] and memory device.[11–13] HfO_2 dielectrics have been heavily studied in recent years to replace SiO_2-based dielectrics.[14,15] However, HfO_2 suffers from charge trapping,[16,17,18] mobility degradation, threshold voltage (V_t) instability, and positive bias temperature instability (PBTI) issues. $Hf_xZr_{1-x}O_2$ dielectrics recently have been shown in the development of advanced devices to be a superior gate dielectric.[19–23] In material characteristics, doping Zr in HfO_2 causes gate dielectrics to transform from a monoclinic to a tetragonal crystal structure after annealing, leading to an increase in the value of the dielectric constant. In addition, the grain sizes of $Hf_xZr_{1-x}O_2$ gate dielectrics are small and stable when compared with HfO_2 gate dielectrics. In electrical characteristics, the increasing value of the dielectric constant leads to a decrease in V_t. Diminishing grain size causes $Hf_xZr_{1-x}O_2$ dielectric to oxidize more completely during annealing, resulting in a reduction in charge trapping, an increase in mobility, and a decrease in PBTI.[24,25] Thus, the devices used in this study are HfO_2 and $Hf_xZr_{1-x}O_2$ dielectric p-MOSFETs. This study mainly focuses on hole trapping which induces an anomalous gate current hump after dynamic NBS and NBTI in Zr-undoped and Zr-doped devices. The causes of the hump are explained in this letter.

The HfO_2, $Hf_xZr_{1-x}O_2$ (x = 3% ∼ 5%), and $Hf_xZr_{1-x}O_2$ (x = 8% ∼ 10%)/metal gate p-MOSFETs used in this study were fabricated through the gate last process. First, high quality thermal oxide with thickness of 10 Å was grown as an interfacial layer on a (100) Si substrate. Second, HfO_2, ZrO_2, and HfO_2 dielectrics were deposited in that order by atomic layer deposition (ALD). Then, after annealing, 2 nm thick $Hf_xZr_{1-x}O_2$ was formed. This annealing process may result in crystallization into either monoclinic or tetragonal crystal structures. For HfO_2 dielectric devices, HfO_2 dielectrics were only deposited by ALD, and 2 nm thick HfO_2 was formed in this step. Finally, Ti_xN_{1-x} was deposited by physical vapor deposition (PVD). This is because a metal gate can eliminate gate depletion and resist remote phonon scattering.[26,27] The dimensions of the devices in this study were 0.5 μm width and 1 μm length in dynamic NBS and 0.3 μm width and 1 μm length in NBTI. The p-MOSFETs are stressed in the dynamic condition with 50% duty cycle. A pulse train with high-voltage of $V_t-1.1$ V or $V_t-0.8$ V, low-voltage of 0 V, and frequency of 10 kHz was applied on the gate terminal. Then the p-MOSFETs were stressed in NBTI with $V_t-1.8$ V at 125°C. To further understand gate current, the Zr-undoped and 8% ∼ 10% Zr-doped devices in high-k bulk were used for comparisons. I_g-V_g transfer curves were measured with the source, drain, and body terminals all grounded (SDB) with V_g given from 0 V to −1.3 V. Then through the body floating (BF) and source/drain floating (SDF) processes, the current path and carrier polarity were confirmed. Next, the I_g-V_g curve is fitted by Frenkel-Poole current and tunneling current after 0 s and 1000 s stress. The formula of Frenkel-Poole mechanism is shown below:

$$J = CE_i \exp\left(\frac{-q(\phi_B - \sqrt{qE_i/\pi\varepsilon_i})}{kT}\right), \quad [1]$$

where C is the pre-exponential factor, φ_B is Frenkel-Poole trap energy level, E_i the electric field in the isolation, and ε_i is dielectric constant in the isolation. Then, the formula of tunnel mechanism is shown below:

$$J\alpha E_i^2 \exp\left(\frac{-4(\sqrt{2m_h^*}(q\phi_0)^{1.5})}{3q\hbar E_i}\right), \quad [2]$$

where m_h^* is hole effective mass for SiO_2, and $q\phi_0$ is an effective tunneling barrier height. All experimental curves were measured using an Agilent B1500 semiconductor parameter analyzer and a Cascade M150 probe station.

Figure 1a and 1b show the I_d-V_g and I_g-V_g transfer characteristic curves with −50 mV drain voltage under dynamic NBS during 1000 s

[z]E-mail: tcchang@mail.phys.nsysu.edu.tw

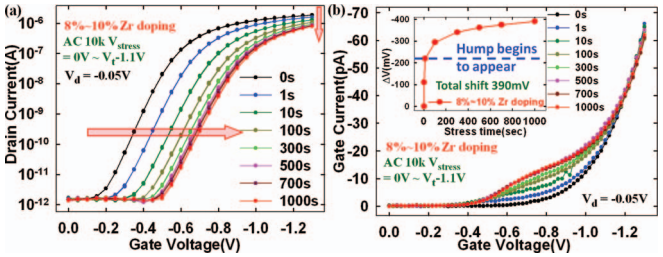

Figure 1. (a) I_d-V_g and (b) I_g-V_g transfer characteristic curves of 8% ~ 10% Zr-doped device as function of stress time under dynamic NBS. A pulse train with high-voltage of $V_t-1.1$ V, low-voltage of 0 V and frequency of 10 kHz was applied on the gate terminal as stress. The sweep was done at $V_d = -0.05$ V. Inset (b) shows V_t-time curves under dynamic NBS.

for the devices with 8% ~ 10% Zr-doping in high-k bulk, respectively. A pulse train with high-voltage of $V_t-1.1$ V, low-voltage of 0 V and frequency of 10 kHz was applied on the gate terminal to stress. Clearly, the V_t shift in the negative direction and on-current is degraded after the dynamic NBS, as shown in Fig. 1a. Furthermore, subthreshold swing degradation is slight. Thus, V_t shift can be mainly attributed to hole trapping in high-k bulk. The inset in Fig. 1b shows the ΔV_t-time curves. V_t total shift is 390 mV in the negative direction under the dynamic NBS at 1000 s. In addition, the gate current generates an anomalous hump under this dynamic NBS. This gate current hump appears clearly in Fig. 1b after 10 s dynamic NBS, when V_t shifts 220 mV, as verified in the inset of Fig. 1b. With hole trapping increasing, the gate current hump becomes clearer. Therefore, the hump is only generated when enough holes are trapped in high-k bulk.

To further understand the causes of the hump, it is necessary to fit and distinguish gate current at initial. Figure 2 shows I_g-V_g characteristics with body floating (BF), source/drain floating (SDF), and source/drain/body all grounded (SDB). Obviously, the I_g-V_g characteristic curve in BF is similar to that in SDB, and the I_g-V_g characteristic curve in SDF is much smaller than those in both SDB and BF. These results indicate that holes transfer from the source/drain to the gate, rather than electrons transferring from gate to body. Moreover, gate current fitted under initial from $V_g = -0.86$ V to $V_g = -1.3$ V, as shown in the inset of Fig. 2, confirms that gate current is the Frenkel-Poole mechanism. Hence, these results show that holes transfer from source/drain to gate with the Frenkel-Poole mechanism.

After confirming the Frenkel-Poole mechanism under initial, the I_g-V_g characteristic curve is fitted after 1000 s dynamic NBS in Fig. 3a, with details of each section in Fig. 3b–3d. Clearly, section A indicates the Frenkel-Poole mechanism, from $V_g = -0.44$ V to $V_g = -0.56$ V, while section B is tunneling mechanism, from $V_g = -0.80$ V to $V_g = -0.92$ V, and section C is again Frenkel-Poole mechanism, from $V_g = -1.16$ V to $V_g = -1.3$ V. In addition, at $V_g < -0.9$ V (V_t), Frenkel-Poole mechanism transfers to tunneling mechanism with increasing V_g. On the contrary, tunneling mechanism

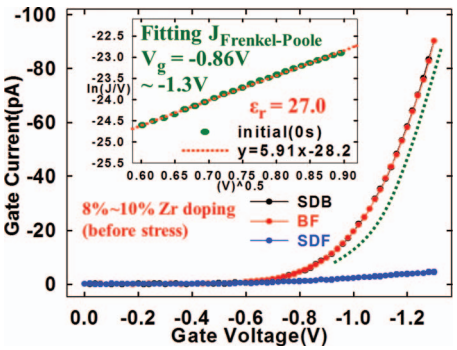

Figure 2. I_g-V_g characteristic curves in the SDF, BF, and SDB conditions. Inset shows that gate current is fitted by Frenkel-Poole model under initial.

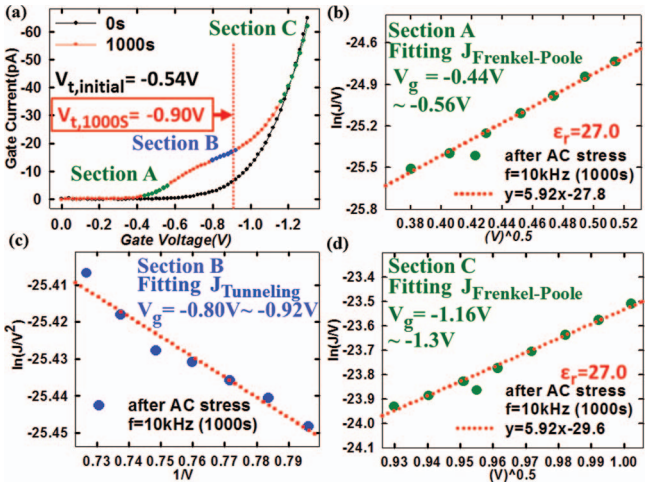

Figure 3. (a) I_g-V_g transfer characteristic curves under initial and after dynamic NBS. Gate currents after dynamic NBS are fitted by (b) Frenkel-Poole model in section A, (c) tunneling model in section B, and (d) Frenkel-Poole model in section C.

transfers to Frenkel-Poole mechanism when $V_g > -0.9$ V (V_t). Then, Frenkel-Poole current path and tunneling current path are a series; whichever current is smaller dominates the current path. Therefore, Frenkel-Poole mechanism dominates current path because $J_{Frenkel\text{-}Poole} \ll J_{Tunneling}$ while tunneling mechanism dominates current path when $J_{Frenkel\text{-}Poole} \gg J_{Tunneling}$. Therefore, the conditions under which a hump is generated is $J_{Frenkel\text{-}Poole} \gg J_{Tunneling}$. The current mechanism cannot be confirmed in the areas between sections A and B, from $V_g = -0.56$ V to $V_g = -0.8$ V as well as between sections B and C, from $V_g = -0.92$ V to $V_g = -1.16$ V because $J_{Frenkel\text{-}Poole} \approx J_{Tunneling}$.

Figure 4a and 4b shows that energy diagrams for $V_g = 0$ V with and without hole trapping in the high k bulk, respectively. Note that $E_{high\text{-}k}$ becomes large and E_{SiO2} becomes smaller with hole trapping. An increase in $E_{high\text{-}k}$ produces a larger Frenkel-Poole current, and

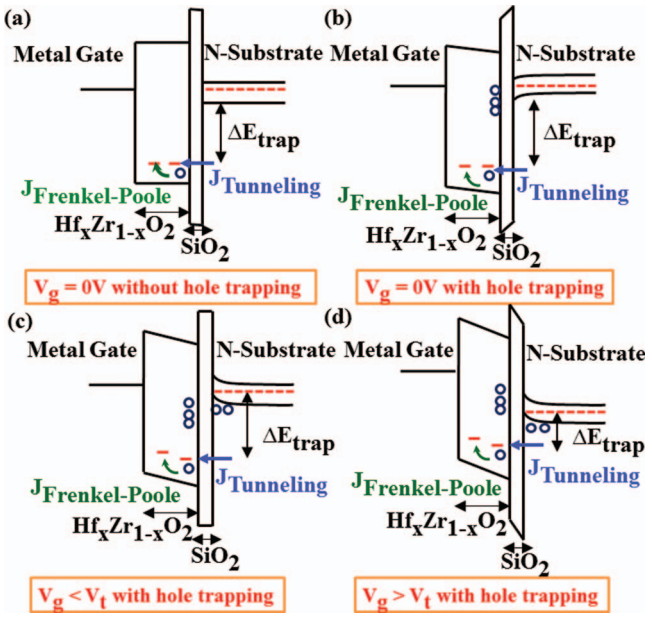

Figure 4. The energy band diagram of $Hf_xZr_{1-x}O_2$/metal gate MOSFETs in the $V_g = 0$ V condition (a) without and (b) with hole trapping. (c) The energy band diagram of $Hf_xZr_{1-x}O_2$/metal gate MOSFETs for $V_g < V_t$ with hole trapping. (d) The energy band diagram of $Hf_xZr_{1-x}O_2$/metal gate MOSFETs for $V_g > V_t$ with hole trapping.

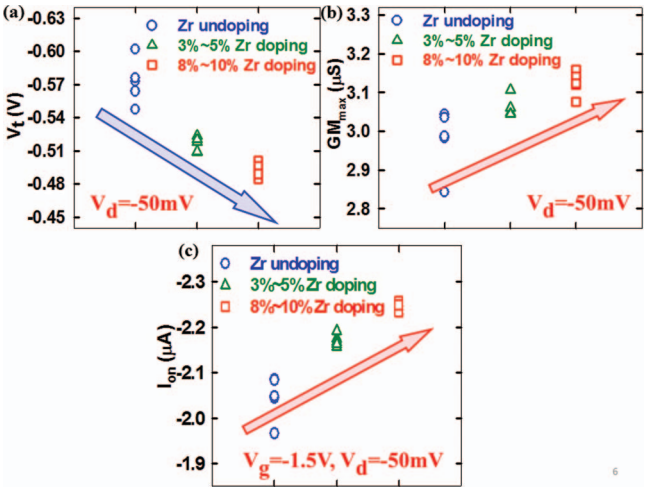

Figure 5. The electric characteristic parameters of (a) V_t (b) GM_{max}, and (c) I_d for Zr-undoped, 3% ~ 5% Zr-doped, and 8% ~ 10% Zr-doped devices.

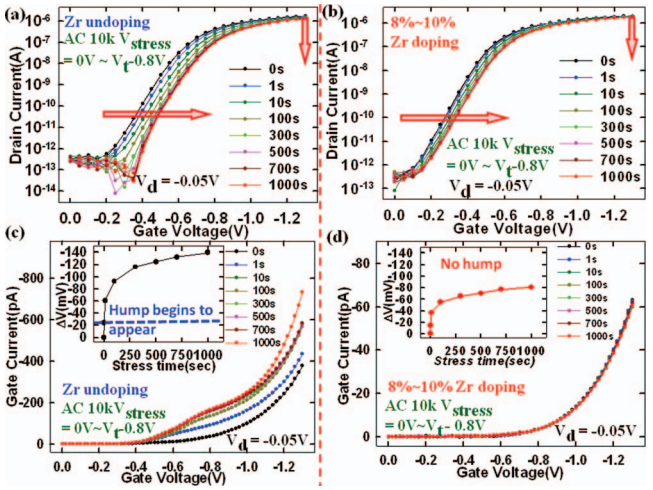

Figure 6. I_d-V_g transfer characteristic curves for (a) Zr-undoped and (b) 8% ~ 10% Zr-doped devices as function of stress time under dynamic NBS with $V_d = -0.05$ V. A pulse train with high-voltage of $V_t-0.8$ V, low-voltage of 0 V and frequency of 10 kHz was applied on the gate terminal to stress. I_g-V_g transfer characteristic curves of (c) Zr-undoped and (d) 8% ~ 10% Zr-doped devices as function of stress time under this dynamic NBS with $V_d = -0.05$ V. Insets (c) and (d) show V_t-time curves under dynamic NBS for Zr-undoped and Zr-doped devices, respectively.

a reduction in E_{SiO2} produces a larger ΔE_{trap}, causing tunneling current to decrease. ΔE_{trap} indicates the energy from the valence band at the surface to trap level. Therefore, with increasing hole trapping, $J_{Frenkel\text{-}Poole}$ is larger than $J_{Tunneling}$. Since the hump generation condition is $J_{Frenkel\text{-}Poole} \gg J_{Tunneling}$, hole trapping leads to a more significant hump. In Fig. 1a and 1b, it can be observed that the more holes that are captured in high-k bulk, the clearer gate current hump we can see. Figure 4c shows energy diagrams in the $V_g < V_t$ situation with hole trapping. The electric field must follow the formula $E_{high\text{-}k}\,\varepsilon_{high\text{-}k} = Q + E_{sio2}\varepsilon_{sio2} = (Q/E_{sio2} + \varepsilon_{sio2})\,E_{sio2} = \varepsilon'\,E_{sio2}$, where Q indicates the quantity of hole trapping ($Q > 0$), E_{sio2} indicates the electric field in the SiO_2, and $E_{high\text{-}k}$ is the electric field in the high-k. The voltage across gate oxide is small when $V_g < V_t$. Hence, Q/E_{sio2} cannot be ignored ($Q \gg E_{sio2}$), resulting in $\varepsilon_{high\text{-}k} < \varepsilon'$ and $E_{high\text{-}k} > E_{sio2}$. When V_g is swept from 0 V to V_t on the device with a large amount of hole trapping in high-k bulk, most of the gate voltage occurs across the $Hf_xZr_{1-x}O_2$ layer. This is the reason why $J_{Frenkel\text{-}Poole}$ after dynamic NBS appears earlier than $J_{Frenkel\text{-}Poole}$ under initial. Nevertheless, relatively smaller voltage occurs across the SiO_2 layer, leading to a slight rise in $J_{Tunneling}$ due to a small variation in ΔE_{trap}. With an increase in V_g, $J_{Frenkel\text{-}Poole}$ increases significantly while $J_{Tunneling}$ changes only slightly. This causes $J_{Frenkel\text{-}Poole}$ to change to $J_{Tunneling}$. At the beginning stages, $J_{Frenkel\text{-}Poole}$ appears in section A (Fig. 3a) owing to the supply of holes exceeding the demand ($J_{Tunneling} \gg J_{Frenkel\text{-}Poole}$). Next, $J_{Tunneling}$ appears in section B (Fig. 3a), because the supply of holes is unable to meet the demand ($J_{Tunneling} \ll J_{Frenkel\text{-}Poole}$). Figure 4d shows energy diagrams in the $V_g > V_t$ condition with hole trapping. The electric field should also obey formula $E_{high\text{-}k}\,\varepsilon_{high\text{-}k} = Q + E_{sio2}\varepsilon_{sio2} = (Q/E_{sio2} + \varepsilon_{sio2})\,E_{sio2}$. On the contrary, V_g occurring across SiO_2 and $Hf_xZr_{1-x}O_2$ in the $V_g > V_t$ condition is large, causing Q/E_{sio2} to be ignored ($Q \ll E_{sio2}$). This result leads to $\varepsilon_{high\text{-}k} > \varepsilon_{sio2}$ and $E_{high\text{-}k} < E_{sio2}$. Therefore, with increasing V_g, ΔE_{trap} decreases, and $J_{Tunneling}$ increases sharply due to the exponential dependence on ΔE_{trap}. This is the reason why $J_{Tunneling}$ changes to $J_{Frenkel\text{-}Poole}$. Finally, $J_{Frenkel\text{-}Poole}$ appears in section C (Fig. 3a), since the supply of holes exceeds the demand ($J_{Tunneling} \gg J_{Frenkel\text{-}Poole}$).

To further understand the generation of gate current hump, the Zr-undoped and 8% ~ 10% Zr-doped devices in high-k bulk are compared after dynamic NBS. Before this comparison, it is necessary to confirm the dielectrics of devices containing Zr. Thus, the electric characteristic parameter of Zr-undoped, 3% ~ 5% Zr-doped, and 8% ~ 10% Zr-doped devices are compared. Figure 5a, 5b, and 5c clearly show an increase of Zr concentration in high-k bulk, a decrease in V_t, an increase in GM_{max}, and an increase in I_d at higher levels of Zr doping. First, V_t decreases since the value of dielectric constant (ε_r) increases in the Zr-doped device. Second, GM_{max} increases since the grain size of Zr-doped devices diminishes, leading to more complete oxidization in Zr-doped devices after annealing. Hence, charge trapping decreases and mobility increases. Third, I_d increases due to V_t decreasing and GM_{max} increasing. All these electric measurement results show a good fit with previous research.[19,20] Therefore, we can infer that the dielectrics of devices actually contain Zr.

After comparison of these electric characteristic parameters, Zr-undoped and 8% ~ 10% Zr-doped devices were stressed in dynamic NBS. Fig. 6a and 6b shows the I_d-V_g transfer characteristic curves with −50 mV drain voltage under the dynamic NBS during 1000 s for Zr-undoped and 8% ~ 10% Zr-doped devices in high-k bulk, respectively. A pulse train with high-voltage of $V_t-0.8$ V, low-voltage of 0 V and frequency of 10 kHz was applied on the gate terminal as stress. Obviously, both V_t curves shift in the negative direction and on-current is degraded after the dynamic NBS. Furthermore, both subthreshold swing degradations are slight. Thus, V_t shift can be attributed mainly to hole trapping in high-k bulk. Next, to further understand gate current hump generation, Fig. 6c and 6d are compared with Fig. 1b. Figure 6c and 6d show the I_g-V_g transfer characteristic curves with −50 mV drain voltage after dynamic NBS in Zr-undoped and 8% ~ 10% Zr-doped devices in high-k bulk, respectively. A pulse train with high-voltage of $V_t-0.8$ V, low-voltage of 0 V is given to stress and a frequency of 10 kHz was applied on the gate terminal. Obviously, the gate current hump appears in the Zr-undoped device, but does not in the Zr-doped device. The inset of Fig. 6c and 6d shows the ΔV_t-time curves. V_t shifts 140 mV in the negative direction in the Zr-undoped device, while shifting 81 mV in the negative direction in the Zr-doped device. This evidence indicates that hole trapping in the Zr-undoped device is more significant than in the Zr-doped device after dynamic NBS. This is because diminishing grain size makes the $Hf_xZr_{1-x}O_2$ dielectric oxidize more completely during annealing than does the HfO_2 dielectric, causing a reduction in hole trapping after dynamic NBS. According to the previous ratiocination, the gate current hump appears when $J_{Tunneling} \ll J_{Frenkel\text{-}Poole}$. Hole trapping can enhance this condition, making the hump more prominent. Therefore, one reason for the gate hump is that enough hole trapping has occurred in the high k layer, while the other reason is the initial gate current. In order to confirm these two reasons, Fig. 1b and Fig. 6d with the same dielectric device, but different stress conditions, should be compared. Thus, the initial gate current is about the same, at about 64 pA. The

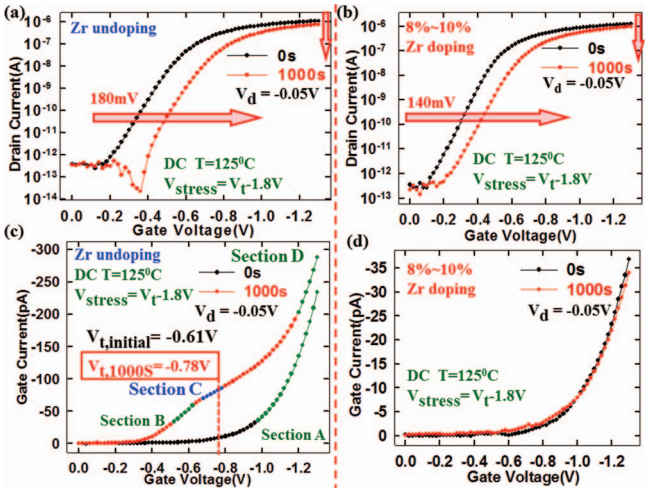

Figure 7. I_d-V_g transfer characteristic curves of (a) Zr-undoped and (b) 8% ∼ 10% Zr-doped devices before and after NBTI at 125°C measured at 30°C with $V_d = -0.05$ V. $V_t-1.8$ V was applied on the gate terminal to stress. I_g-V_g transfer characteristic curves of (c) Zr-undoped and (d) 8% ∼ 10% Zr-doped devices before and after this NBTI measured at 30°C with $V_d = -0.05$ V.

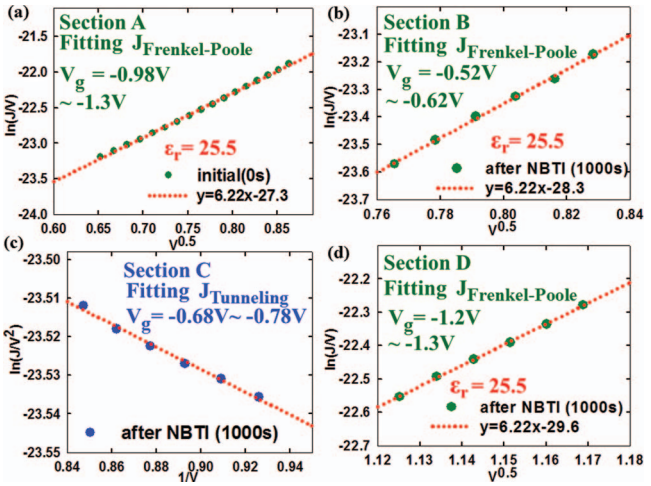

Figure 8. Gate currents after NBTI are fitted in Zr-undoped devices by (a) Frenkel-Poole model in section A under initial, (b) Frenkel-Poole model in section B, (c) tunneling model in section C, and (d) Frenkel-Poole model in section D.

gate current of the device with a lower stress voltage displays no hump, while that with a higher stress voltage exhibits one. These results also show that enough hole trapping can generate a gate current hump. Next, a comparison of Fig. 1b and Fig. 6c with different dielectric devices and stress conditions indicates that both devices have the gate current hump. The inset of Fig. 6c shows that gate current begins to display a hump when $\Delta V_t = 24$ mV; in contrast, the inset of Fig. 1b shows that gate current begins to display a hump when $\Delta V_t = 220$ mV. Obviously, the gate current of the Zr-undoped device more easily displays a hump. This result can be attributed to initial gate current. The initial gate current of the Zr-undoped device (378 pA) is larger than that of the Zr-doped device (64 pA), as shown in Figs. 1b and 6c. In addition, because the hump generation condition is $J_{Tunneling} \ll J_{Frenkel-Poole}$, the initial gate current is Frenkel-Poole current, as shown in Fig. 2. Therefore, whichever Frenkel-Poole current is larger between the undoped or Zr-doped devices generates the gate current hump more easily. Therefore, the gate current hump requires not only sufficient hole trapping in high k bulk, but also requires a sufficiently large initial gate current. These results obey the hump generation condition $J_{Tunneling} \ll J_{Frenkel-Poole}$.

Figures 7a and 7b shows the I_d-V_g transfer characteristic curves measured at 30°C with −50 mV drain voltage before and after NBTI at 125°C for the Zr-undoped and Zr-doped devices, respectively. Clearly, on-current are both degraded and V_t shifts in the negative direction at 1000 s NBTI. Furthermore, subthreshold swing degradation is slight. Thus, V_t shift also can be attributed mainly to hole trapping in the high-k bulk. Figure 7c and 7d shows I_g-V_g transfer characteristic curves at the same conditions for the same devices, respectively. Obviously, after NBTI, the gate current hump is significant in Zr-undoped devices while not appearing in the 8% ∼10% Zr-doped devices. This is because hole trapping in the high-k layer after NBTI is more and the initial gate current is larger in the Zr-undoped device as previously concluded. Figure 8a–8d shows section details of the fitting gate current before and after NBTI described completely in Fig. 7c. Clearly, section A indicates the Frenkel-Poole mechanism, from $V_g = -0.98$ V to $V_g = -1.3$ V; section B is also the Frenkel-Poole mechanism, from $V_g = -0.52$ V to $V_g = -0.62$ V; section C is tunneling mechanism, from $V_g = -0.68$ V to $V_g = -0.78$ V; and section D is again Frenkel-Poole mechanism, from $V_g = -1.2$ V to $V_g = -1.3$ V. The results show that gate current at initial is Frenkel-Poole mechanism while after NBTI alternates as Frenkel-Poole, tunneling, and Frenkel-Poole mechanisms. These phenomena of gate current hump after NBTI are similar with that after dynamic NBS. Thus, this gate current hump is also generated by hole trapping in high-k bulk.

In this paper, the V_t shifts in the negative direction and a hump is generated in the I_g-V_g transfer characteristic curves after dynamic NBS and NBTI, results of hole trapping in high-k bulk. Fitting and distinguishing gate current under initial shows holes transfer through the Frenkel-Poole mechanism from the source and drain. Gate current fitting after dynamic NBS and NBTI indicates that $J_{Frenkel-Poole}$ changes to $J_{Tunneling}$ when $V_g < V_t$ owing to the influence of $E_{high-k} > E_{sio2}$, while $J_{Tunneling}$ changes to $J_{Frenkel-Poole}$ when $V_g > V_t$ due to the influence of $E_{high-k} < E_{sio2}$. These phenomena can be attributed to the fact that the electric field must follow the formula $E_{high-k}\,\varepsilon_{high-k} = Q + E_{sio2}\varepsilon_{sio2}$. Subsequently, from Zr-undoped and Zr-doped devices after dynamic NBS, we conclude that the gate current hump requires both sufficient hole trapping and larger initial gate current. These results obey the hump generation condition $J_{Tunneling} \ll J_{Frenkel-Poole}$.

Part of this work was performed at United Microelectronics Corporation. The work was supported by the National Science Council under Contract No. NSC 101-2120-M-110-002.

References

1. Y. J. Kuo, T. C. Chang, P. H. Yeh, S. C. Chen, C. H. Dai, C. H. Chao, T. F. Young, Osbert Cheng, and C. T. Huang, *Thin Solid Films*, **517**, 1715 (2009).
2. Y. J. Kuo, T. C. Chang, C. H. Dai, S. C. Chen, J. Lu, S. H. Ho, C. H. Chao, T. F. Young, Osbert Cheng, and C. T. Huang, *Electrochemical and Solid-State Lett.*, **12**, H32 (2009).
3. C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, S. C. Chen, C. T. Tsai, W. H. Lo, S. H. Ho, G. Xia, and O. Cheng, *Surface & Coatings Technology*, **205**, 1470 (2010).
4. C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, F. Y. Jian, W. H. Lo, S. H. Ho, C. E. Chen, W. L. Chung, and J. M. Shih et al., *IEEE Electron Device Lett.*, **32**(7), 847 (2011).
5. W. H. Lo, T. C. Chang, C. H. Dai, W. L. Chung, C. E. Chen, S. H. Ho, O. Cheng, and C. T. Huang, *IEEE Electron Device Lett.*, **33**(3), 303 (2012).
6. Liang-Yu Su, Huang-Kai Lin, Chia-Chin Hung, and JianJang Huang, Senior Member, *IEEE Journal Of Display Technology*, **8**(12), 695 (2012).
7. C. J. Chiu, S. P. Chang, and S. J. Chang, Member, *IEEE Electron Device Lett.*, **31**(11), 1245 (2010).
8. Jae Sang Lee, Seongpil Chang, Sang-Mo Koo, and Sang Yeol Lee, *IEEE Electron Device Lett.*, **31**(3), 225 (2010).
9. C. T. Tsai, T. C. Chang, S. C. Chen, I. Lo, S. W. Tsao, M. C. Hung, J. J. Chang, C. Y. Wu, and C. Y. Huang, *Appl. Phys. Lett.*, **96**, 242105 (2010).
10. T. C. Chen, T. C. Chang, C. T. Tsai, T. Y. Hsieh, S. C. Chen, C. S. Lin, M. C. Hung, C. H. Tu, J. J. Chang, and P. L. Chen, *Appl. Phys. Lett.*, **97**, 112104 (2010).
11. Y. E. Syu, T. C. Chang, T. M. Tsai, Y. C. Hung, K. C. Chang, M. J. Tsai, M. J. Kao, and S. M. Sze, *IEEE Electron Device Lett.*, **32**(4), 545 (2011).
12. T. C. Chang, F. Y. Jian, S. C. Chen, and Y. T. Tsai, *Mater. Today*, **14**(12), 608 (2011).

13. M. C. Chen, T. C. Chang, C. T. Tsai, S. Y. Huang, S. C. Chen, C. W. Hu, S. M. Sze, and M. J. Tsai, *Appl. Phys. Lett.*, **96**, 262110 (2010).
14. C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, S. H. Ho, T. Y. Hsieh, W. H. Lo, C. E. Chen, J. M. Shih, and W. L. Chung et al., *Appl. Phys. Lett.*, **99**, 012106 (2011).
15. C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, W. H. Lo, S. H. Ho, C. E. Chen, J. M. Shih, H. M. Chen, and B. S. Dai et al., *Appl. Phys. Lett.*, **98**, 092112 (2011).
16. C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, Y. C. Hung, W. H. Lo, S. H. Ho, C. E. Chen, J. M. Shih, and W. L. Chung et al., *Thin Solid Films*, **520**, 1511 (2011).
17. W. H. Lo, T. C. Chang, J. Y. Tsai, C. H. Dai, C. E. Chen, S. H. Ho, H. M. Chen, O. Cheng, and C. T. Huang, *Appl. Phys. Lett.*, **100**, 152102 (2012).
18. M. Chang, M. Jo, S. Jung, J. Lee, S. Jeon, and H. Hwang, *Appl. Phys. Lett.*, **94**, 262107 (2009).
19. D. H. Triyoso, R. I. Hegde, J. K. Schaeffer, R. Gregory, X.-D. Wang, M. Canonico, D. Roan, E. A. Hebert, K. Kim, J. Jiang, and R. Rai et al., *J. Vac. Sci. Technol., B*, **25**(3), 845 (2007).
20. R. I. Hegde, D. H. Triyoso, P. J. Tobin, S. Kalpat, M. E. Ramon, H.-H. Tseng, J. K. Schaeffer, E. Luckowski, W. J. Taylor, and C. C. Capasso et al., *IEDM Technical Digest*, 35 (2005).
21. D. H. Triyoso, Senior Member, IEEE, R. I. Hegde, Member, IEEE, J. Jiang, J. K. Schaeffer, Member, IEEE, and M. V. Raymond, *IEEE Electron Device Lett.*, **29**(1), 57 (2008).
22. D. H. Triyoso, R. I. Hegde, J. K. Schaeffer, D. Roan, P. J. Tobin, S. B. Samavedam, and B. E. White, Jr., *Appl. Phys. Lett.*, **88**, 222901 (2006).
23. D. H. Triyoso, R. I. Hegde, R. Gregory, G. Spencer, J. K. Schaeffer, and M. Raymond, *IC Design and Technology, 2009. ICICDT '09. IEEE International Conference on*, pp. 89–92 (2009).
24. H. S. Jung, S. A. Lee, S. h. Rha, S. Y. Lee, H. K. Kim, D. H. Kim, K. H. Oh, J. M. Park, W. H. Kim, and M. W. Song et al., *IEEE Trans. Electron Devices.*, **58**(7), 2094 (2011).
25. C. K. Chiang, J. C. Chang, W. H. Liu, C. C. Liu, J. F. Lin, C. L. Yang, and J. Y. Wu, *Reliability Physics Symposium (IRPS), 2012 IEEE International*, pp. GD.3.1–GD.3.4 (2012).
26. W. J. Zhu, Member, IEEE, and T. P. Ma, Fellow, *IEEE Electron Device Lett.*, **25**(2), 89 (2004).
27. R. Chau, Senior Member, IEEE, S. Datta, Member, IEEE, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, *Electron Devices Lett.*, **25**(6), 408 (2004).