AIP Applied Physics Letters

Demonstrating 1nm-oxide-equivalent-thickness HfO2/InSb structure with unpinning Fermi level and low gate leakage current density

Hai-Dang Trinh, Yueh-Chin Lin, Minh-Thuy Nguyen, Hong-Quan Nguyen, Quoc-Van Duong, Quang-Ho Luc, Shin-Yuan Wang, Manh-Nghia Nguyen, and Edward Yi Chang

Citation: Applied Physics Letters **103**, 142903 (2013); doi: 10.1063/1.4823584
View online: http://dx.doi.org/10.1063/1.4823584
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/103/14?ver=pdfcov
Published by the AIP Publishing

Articles you may be interested in

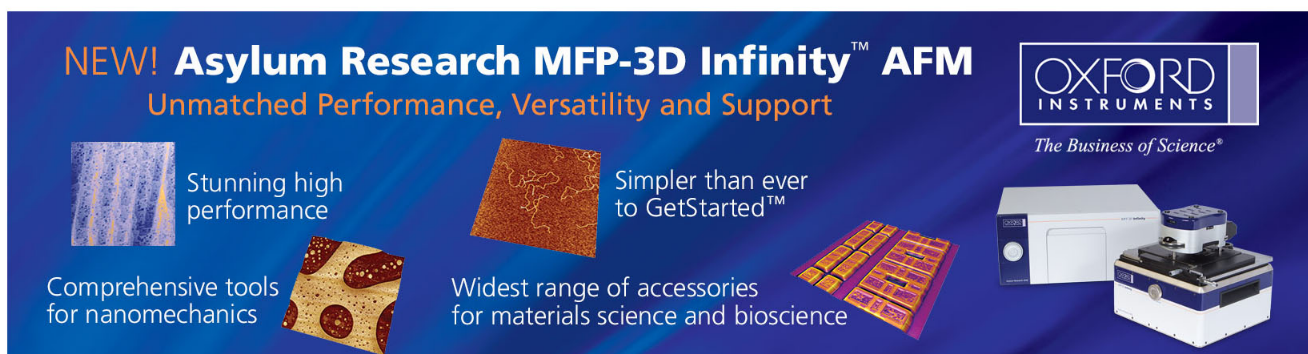
Effect of NH3 plasma treatment on the interfacial property between ultrathin HfO2 and strained Si0.65Ge0.35 substrate
J. Appl. Phys. **113**, 044105 (2013); 10.1063/1.4788907

1-nm-capacitance-equivalent-thickness HfO2/Al2O3/InGaAs metal-oxide-semiconductor structure with low interface trap density and low gate leakage current density
Appl. Phys. Lett. **100**, 132906 (2012); 10.1063/1.3698095

Excellent electrical properties of Ti O 2 Hf Si O Si O 2 layered higher- k gate dielectrics with sub- 1 nm equivalent oxide thickness
Appl. Phys. Lett. **92**, 212902 (2008); 10.1063/1.2929680

Atomic-layer-deposited Hf O 2 on In 0.53 Ga 0.47 As : Passivation and energy-band parameters
Appl. Phys. Lett. **92**, 072901 (2008); 10.1063/1.2883967

Electrical conduction and band offsets in Si/Hf x Ti 1x O 2 / metal structures
J. Appl. Phys. **95**, 7936 (2004); 10.1063/1.1703821



This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Wed, 30 Apr 2014 08:49:25

CrossMark

Demonstrating 1 nm-oxide-equivalent-thickness HfO_2/InSb structure with unpinning Fermi level and low gate leakage current density

Hai-Dang Trinh,[1,2,a)] Yueh-Chin Lin,[1] Minh-Thuy Nguyen,[2] Hong-Quan Nguyen,[1] Quoc-Van Duong,[2] Quang-Ho Luc,[1] Shin-Yuan Wang,[3] Manh-Nghia Nguyen,[2] and Edward Yi Chang[1,3,b)]

[1]*Department of Materials Science and Engineering, National Chiao Tung University, 1001 University Road, Hsinchu, Taiwan*
[2]*Department of Physics, Hanoi National University of Education, 136 Xuan Thuy, Cau Giay, Hanoi, Vietnam*
[3]*Department of Electronic Engineering, National Chiao Tung University 1001, University Rd., Hsinchu 300, Taiwan*

(Received 17 August 2013; accepted 14 September 2013; published online 30 September 2013)

In this work, the band alignment, interface, and electrical characteristics of HfO_2/InSb metal-oxide-semiconductor structure have been investigated. By using x-ray photoelectron spectroscopy analysis, the conduction band offset of 1.78 ± 0.1 eV and valence band offset of 3.35 ± 0.1 eV have been extracted. The transmission electron microscopy analysis has shown that HfO_2 layer would be a good diffusion barrier for InSb. As a result, 1 nm equivalent-oxide-thickness in the 4 nm HfO_2/InSb structure has been demonstrated with unpinning Fermi level and low leakage current of 10^{-4} A/cm^{-2}. The D_{it} value of smaller than 10^{12} eV^{-1}cm^{-2} has been obtained using conduction method. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4823584]

InSb has been raised an attention for ultra-low power, high-speed field effect transistor (FET) application due to its high electron and hole mobility as compared to Si and other III-V compounds.[1–3] Due to its narrow bandgap, InSb has been preferred to apply to quantum-well (QW),[4,5] nanowire (NW),[6,7] or tunnel (T) FET architectures.[8] The high performance InSb-based QWFETs with very high-speed low supply voltage (≤ 0.5 V) have been demonstrated for both n- and p-channel devices. Both kinds of these devices have been showed much improvement in speed and power consumption as compared with start-of-the-art Si transistors.[3–5] For those applications, the deposition of high k gate dielectric on InSb with good interface quality is very important for the effective performance of devices. Moreover, the scaling down of high k dielectric into sub-nanometer scale is of critical importance since devices have been getting smaller. In previous works, we have demonstrated that the electrical properties of Al_2O_3/InSb metal-oxide-semiconductor capacitors (MOSCAPs) are essential to the thermal (such as deposition and annealing) steps during the fabrication of devices.[9,10] The low thermal budget of InSb would lead to the out-diffusion of Sb and In into Al_2O_3 layer under high temperature thermal step and thus, degrading the Al_2O_3/InSb interface as well as high k quality.[9,10] In this work, we study the HfO_2/InSb structure, focusing on the band alignment, interface characteristics, and down scaling oxide thickness into sub-nm. It is found that HfO_2 can be a better diffusion barrier layer for InSb as compared to Al_2O_3. A 1 nm equivalent-oxide-thickness HfO_2/InSb MOSCAPs with good interface quality, unpinning Fermi level, and low leakage current is demonstrated.

Wafers used in this work are (100) n-type InSb substrate with doping concentration of 2.2×10^{16} cm^{-3} at room temperature. The process for the fabrication of MOSCAPs is similar to previous studies but HfO_2 gate oxide was used instead of Al_2O_3.[9,10] After degreasing in acetone and isopropanol, sample was dipped in HCl 4% solution for removing native oxides, following by rinsing in deionized water and blown dry by N_2 gas. Samples were then loaded into the atomic-layer-deposition (ALD) chamber (Cambridge NanoTech Fiji 202 DSC) within 5 min. In ALD chamber, several pulses of trimethylaluminium (TMA)/Ar were performed before the deposition of 40 cycles (CYC) HfO_2 at 250 °C using tetrakis-ethylmethylaminohafnium (TEMAHf) and water as precursors. TMA/Ar pulses were used because TMA has an effect not only in further removing III-V's native oxides but also reducing the dangling bonds at III-V surface.[11–14] The use of TMA pretreatment could help to reduce defects at InSb surface by satisfying electron counting rule as proposed by J. Robertson and L. Lin.[11] Experimentally, the deposition of a very thin layer of Al_2O_3 (2 CYC) before depositing HfO_2 has shown significant improvement of high k/InGaAs interface.[12] After high k deposition, Ni/Au gate metal was formed via photolithography/e-beam evaporation/liftoff process. Finally, the Au/Ge/Ni/Au metal was deposited for backside ohmic contact and followed by post metal deposition annealing (PMA) at 250 °C, in N_2, for 30 s.

The band alignment of HfO_2/InSb structure is firstly evaluated. The valence band offset ΔE_V of HfO_2/InSb structure is determined from XPS spectra, via the following equation:[10,15]

$$\Delta E_V = E^{HfO/InSb}_{Hf4f} - E^{HfO/InSb}_{Sb4d} + (E^{InSb}_{Sb4d} - E^{InSb}_{VBM}) - (E^{HfO}_{Hf4f} - E^{HfO}_{VBM}), \quad (1)$$

where $E^{HfO/InSb}_{Hf4f} - E^{HfO/InSb}_{Sb4d}$ is the energy difference between Hf 4f and Sb 4d core levels measured in 3 nm HfO_2/InSb interface; $E^{InSb}_{Sb4d} - E^{InSb}_{VBM}$ and $E^{HfO}_{Hf4f} - E^{HfO}_{VBM}$ are the differences

a)Electronic mail: trinhhaidang@gmail.com
b)Electronic mail: edc@mail.nctu.edu.tw

 © 2013 AIP Publishing LLC

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Wed, 30 Apr 2014 08:49:25

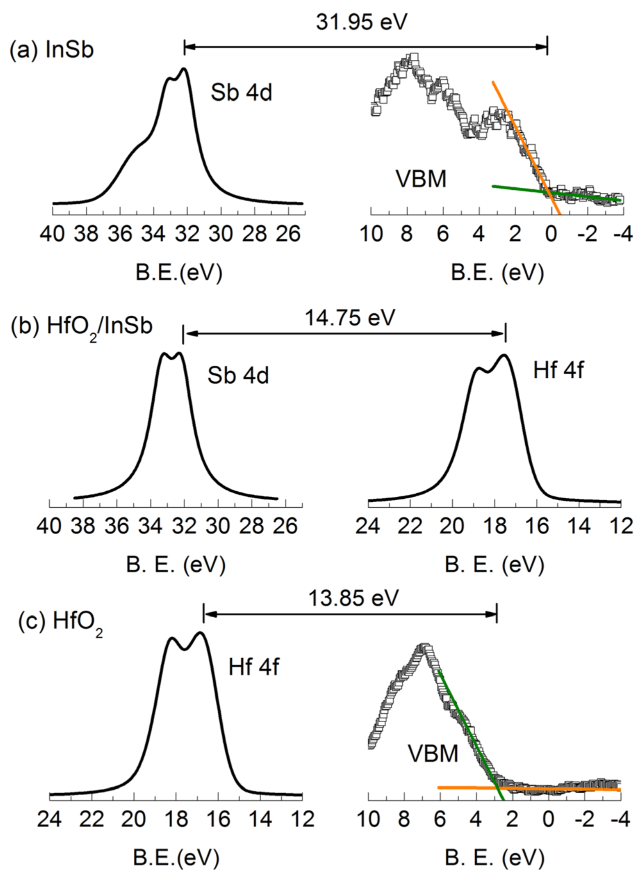


FIG. 1. XPS spectra of (a) Sb 4d core level and valence band of InSb surface (after HCl cleaning), (b) Hf 4f and In 4d core levels at the 3 nm HfO_2/InSb interface, and (c) Hf 4f and valence band of 8 nm HfO_2 film.

between valence band maximum (VBM) energies and corresponding Sb 4d core level in InSb and Hf 4f core level in 8-nm-thick HfO_2/InSb, respectively. Figure 1 shows the Sb 4d, Hf 4f, and VBM spectra of the samples for valence band offset measurement. The procedure for extracting core levels and VBMs was similar to what has been done for Al_2O_3/InSb structure.[10] From Eq. (1) and the data showed in Fig. 1, the value of $\Delta E_V \sim 3.35 \pm 0.1\,\text{eV}$ was extracted. The band gap of HfO_2 was deduced from the O 1 s energy lose spectra to be $5.3 \pm 0.1\,\text{eV}$ (data not shown). By combining these two data with the InSb band gap of 0.17 eV at room temperature, the conduction band offset ΔE_C of HfO_2/InSb struture is deduced to be $1.78 \pm 0.1\,\text{eV}$.

Figure 2 shows the Sb 3d plus O 1 s and In $3d_{3/2}$ spectra of InSb surface before and after HCl cleaning, and HfO_2/InSb interface after deposition and after annealing at 250 °C for 30 s, respectively. Because the O1s and Sb $3d_{5/2}$ spectra are overlapped, the change of Sb-O bonds would be verified by Sb $3d_{3/2}$ spectrum. As shown in the In $3d_{3/2}$ and Sb $3d_{3/2}$ spectra in the Figs. 2(a) and 2(b), the Sb-O and In-O bonds were reduced after HCl cleaning, especially for In-O bonds. Compared to the InAs case by using the same HCl clean,[13] the reduction of In-O bonds is similar but the reduction As-O bonds is more significant than that of Sb-O bonds. The less significant reduction of Sb-O bonds might due to the rapid re-oxidation of Sb-O oxides during air exposure after HCl clean. After loading into ALD chamber and depositing high k, there is a reduction of Sb-O bonds as indicated in Fig. 1(c), Sb $3d_{3/2}$ spectrum. This reduction might come from two reasons (1) the self-cleaning effect by TMA pre-clean step[9,16] and (2) the Sb-O oxides changed to In-O oxides via reaction: $Sb_2O_3 + 2InSb \rightarrow In_2O_3 + 4Sb$ (because the Gibbs free energy of In_2O_3 is lower than that of Sb_2O_3: -198.6 kcal/mol as compared to -151.5 kcal/mol).[17] The reaction results in the increase of In-O bond as indicated in the Fig. 1(c), In $3d_{3/2}$ spectra. After annealing, almost Sb-O oxides changed to In-O oxides as indicated by the reduction of Sb-O signal to below the XPS detection level and a further increase of In-O signal (Fig. 1(d)).

The high-resolution transmission electron microscopy (HRTEM) image with the energy-dispersive X-ray spectroscopy (EDX) analysis is shown in Fig. 3. As shown in the figure, the total thickness of gate stack is ~4 nm, including 0.8 nm interfacial layer which is attributed to the out-diffusion of In, Sb into HfO_2 during thermal processes. For the Al_2O_3/InSb structure with very similar fabrication

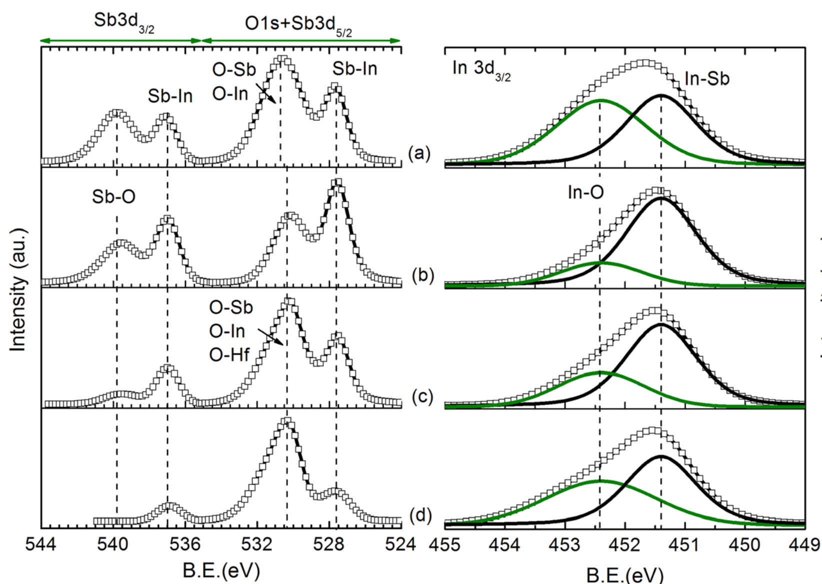


FIG. 2. In $3d_{5/2}$ and Sb 3d plus O1s XPS spectra of (a) native InSb surface, (b) as HCl treated InSb surface, (c) as deposited HfO_2/InSb interface, and (d) HfO_2/InSb interface after annealing at 250 °C, in N_2, for 30 s.

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Wed, 30 Apr 2014 08:49:25

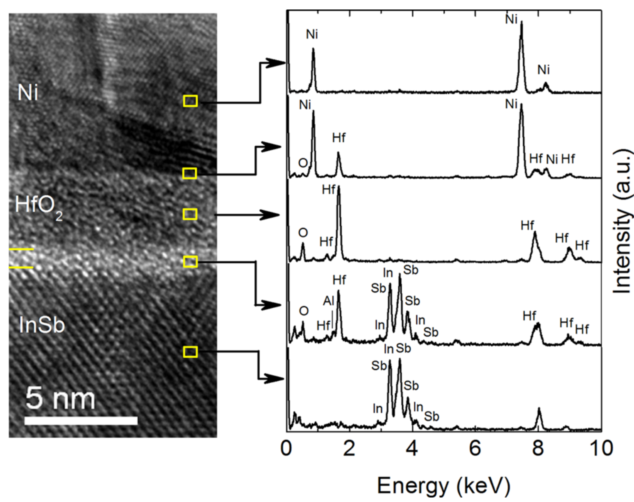


FIG. 3. HRTEM image with the EDX analysis of the sample.

process, a 1.5 nm-thick interfacial layer was observed.[9] This implies that HfO_2 would be a good diffusion barrier for InSb. The EDX spectra clearly indicate that the Sb, In signals are under detection level of EDX measurement in the HfO_2 bulk layer. Ni gate metal also did not diffuse into HfO_2 during the PMA step as indicated by EDX spectra in the figure.

Next, the electrical properties of the MOSCAPs are investigated. The multi-frequency capacitance-voltage (C-V) curves at different temperatures (77 K, 150 K, and 300 K) of the sample are shown in Figs. 4(a)–4(c). At room temperature (300 K), the sample exhibits low frequency C-V behavior in whole measured frequencies (1 MHz–1 kHz). This is attributed to the very short minor carrier response time τ_R in InSb which was discussed in previous reports.[9,10] Because of very short response time, minority carriers could response to high frequency ac signal and form an inversion layer when the gate voltage bias to negative side. From 300 K down to 77 K τ_R increases progressively, thus the C-V curves change gradually from the low frequency behavior at high temperature to the high frequency behavior at low temperature (77 K) and high frequency (100 kHz–1 MHz). This gradual changing indicates that Fermi level at HfO_2/InSb interface could move freely in the InSb bandgap. The unpinning Fermi level will be confirmed by using conduction map method as presented elsewhere. As shown in Fig. 4(a), the accumulation capacitance at room temperature can reach to 2900 pF/cm^2 at the gate voltage of 1.0 V. From that, the capacitance-equivalent-thickness (CET) is estimated directly from the relationship CET (V) = ($\kappa_{SiO2} \times \varepsilon_o$)/C(V) ($\kappa_{SiO2}$ is dielectric constant of SiO_2, ε_o is the permittivity of free space, and C(V) is measured capacitance) to be about 1.19 nm. The equivalent-oxide-thickness (EOT) value extracted by taking into account of quantum-mechanical correction is generally lower that CET value. The difference between CET and EOT for is about several angstrom (0.43–0.47 nm for HfO_2/InGaAs MOS structure).[18] From this point, the EOT value in this work is expected to be smaller than 1 nm. The current-voltage (J-V) characteristic of sample is shown in Fig. 4(d). The leakage current 10^{-4} A/cm^2 (at V_{FB} + 0.5 V) and breakdown field E_{BD} of 5.9 MV/cm are adequate for the future logic devices application.

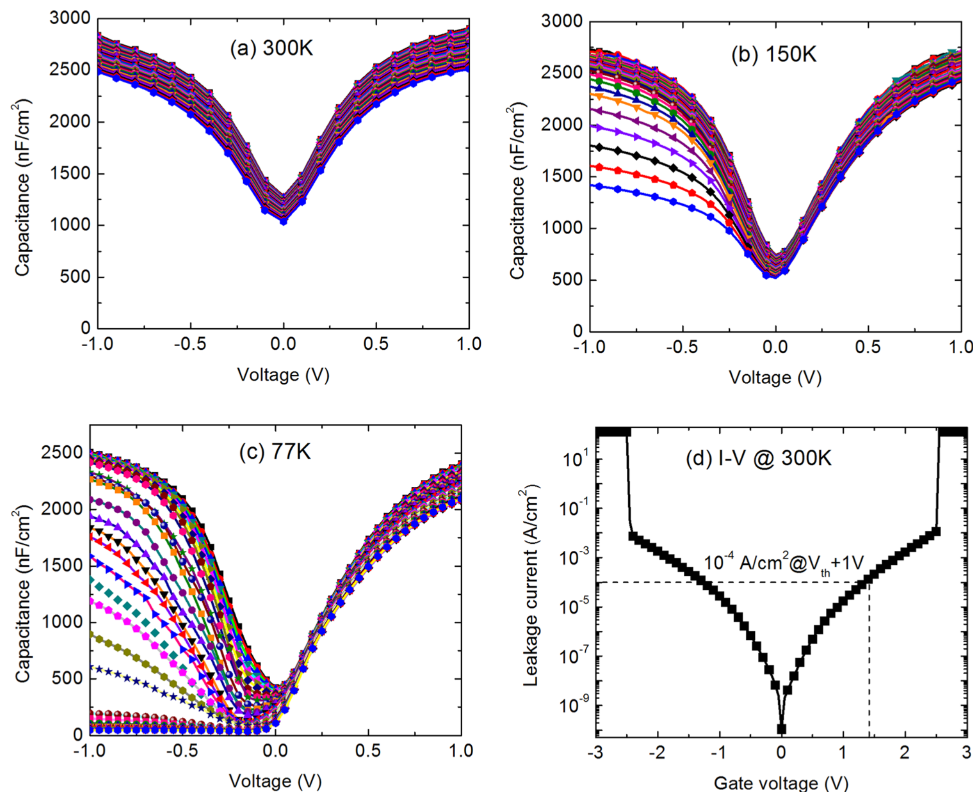


FIG. 4. Multi-frequency C-V characteristics of the sample at temperature of (a) 300 K, (b) 150 K, and (c) 77 K; (d) the leakage current-voltage characteristic of sample at 300 K.

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Wed, 30 Apr 2014 08:49:25

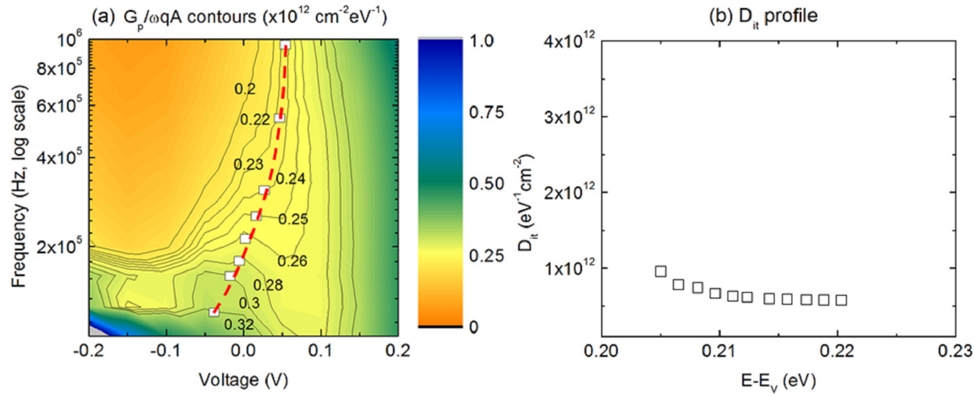


FIG. 5. (a) The normalized parallel conduction contour of the sample (77 K, 100 kHz–1 MHz) shows clearly the trace of free movement of Fermi level (red dash line); (b) the interface density of states distribution of the sample extracted by conduction method.

The conductance map method was applied to verify the interface density of states as well as the movement of Fermi level.[19–21] The normalized parallel conductance is determined from the measured impedance by[20,21]

$$\frac{G_p}{\omega qA} = \frac{1}{qA} \times \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}, \quad (2)$$

where A is area of the MOSCAP, $\omega = 2\pi f$ (f is frequency), q is the elementary charge, C_{ox} is the oxide capacitance, C_m is the measured capacitance, and G_m is the measured conductance. Because the conductance method is limited in the depletion region,[19] only the measured data at 77 K and frequencies in range of 100 kHz to 1 MHz were selected for verifying. Figure 5(a) shows the normalized conductance contour as a function gate voltage and frequency (100 kHz–1 MHz) of the sample at 77 K. From the figure, the conductance peak maximum can shift along with gate bias and frequency (dashed line), indicating that Fermi level could move freely inside InSb bandgap. The interface density of states, D_{it}, was extracted from the maximum of normalized parallel conduction by

$$D_{it} = 2.5 \times \left(\frac{G_p}{\omega qA}\right)_{\max}. \quad (3)$$

The trap levels E_T can be estimated from the trap response time $\tau_T = 1/f$ which is given by the Shockley–Read–Hall statistic[21,22]

$$\tau_T = \frac{1}{f} = \frac{1}{\sigma v_{th} N} \times \exp(\Delta E/kT), \quad (4)$$

$$\Rightarrow \Delta E = kT \ln\left(\frac{\sigma v_{th} N}{f}\right), \quad (5)$$

where $\Delta E = E_C - E_T$ is the energy different between trap level and majority carrier band edge energy (conduction band in this case), σ is the capture cross section of the trap ($\sigma = 10^{-16}$ cm^2 was taken in this work), v_{th} is average thermal carrier velocity, N is the effective density of state (DOS) in majority carrier band, k is the Boltzmann constant, and T is temperature. At temperature 77 K, the values of $v_{th} = 5 \times 10^7$ cm/s, $N = 5.4 \times 10^{15}$ cm^{-3}, and InSb bandgap of 0.23 eV were taken.[1] For the frequency in range of 100 kHz to 1 MHz, the traps with energy level from 0.01 to 0.025 eV below the InSb conduction band edge E_C (i.e., 0.22 to 0.205 eV above the InSb valence band edge E_V) would be extracted. The calculation also took into account the limitation of conductance method that the value of D_{it} is reasonable only if $C_{ox} > qD_{it}$. The D_{it} distribution as a function of trap energy levels of the sample is shown in Fig. 5(b). From the figure, the low D_{it} of 6×10^{11}–1×10^{12} $eV^{-1}cm{-}^{2}$ in the energy range of 0.22–0.205 eV above InSb valence band maximum has been obtained.

In conclusion, we have characterized the properties of the HfO_2/InSb MOS struture by using XPS, TEM, I-V, and C-V measurement. The band alignment of the HfO_2/InSb structure including conduction band offset of 1.78 ± 0.1 eV and valence band offset of 3.35 ± 0.1 eV has been deduced by XPS. The reduction of InSb native oxides via surface clean and thermal annealing steps has been verified. The TEM in conjuction with EDX analysis implied that HfO_2 could be a good diffusion barrier for InSb. With 4 nm gate oxide thickness, a 1 nm EOT in the HfO_2/InSb MOSCAPs has been demonstrated with low leakage current of 10^{-4} A/cm^2 at $V_{FB} + 0.5$ V. Unpinning Fermi level and the D_{it} value of smaller than 10^{12} $eV^{-1}cm^{-2}$ has been demostrated by C-V characteristics and conduction method. These good results would give a benefit for future realizing the InSb-based MOS devices application.

This work was supported by NCTU-UCB I-RiCE Program, Taiwan and Vietnam National Foundation for Science and Technology Development (Contract No. 103.02-2011.12).

[1]M. Levinshtein, S. Rumyantsev, and M. Shur, *Handbook Series on Semiconductor Parameters* (World Scientific, Singapore, 1996), Vol. 1.
[2]J. A. del Alamo, Nature **479**, 317–323 (2011).
[3]R. Chau, B. Doyle, S. Datta, J. Kavalieros, and K. Zhang, Nature Mater. **6**, 810–812 (2007).
[4]S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. Wallis, P. Wilding, and R. Chau, Tech. Dig. - Int. Electron Devices Meet. **2005**, 763.
[5]M. Radosavljevic, T. Ashley, A. Andreev, S. D. Coomber, G. Dewey, M. T. Emeny, M. Fearn, D. G. Hayes, K. P. Hilton, M. K. Hudait, R. Jefferies, T. Martin, R. Pillarisetty, W. Rachmady, T. Rakshit, S. J. Smith, M. J. Uren, D. J. Wallis, P. J. Wilding, and R. Chau, Tech. Dig. - Int. Electron Devices Meet. **2008**, 727.
[6]H. A. Nilsson, P. Caroff, C. Thelander, E. Lind, O. Karlstrom, and L.-E. Wernersson, Appl. Phys. Lett. **96**, 153505 (2010).

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Wed, 30 Apr 2014 08:49:25

[7]A. Pitanti, D. Coquillat, D. Ercolani, L. Sorba, F. Teppe, W. Knap, G. De Simoni, F. Beltram, A. Tredicucci, and M. S. Vitiello, Appl. Phys. Lett. **101**, 141103 (2012).
[8]A. C. Seabaugh and Z. Qin, Proc. IEEE **98**, 2095 (2010).
[9]H. D. Trinh, Y. C. Lin, E. Y. Chang, C. T. Lee, S. Y. Wang, H. Q. Nguyen, Y. S. Chiu, Q. H. Luc, H. C. Chang, C. H. Lin, S. Jang, and C. H. Diaz, IEEE Trans. Electron Devices **60**, 1555 (2013).
[10]H. D. Trinh, M. T. Nguyen, Y. C. Lin, Q. V. Duong, H. Q. Nguyen, and E. Y. Chang, Appl. Phys. Express **6**, 061202 (2013).
[11]J. Robertson and L. Lin, Appl. Phys. Lett. **99**, 222906 (2011).
[12]R. Suzuki, N. Taoka, M. Yokoyama, S. Lee, S. H. Kim, T. Hoshii, T. Yasuda, W. Jevasuwan, T. Maeda, O. Ichikawa, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi, Appl. Phys. Lett. **100**, 132906 (2012).
[13]H.-D. Trinh, E. Y. Chang, Y.-Y. Wong, C.-C. Yu, C.-Y. Chang, Y.-C. Lin, H.-Q. Nguyen, and B.-T. Tran, Jpn. J. Appl. Phys. Part 1 **49**, 111201 (2010).
[14]H. D. Trinh, G. Brammertz, E. Y. Chang, C. I. Kuo, C. Y. Lu, Y. C. Lin, H. Q. Nguyen, Y. Y. Wong, B. T. Tran, K. Kakushima, and H. Iwai, IEEE Electron Device Lett. **32**, 752–754 (2011).
[15]S.-H. Tang, E. Y. Chang, M. Hudait, J.-S. Maa, C.-W. Liu, G.-L. Luo, H.-D. Trinh, and Y.-H. Su, Appl. Phys. Lett. **98**, 161905 (2011).
[16]C. H. Hou, M. C. Chen, C. H. Chang, T. B. Wu, C. D. Chiang, and J. J. Luo, J. Electrochem. Soc. **155**, G180–G183 (2008).
[17]O. Salihoglu, A. Muti, K. Kutluer, T. Tansel, R. Turan, C. Kocabas, and A. Aydinli, J. Appl. Phys. **111**, 074509 (2012).
[18]T. D. Lin, Y. H. Chang, C. A. Lin, M. L. Huang, W. C. Lee, J. Kwo, and M. Hong, Appl. Phys. Lett. **100**, 172110 (2012).
[19]E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, 1982).
[20]G. Brammertz, H. C. Lin, K. Martens, D. Mercier, C. Merckling, J. Penaud, C. Adelmann, S. Sioncke, W. E. Wang, M. Caymax, M. Meuris, and M. Heyns, J. Electrochem. Soc. **155**, H945–H950 (2008).
[21]H. Q. Nguyen, H. D. Trinh, E. Y. Chang, C. T. Lee, S. Y. Wang, H. W. Yu, C. H. Hsu, and C. L. Nguyen, IEEE Trans. Electron Devices **60**, 235–240 (2013).
[22]W. Shockley and W. T. Read, Jr., Phys. Rev. **87**, 835 (1952).

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Wed, 30 Apr 2014 08:49:25