# The versatile designs and optimizations for cylindrical $TiO_2$-based scatterers for solar cell anti-reflection coatings

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**Abstract:** The anti-reflection coating(ARC) based on dielectric nano-particles has been recently proposed as a new way to achieve the low reflectance required for solar cell front surfaces. In this scenario, the Mie modes associated with the dielectric nano-particles are utilized to facilitate photon forward scattering. In this work, versatile designs together with systematically optimized geometry are examined, for the ARCs based on dielectric scatterers. It is found that the $Si_3N_4$-$TiO_2$ or $SiO_2$-$TiO_2$ stack is capable of providing low reflectance while maintaining a flat and passivated ARC-semiconductor interface which can be beneficial for reduced interface recombination and prevent $V_{OC}$ degradation associated with topography on the active materials. It is also confirmed that the plasmonic nano-particles placed at the front side of solar cells is not a preferred scheme, even with thorough geometrical optimization. At the ultimate design based on mixed graded index(GI) Mie-scattering, the averaged reflectance can be as low as 0.25%. Such a low reflectance is currently only achievable by ultra-long silicon nano-tips, but silicon nano-tips introduce severe surface recombination. On the other hand, the mixed GI Mie design preserves a flat and passivated ARC-silicon interface, with total thickness reduced to 279.8nm, much thinner than 1.6μm for silicon nanotips. In addition, the light trapping capability of mixed GI Mie design is much better than silicon nanotips. In fact, when compared to the state-of-art $TiO_2$ light trapping anti-reflection coating, the mixed GI Mie design provides same light trapping capability while providing much lower reflectance.



**OCIS codes:** (310.6845) Thin film devices and applications; (040.5350) Photovoltaic; (290.4020) Mie theory.

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## 1. Introduction

Recently, anti-reflection coatings (ARC) based on dielectric nano-particles have drawn considerable attention due to the potential to provide a new way for achieving anti-reflection for solar cell applications [1–4]. This includes $SiO_2$ spherical dielectric nano-particles [1], silicon-based Mie scatterers for ARC [2], the study on the void resonators [3], and comparison of different dielectric and metallic materials for the solar cell application [4]. The physics is that the nano-scaled dielectric scatterers initiate Mie modes and facilitate photon forward scattering and in-coupling into the semiconductor film [2, 3]. It has been shown that the mechanism is quite different from previously proposed anti-reflection coatings which either based on diffraction of periodic structures [5], or based on the so-called graded index approach [6, 7]. The dielectric-scatterer based ARCs can potentially have the advantage of no surface plasmonic (SP) absorption loss, compared to the SP nano-particles placed at the front side of solar cells. There are several important considerations for anti-reflection coating as far

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as solar cells is concerned. The very first one is certainly the low reflectance. The requirement of low reflectance is particularly important for the first generation wafer-based photovoltaics or multi-junction cells since most of the spectral photons can be absorbed within one or two photon passes and thus the transmittance into the cells pretty much determines the actual integrated absorbance ($A_{Int}$, defined later in Eq. (2)). The other constraint for ARCs is light trapping. This is more important for the second generation thin-film photovoltaics. In fact, the integrated absorbance is actually what determines the final photocurrent and thus for thin-film photovoltaics, integrated absorbance should be used to assess solar cell front surface coatings. The use of integrated absorbance to study solar cell optics is a very common practice [5, 8, 9] with potentially different names to indicate this quantity in different literatures. It can be regarded as the photocurrent assuming perfect charge collection. The third requirement for ARC is a flat and passivated ARC-active material interface to reduce surface/interface recombination. It will be explained in section 3 why this flat and passivated ARC-silicon interface is beneficial for both thin-film and wafer-based photovoltaics. Previously proposed ARC based on ultra-long silicon nano-tips can provide ultra-low reflectance, but it leads to severe surface recombination [7]. Finally, the thickness of ARC should be kept thin in order not to increase the total device thickness and also to make proposed ARC to be compatible with thin-film photovoltaics. The ARCs like long silicon nanotips are difficult to be used for thin-film since the thickness of ARC itself is already 1.6μm. In this work, the versatile design and systematic optimization by genetic algorithm (GA) is employed to investigate four new anti-reflection structures based on $TiO_2$ dielectric scatterers or dielectric wrapped surface plasmonic scatterers. By proper optimization of the geometrical parameters, the proposed ARC structures can possess combined advantageous features: It can achieve the low reflectance that is comparable to the lowest reflectance ARC to date [7], but without the drawbacks of elevated surface recombination, bulky dimension and poor light trapping. On the other hand, the light trapping capability of the proposed ARC structure here is comparable to the state of art light-trapping-anti-reflection coating [5], while providing a lower reflectance. The flat and passivated ARC-silicon interface are maintained for all of the proposed Mie scattering ARCs in this study which is expected to reduce surface/interface recombination, beneficial for higher $V_{OC}$ and $J_{SC}$.

## 2. Calculation set-up for cylindrical Mie scattering ARC

The first Mie scattering structure consists of $Si_3N_4$-$TiO_2$ or $SiO_2$-$TiO_2$ complex. Silicon scatterers have also been proposed for anti-reflection coating [2] but the silicon scatterers themselves still absorbs part of the sunlight while there is no guarantee that the electron-hole pair generated in the silicon scatterer region can be properly collected. This point will be discussed further in section 3. Using dielectric, such as $TiO_2$, as the anti-reflection coating can eliminate this problem. Besides, using the dielectric as the ARC also lead to the advantage of flat ARC-silicon interface and thus a reduced interface recombination rate [5]. In fact, the flat geometry is also more preferable as far as open circuit voltage ($V_{OC}$) is concerned. It has been shown that etching the active silicon material or depositing the silicon thin-film on grooved substrates can lead to significant $V_{OC}$ reduction [10–12]. Besides, the reduced interface recombination itself can also help to achieve higher $V_{OC}$ and $J_{SC}$.

The second structure under investigate is a surface plasmonic (SP) Mie scattering structure. Abundant literature has been devoted to the structures where the metallic SP particles are placed at the front side of solar cells [13–17]. Nonetheless, by systematic optimization, it is shown here that the metallic absorption associated with the metallic particles is difficult to be reduced to the point where the transmittance of SP scattering ARCs are comparable to dielectric-based ones. This observation also holds for optimized geometry with dielectric spacer($TiO_2$). Even with dielectric wrapping around silver nano-particles, the metallic absorption still deteriorate the transmittance significantly.

The third structures is a mixed graded index (GI) Mie scattering ARC. The main advantage of this structure is that it provides ultra-low reflectance. The low reflectance by GI Mie ARC can only be achieved previously by ultra-long silicon nano-tips ARC [7]. While the

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long silicon nano-tips introduces severe surface recombination leading to significantly reduced $V_{OC}$ and $J_{SC}$, the GI Mie ARC still maintains a flat and passivated ARC-silicon interface. In addition, the total thickness of GI Mie ARC is only 279.8nm after optimization, much thinner than the required length for silicon nano-tip ARC which is around 1.6μm for the solar cell application. Besides, the light trapping capability of the Mixed GI Mie ARC is much better than silicon nano-tips. Actually, the light trapping capability of mixed GI Mie ARC is comparable to the state-of-art light trapping anti-reflection coating [5] while the mixed GI Mie ARC provides much lower reflectance.

The fourth ARC structure is a sidewall free(SWF) version of dielectric scatterer ARC where the topmost $Si_3N_4$ or $SiO_2$ coverage is removed while the ARC can still maintain satisfactory low reflectance and light trapping property after optimization. The removal of the topmost dielectric can eliminate the need to control the sidewall or step coverage property during deposition process [2]. Although in experiment it has been shown that the control of sidewall coverage profile is achievable [2], the sidewall free version reduces the fabrication complexity for dielectric scatterer ARCs.

The material parameters are from Rsoft material database [18] and the refractive index of porous silicon dioxide($SiO_2$) is 1.07 [6]. For the reflectance calculation in sections 3, 4, 5, and 6, crystalline silicon parameter is used since it is more related to wafer-based solar cells and also consistent with [2, 6, 7]. For the absorbance calculation in sections 5 and 6, crystalline silicon(c-Si) from Rsoft material database [18] and microcrystalline silicon (μc-Si) from SOPRA material database have been used for calculation. The conclusion is the same where in both cases dielectric Mie scatterer ARCs can provide decent light trapping comparable to the state-of-art light-trapping anti-reflection coating [5]. Amorphous silicon (α-Si) is not chosen here due to its much higher absorption coefficient. This makes the light trapping effect of α-Si less pronounced compared to c-Si or μc-Si unless the silicon thickness is further reduced. In order to study the effect of light trapping and to have unified material parameters in this study, the absorbance result for c-Si is included in this paper. It should be emphasized that the proposed dielectric scatterer ARCs not only work for silicon of different phases, they can also provide low reflectance and light trapping for other inorganic semiconductors as well. This is due to the similar mode coupling, light trapping, and waveguiding behaviors in inorganic solar cells. One example is that the TiO2 nanotips [5] are originally proposed based on simulation with silicon solar cells but later it can be applied to III-V solar cells equally well [19]. As a result, which inorganic semiconductor is used as an example to demonstrate the effectiveness of dielectric scatter ARCs is not critical. The calculation method is based on rigorously coupled wave anaylsis (RCWA) implemented by Rsoft Diffractmode. The polarization angle is 45° and therefore the result is the average of s- and p-polarization. In fact, the calculation results are exactly the same for s-, p-, or 45° polarization since the structure is rotationally symmetric. Therefore, in field plots the polarization is taken to be s-polarization. The field profiles for p-polarization are the same as s-polarization except the profiles are rotated 90°.

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### 3. $TiO_2$-$Si_3N_4$ or $TiO_2$-$SiO_2$ cylindrical dielectric scatterer ARC

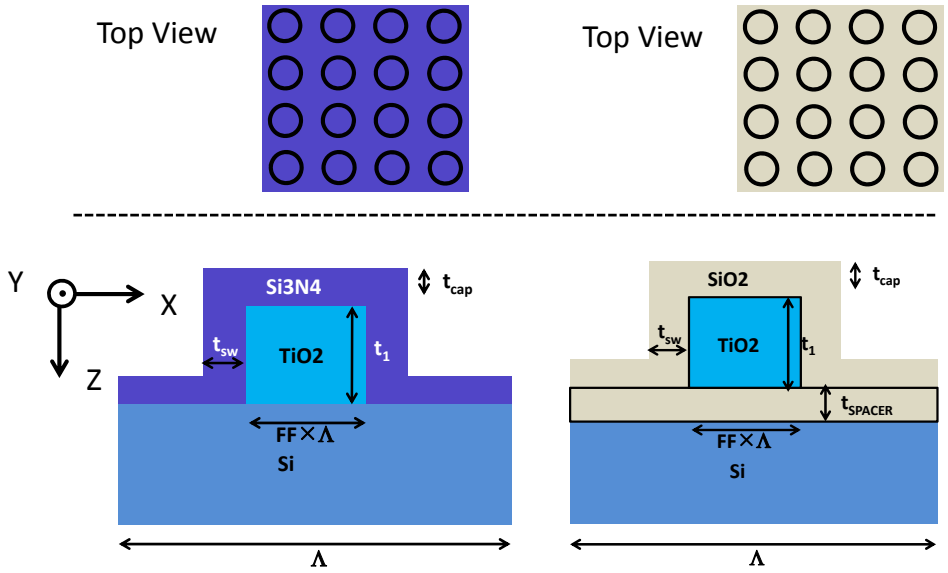


Fig. 1. The cross-section and the topview of the cylindrical dielectric scatterer anti-reflection coating. The geometrical parameters under global optimization is labeled in the cross sectional view. (Left) Cylindrical $TiO_2$ scatterers with $Si_3N_4$ wrapping. (Right) Cylindrical $TiO_2$ scatterers with $SiO_2$ wrapping.

The geometry is illustrated in Fig. 1. The structure can be $TiO_2$ scatterers with $Si_3N_4$ wrapping or $TiO_2$ scatterers with $SiO_2$ wrapping. The inclusion of a $SiO_2$ dielectric spacer between $TiO_2$ and Si, in the structure on the right hand side of Fig. 1, can further reduce the interface recombination by the low defect interface between $SiO_2$-Si. The optimized geometry by genetic algorithm is $\Lambda = 0.44$ μm, FF = 0.6039, $t_1 = 0.1214$μm, $t_{cap} = 0.056$ μm, $t_{sw} = 0.02$ μm for $TiO_2$-$Si_3N_4$ complex ARC, and $\Lambda = 0.397$ μm, FF = 0.6394, $t_1 = 0.102$μm, $t_{cap} = 0.066$μm, $t_{sw} = 0.0177$ μm, $t_{SPACER} = 10$ nm for $TiO_2$-$SiO_2$ complex ARC. For comparison, the geometry for silicon Mie scatterers from [2] is $\Lambda = 0.45$ μm, FF = 0.2778, $t_1 = 0.15$μm, $t_{cap} = 0.05$μm, $t_{sw} = 0.075$μm. The sidewall thickness, $t_{sw}$, of the silicon scatterer ARC [2] is critical for low reflectance, which can be verified by optics simulation and comparing to the measured results in [2]. The averaged reflectance is 0.76% for $TiO_2$-$Si_3N_4$ complex ARC, and 1.13% for $TiO_2$-$SiO_2$ complex ARC, and 1.87% for Si scatterer ARC [2]. The structure in reference [2] consists of silicon scatterers and a $Si_3N_4$ conformal coverage. The cylindrical silicon scatterers can be formed by depositing silicon thin-film on grated substrates or by etching the silicon material. The former method is mostly found in thin-film photovoltaics [10, 20–27] while the later method is more common in wafer-based photovoltaics [2, 28]. The potential problem with the silicon Mie-scatterers is that silicon scatterers still absorb some of the incoming sunlight, and the electron-hole pair generated in the grating region may not be collected depending on the device structures. For wafer-based silicon solar cells, the highly doped $n^+$ and p + emitters only exist in the selected regions at the front or back side of wafers depending on device design. Therefore, the e-h pairs can recombine before being collected if they are generated inside the Si Mie scatterers where interface recombination is more pronounced. For thin-film silicon solar cells, the conformal p-i-n layers are deposited sequentially, and the junction can indeed exist inside the Si scatterers, i.e. the grating region. Nonetheless, it has been shown that depositing silicon thin-film on a grated or grooved substrate leads to significant $V_{OC}$ reduction [10]. In the case of $TiO_2$-$SiO_2$, the flat silicon-ARC interface together with decent interface property between thermally grown $SiO_2$ and Si ensure very low interface recombination.

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In the spectral response of Fig. 2, it can be found that through geometry optimization, the reflectance can be very effectively reduced based on the proposed $TiO_2$ cylindrical scatterer schemes. While $SiO_2$ and $Si_3N_4$ are common dielectrics for surface passivation, it is expected that the proposed $TiO_2$-$Si_3N_4$ or $TiO_2$-$SiO_2$ structure can achieve low surface recombination. In the second structure on the right side of Fig. 1, the planar Si-$SiO_2$ interface can especially ensure the surface passivation. The field profiles on the right of Fig. 2 confirm the excitation of weakly confined resonator modes inside the cylindrical $TiO_2$ Mie scatterers. For the case of $Si_3N_4$ wrapping, the weak confinement is due to the wrapping is only partial, not including the bottom side of $TiO_2$ scatterers. For the case of $SiO_2$ wrapping, the bottom $SiO_2$ spacer is usually thin after optimization, and therefore the confinement is still weak. The bottom side of the cylindrical $TiO_2$ scatterers should act as resonator openings for the incident power to be coupled into the silicon thin film, and that is the reason why the $SiO_2$ dielectric spacer thickness is always thin after optimization.

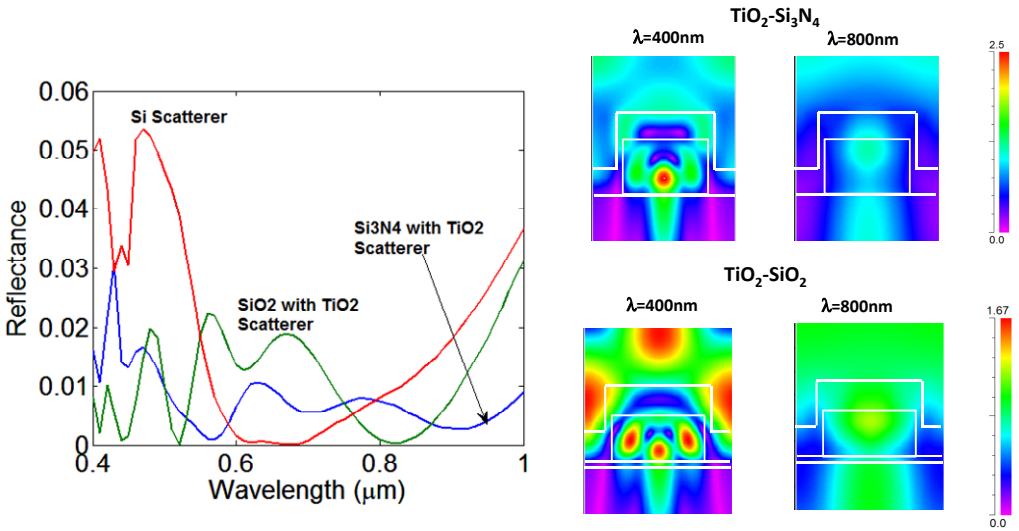


Fig. 2. (Left) the spectral reflectance for $TiO_2$-$Si_3N_4$ and $TiO_2$-$SiO_2$ dielectric scatterer ARC. (Right) the corresponding field profiles $E_y$ at y = 0 for λ = 400nm and λ = 800nm.

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## 4. Surface plamonic (SP) assisted cylindrical dielectric scatterer ARC

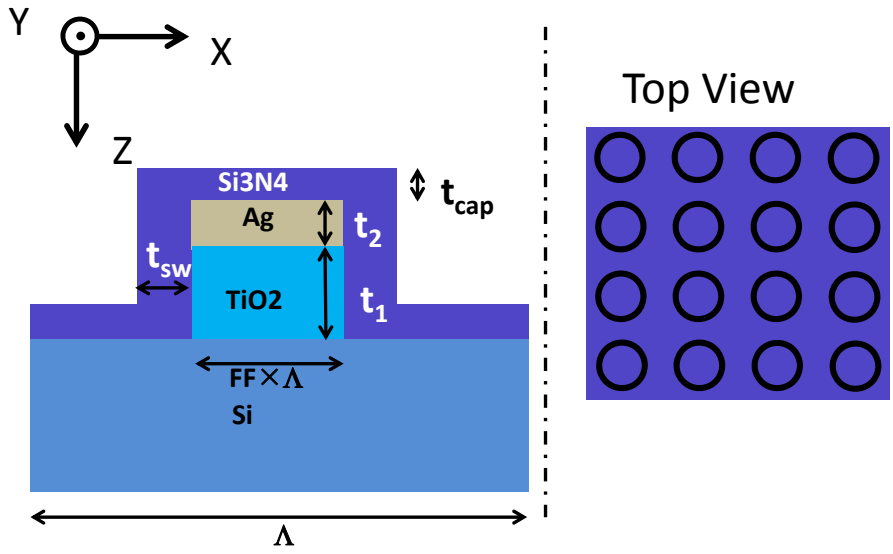


Fig. 3. The cross-section and the topview of the cylindrical surface plasmonic (SP) assisted dielectric scatterer anti-reflection coating. The geometrical parameters under global optimization is labeled in the cross sectional view.

The surface plasmonic nano-particles have been proposed to be placed at the front side of solar cells to enhance photon forward scattering [13–17]. Here the cylindrical scatterers consist of silver-$TiO_2$ complex, as illustrated in Fig. 3, is studied and globally optimized by genetic algorithm. The optimized geometry is $\Lambda$ = 0.64μm, FF = 0.3417, $t_1$ = 0.1986μm, $t_2$ = 20nm, $t_{cap}$ = 0.0611μm, $t_{sw}$ = 0.0258μm. The averaged transmittance ($T_{avg}$) is 91.35% and thus 1-$T_{avg}$ is 8.65%, to compare with the dielectric ARCs. It should be pointed out that for dielectric ARC, T = 1-R, where T is the transmittance and R is the reflectance. Therefore, plotting the transmittance or reflectance does not matter. Nonetheless, since the metallic absorption (Abs) exists for SP ARC, the transmittance should be plotted, and T = 1-R-Abs. Here in order to compare to the reflectance of dielectric ARCs, 1-T of the SP ARC is also plotted, which is the power that is lost and can be regarded as the equivalent of the reflected power in the case of all-dielectric ARCs. During the optimization, the thickness of Ag is always converging to the lower limit (20nm) in the genetic algorithm set-up, reflecting the dominant and detrimental effect of the metallic absorption by Ag scatterers. The original purpose of genetic algorithm is to achieve a balance between photon forward scattering and surface plasmonic loss, but the effect of metallic absorption is too pronounced leading to the situation where the Ag thickness is kept reduced in order to maximize transmitted power into silicon.

From Fig. 4, it is clear that it is quite difficult for the surface plasmonic ARC to compete with dielectric ARC due to the metallic absorption, even with thorough geometry optimization. The dielectric wrapping in the case here is the top $Si_3N_4$ coverage and the bottom $TiO_2$ below silver nano-paritlces. The dielectric wrapping can reduce the metallic absorption since the number of photons actually reaching silver particles will be reduced. Here the dimension of the dielectric wrapping is actually optimized by GA. Nonetheless, even at the optimized layer thickness, the transmittance is still lower than the dielectric ARCs. In the right of Fig. 4, the field profiles are plotted. It is evident that SP modes are excited by noticing the field intensity at the dielectric-silver interface. The significant field intensity at the dielectric-silver interface results in absorption loss. As a result, while SP photovoltaics is

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promising for many purposes, such as the light trapping by SP back reflector, field condensation, and energy transfer, the application SP nano-particles for ARCs is less preferable even with globally optimized geometry.

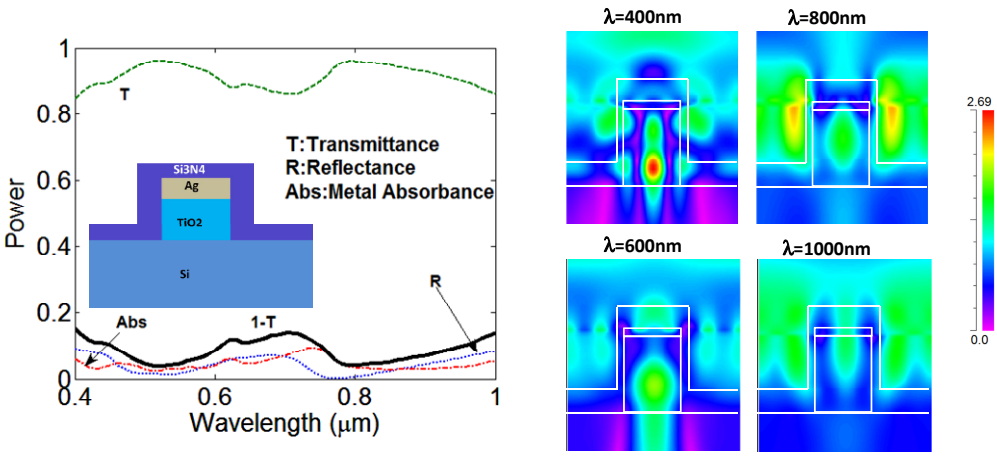


Fig. 4. (Left) the spectral transmittance(T), reflectance(R), and metal absorbance(Abs) for the surface plasmonic assisted dielectric scatterer anti-reflection coating. (Right) the corresponding field profiles $E_y$ at y = 0, for λ = 400nm,λ = 600nm, λ = 800nm, and λ = 1000nm.

## 5. Cylindrical mixed graded-index(GI) Mie scattering ARC

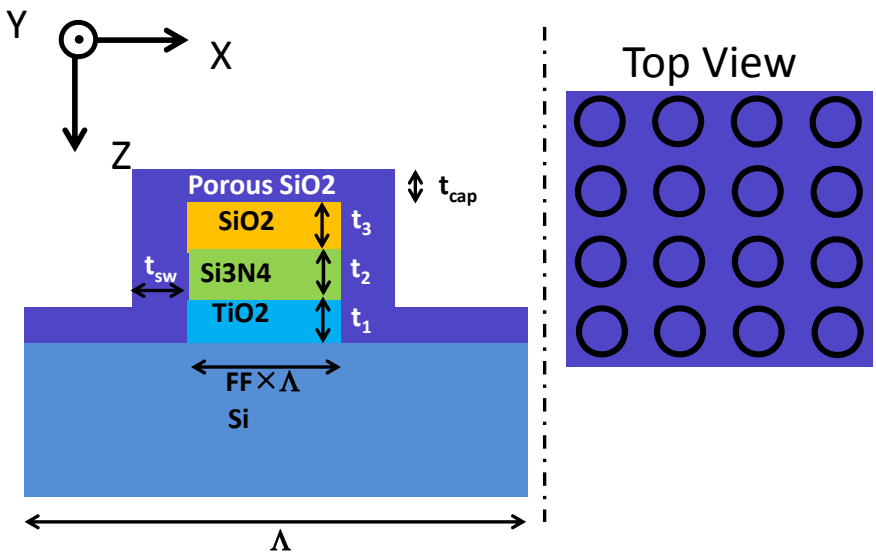


Fig. 5. The cross-section and the topview of the cylindrical mixed graded index(GI) Mie scattering anti-reflection coating. The geometrical parameters under global optimization is labeled in the cross sectional view. This structure will be abbreviated as mixed GI Mie ARC below.

It is desirable to further decrease the reflectance of a dielectric scatterer ARC. Currently, the ARC with the lowest reflectance is the ultra-long silicon nanotips [7]. Nonetheless, silicon nanotips suffer from the drawbacks of no passivation, high surface recombination, bulky dimension, and poor charge collection for the carriers generated inside the nanotip region. Figure 5 illustrates the structure for proposed mixed graded index Mie scattering ARC

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(abbreviated mixed GI Mie ARC below). The refractive index of porous $SiO_2$ is assumed to be 1.07 [6]. For minimized averaged reflectance ($R_{avg}$), the optimized geometry by GA is $\Lambda$ = 0.3969μm, FF = 0.7622, $t_1$ = 0.113μm, $t_2$ = 0.029μm, $t_3$ = 0.0625μm, $t_{cap}$ = 0.0739μm, $t_{sw}$ = 2.73nm. The averaged reflectance is 0.25%. The averaged reflectance achieved here is comparable to the silicon-nano tips [7], which is the lowest reflectance ARC to date. Nonetheless, the mixed GI Mie scattering ARC does not suffer from interface or surface recombination due to the all-dielectric nature and its passivated surface. The total thickness of the mixed GI Mie scattering ARC is also significantly reduced, which is only 279.8nm compared to 1.6 μm for the silicon nano-tips. In addition, while the silicon nanotips provides mediocre light trapping property which will be clear later in Table 1, the light trapping capability of the mixed GI Mie scattering ARC is actually comparable to the state-of-art light trapping anti-reflection coating which is based on $TiO_2$ nanotips [5]. Furthermore, it is worth to point out that the averaged reflectance of mixed GI Mie scattering ARC is much lower than $TiO_2$ naontips in reference [5]. The dimension for $TiO_2$ nanotips [5] is P = 0.6μm, the dimension for the silicon nanotips [7] are L = 1.6μm and P = 0.2μm, and the dimension for the planar multi-layer ARC is from [6].

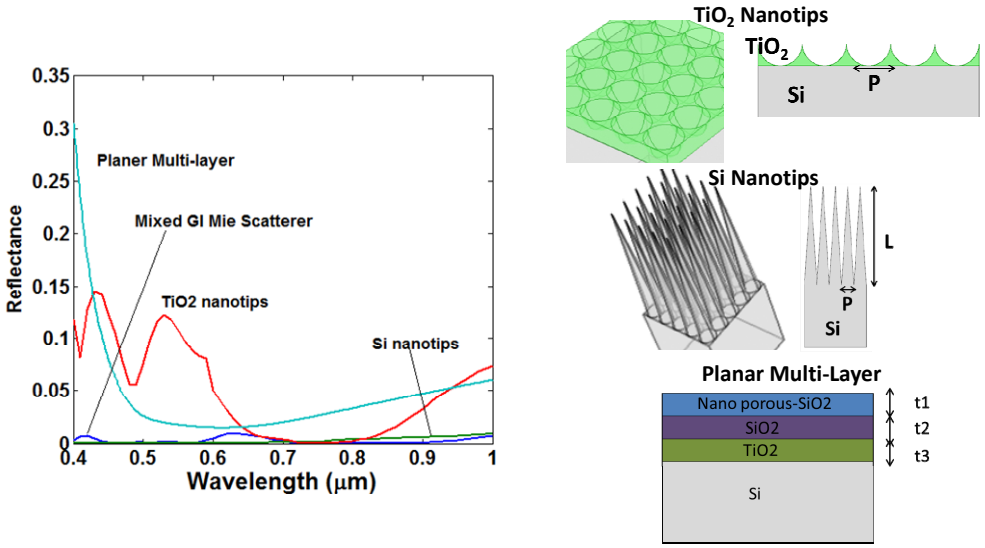


Fig. 6. Comparison of mixed graded index Mie scattering anti-reflection coating with ultra-low reflectance silicon nano-tip ARC in reference [7] and the state-of-art light trapping anti-reflection $TiO_2$ coating in [5]. The dimension for $TiO_2$ nanotip ARC [5] is P = 0.6μm, the dimension for the silicon nanotip ARC [7] is L = 1.6μm and P = 0.2μm, and the dimension for the planar multi-layer ARC is from [6].

The light trapping property is also crucial in addition to the anti-reflection property as far as the solar cell front surface coating is concerned. For thin-film solar cells, integrated absorbance weighted by AM1.5 spectrum (Eq. (2)) is more important than the low reflectance. In order to compare the light trapping property of different surface coatings, a 0.3μm silicon and a silver back reflector is added to the ARC and the integrated absorbance is calculated for the above-mentioned structures in Fig. 6. Before comparing the light trapping property of different surface coatings, it is important to point out that in this work, the structure for the absorbance calculation (in Table 1) is ARC + 0.3μmSi + Ag, while the structure for the reflectance or transmittance calculation (in Fig. 2, Fig. 4, Fig. 6, and Fig. 9) is ARC + 0.3μmSi + perfectly matched layer (PML). This is illustrated in Fig. 7. It should be emphasized that the silicon thickness is kept much thinner than what is required for full absorption in order to compare the light trapping capability of different front surface coatings. It is actually a very common practice to include only the front surface texture when comparing the effectiveness of anti-reflection characteristics [2, 5–7]. If the geometry is

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optimized for integrated absorbance ($A_{Int}$) instead, $\Lambda$ = 0.3535μm, FF = 0.7858, $t_1$ = 0.1915μm, $t_2$ = 0.0838μm, $t_3$ = 0.133μm, $t_{cap}$ = 0.1107μm, $t_{sw}$ = 1.53nm. For $TiO_2$ nanotips [5] geometry optimized for integrated absorbance, $A_{Int}$, P = 0.745μm.

The absorbance is calculated by integrating the power dissipation in silicon:

$$A(\lambda) = \frac{\frac{1}{2}\int_V \omega\varepsilon_0\varepsilon''(\lambda)\left|\vec{E}(\vec{r})\right|^2 dv}{\frac{1}{2}\int_S \mathrm{Re}\left\{\vec{E}(\vec{r})\times\vec{H}^*(\vec{r})\right\}\cdot d\vec{s}}. \quad (1)$$

where $\omega$ is the angular frequency, $\lambda$ is the free space wavelength, $\varepsilon_0$ is the permittivity in vacuum, and $\varepsilon''$ is the imaginary part of the complex semiconductor dielectric constant. The normalized integrated absorbance can be defined to compare different ARCs. This is needed since the active silicon material volume might be different for various ARCs. In fact, in Table 1 only the silicon nano-tip ARC possesses a different active material volume, while other ARCs are all dielectric-based so the active silicon volume is all the same. The normalized integrated absorbance, $A_{Int}$, is defined as

$$A_{Int} = \frac{V_{Si,Ref}}{V_{Si}} \frac{\int \frac{\lambda}{hc}\Omega(\lambda)A(\lambda)d\lambda}{\int \frac{\lambda}{hc}\Omega(\lambda)d\lambda}. \quad (2)$$

where $V_{Si,Ref}$ is the silicon volume of one period(P) in the case of a planar reference cell with no front surface texture or coating. In this study the silicon thickness is taken to be 0.3μm and thus $V_{Si,Ref}$ = P×P×0.3μm. $V_{Si}$ is the silicon volume of one period for the solar cell structure with a specific front surface coating. For dielectric coatings, the active silicon volume is the same as the planer reference cell. $\Omega(\lambda)$ is the AM 1.5 solar spectrum in unit of J $s^{-1}cm^{-2}$ $nm^{-1}$, $h$ is the Plank constant, $\lambda$ is the free space wavelength and $c$ is the speed of light. The details for calculating the absorbance can be found in [29–31]. The use of integrated absorbance to study solar cell optics is a very common practice [5, 8, 9] with potentially different names to indicate this quantity in different literatures. It can be regarded as the photocurrent assuming perfect charge collection.

Table 1 compares the averaged reflectance ($R_{avg}$) and the integrated absorbance ($A_{Int}$) for different ARCs. In the first row of Table 1, the geometry is optimized for achieving low reflectance so the resulting coating is for wafer-based photovoltaics or multi-junction cells where photons can be fully absorbed within one or two photon passes. The second row is more likely for thin-film photovoltaics and the geometry of ARC is optimized with respect to maximized integrated absorbance weighted by AM 1.5 spectrum, as defined in Eq. (2). It can be found that the averaged reflectance is roughly the same for the silicon nanotips and the mixed GI Mie ARC, while mixed GI Mie ARC provides lower interface recombination, reduced thickness with all-dielectric nature, and better light trapping. If the geometry is optimized for maximizing the integrated absorbance, i.e. optimized for thin-film photovoltaics, the light trapping property of the mixed GI Mie ARC is comparable to the state-of-art $TiO_2$ nanotips ARC [5]. Nonetheless, the $TiO_2$ nano-tip ARC is difficult to be tailored to provide low reflectance, evident from the first row of Table 1, even after geometry optimization. The difficulty to attain low reflectance for $TiO_2$ nanotips ARC [5] is due to the existence of a heterogeneous interface between $TiO_2$ and Si so the perfect index grading is broken.

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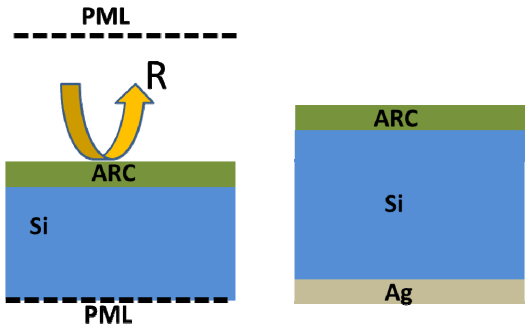


Fig. 7. (Left) the simulation structure for calculating the reflectance of anti-reflection coatings for Fig. 2, Fig. 4, Fig. 6, and Fig. 9 and the $R_{avg}$ in Table 1. (Right) the simulation structure for calculating the integrated absorbance weight by AM1.5 spectrum, $A_{Int}$, in Table 1.

**Table 1. Comparison of different anti-reflection coatings at their respective optimized geometry**

| ARC Type | Planer Multi-Layer | Silicon Nano-tips | $TiO_2$ Nano-tips | Mixed GI Mie Scatterer |
|---|---|---|---|---|
| **$R_{avg}$** | **4.39%** | **0.25%** | **4.85%** | **0.25%** |
| $A_{Int}$ | 0.1189 | 0.1783 | 0.3817 | 0.3293 |

| ARC Type | $TiO_2$ Nano-tips (Geometry optimized for thin-film photovoltaics) | Mixed GI Mie Scatterer (Geometry optimized for thin-film photovoltaics) |
|---|---|---|
| $R_{avg}$ | - | - |
| **$A_{Int}$** | **0.4014** | **0.4103** |

## 6. Sidewall free (SWF) cylindrical Mie scattering ARC

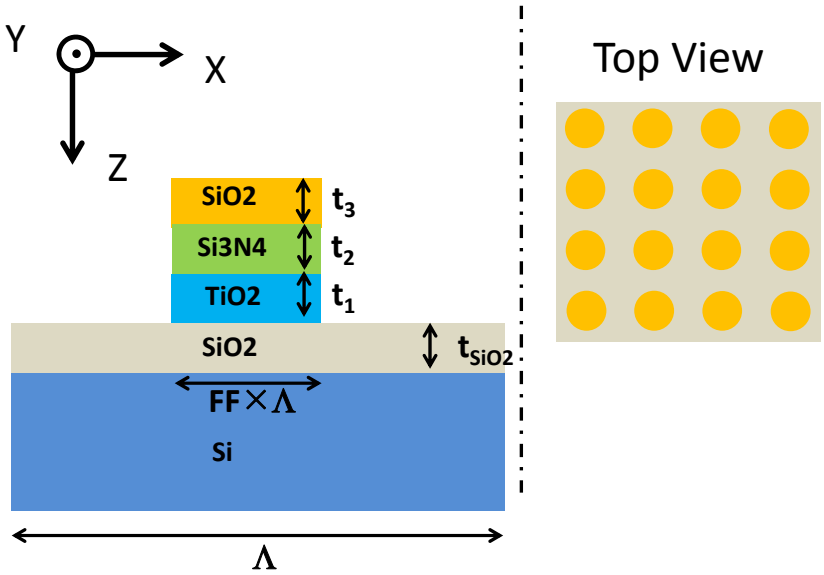


Fig. 8. The cross-sectional and topview of the sidewall-free (SWF) Mie scattering anti-reflection coating and the geometrical parameters under global optimization.

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The above mentioned geometries for various dielectric or surface plasmon (SP) scatterer based ARCs are all practical since the dimensions are all fabricable by common lithography methods. The well-defined geometry guarantees that the low reflectance can be realized in experiments, as in the case of silicon scatterers [2]. The only geometrical parameter that is a little more subtle to control is the sidewall thickness, which is mostly related to the step-coverage property of a specific deposition method. Nonetheless, with the fact that the silicon scatterers [2] have been successfully realized while its low reflectance is affected by its sidewall coverage, it is believed that by adjusting process conditions or by proper selection of deposition methods, the desired step coverage can be achieved.

For the completeness of this work, a sidewall-free version of cylindrical Mie scattering ARC is provided as illustrated in Fig. 8, while the result also shows decent anti-reflection and light trapping property, despite the fact there is no topmost dielectric wrapping. The sidewall-free ARC will eliminate the need for the selection of proper deposition methods in process. For minimized averaged reflectance ($R_{avg}$), the optimized geometry is $\Lambda$ = 0.396μm, FF = 0.7669, $t_1$ = 0.0965μm, $t_2$ = 0.0214μm, $t_3$ = 0.0667μm, $t_{SiO2}$ = 0.01μm. The spectral reflectance is illustrated in Fig. 9 and the averaged reflectance is 0.64%. Alternatively, if the geometry is optimized to maximize integrated absorbance($A_{Int}$) for thin-film photovoltaics using the structure of ARC + 0.3μmSi + Ag as illustrated on the right of Fig. 7, the optimized geometry is $\Lambda$ = 0.436μm, FF = 0.6913, $t_1$ = 0.19μm, $t_2$ = 0.0923μm, $t_3$ = 0.1348μm, $t_{SiO2}$ = 0.01μm, and the integrated absorbance($A_{Int}$), is 0.3836. Notice in this structure a flat and fully passivated $SiO_2$-Si interface is still achieved, which can ensure very low surface recombination. The inclusion of $SiO_2$ layer just above silicon is actually difficult since this breaks the arrangement of the gradual index change. The $SiO_2$-$Si_3N_4$-$TiO_2$ is originally index-grading arrangement while the addition of $SiO_2$ layer between $TiO_2$ and Si breaks the index grading. Nevertheless, without this $SiO_2$ passivation layer, severe surface recombination will be resulted due to the exposed silicon surface, similar to the case of silicon nano-tips [7]. As a result, the optimization using genetic algorithm to adjust the geometrical parameters is essential, and it is found that the $SiO_2$ passivation layer should be thin enough, in order to minimize the effect of broken index grading. In the case of thin $SiO_2$ passivation, the effect of diffraction will outperform the sequential index grading and the low reflectance can still be maintained. It can be seen that the optimized geometry for $R_{avg}$ and $A_{Int}$ does not differ significantly. This is due to the fact that in dielectric scatterer ARCs, resonator modes are beneficial not only for facilitating photon forward scattering, but also for coupling into the waveguide modes in the case of absorbance calculation where a silver back reflector exists. In contrast, for the silicon nanotip ARC [7], the low reflectance is due to the gradual change of effective index. Therefore, the silicon nanotip ARC [7] cannot improve the waveguiding for the absorbance calculation since there is no mode coupling exists. This is evident from Table 1.

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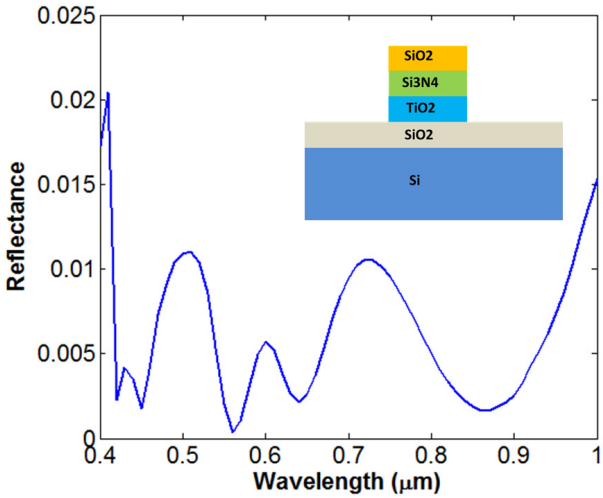


Fig. 9. The spectral reflectance of the sidewall-free cylindrical Mie scattering ARC at its optimal geometry.

## 7. Conclusion

The genetic algorithm is utilized to achieve four versatile designs using dielectric scatterers or surface plasmon assisted dielectric scatterers for solar cell anti-reflection coatings. The flat and passivated ARC-semiconductor interface is always maintained by all of the designs proposed in this work, which can ensure low surface/interface recombination and efficient charge collection. For the ultimate version of mixed graded index (GI) Mie scattering ARC, it possesses the combined advantage of low reflectance and efficient light trapping. The reflectance of mixed GI Mie ARC is comparable to the silicon nano-tip ARC, which is the lowest reflectance ARC to date. Nonetheless, the silicon nano-tip ARC suffers from severe surface recombination, ultra-long dimension, poor charge collection, and mediocre light trapping property, while mixed GI Mie ARC does not. The total thickness of mixed GI Mie ARC is 279.8nm after optimization compared to 1.6 μm for the silicon nano-tip ARC. The light trapping capability of the mixed GI Mie scattering ARC is far superior to silicon nano-tips, and in fact it is comparable to the state-of-art light-trapping-anti-reflection coating based on $TiO_2$ nanotips [5]. While the $TiO_2$ nanotips in [5] suffer from higher reflectance due to the existence of a heterogeneous interface between Si and $TiO_2$, mixed GI Mie ARC possesses ultra-low reflectance with the help of coupling into Mie modes. It is also found that there exists difficulty for the surface plasmonic ARCs to compete with dielectric ones due to the metallic absorption. This is true even with thorough geometry optimization and the dielectric wrapping around the silver nano-particles. A sidewall free (SWF) Mie scattering ARC is proposed at the end, to reduce the fabrication complexity. At the optimized geometry, the sidewall-free dielectric scatterers can still provide decent light trapping and anti-reflection, even without the topmost $SiO_2$ or $Si_3N_4$ wrapping.

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