Bidirectional Current Sensorless Control for the Full-Bridge AC/DC Converter With Considering Both Inductor Resistance and Conduction Voltages

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***Abstract*—The full-bridge converter is often connected between the ac grid and the dc bus. In the conventional multiloop control, the inner current control loop shapes the ac-side current waveform, and the outer voltage control loop regulates the dc-bus voltage. In this paper, the single-loop bidirectional current sensorless control (BCSC) for the full-bridge ac/dc converter with considering both the inductor resistance and conduction voltage is first proposed. The average-value behavior of the full-bridge ac/dc converter is analyzed and it is simplified to an equivalent single-switch model. Based on this developed equivalent model, BCSC is designed and implemented in the FPGA-based system. There is only voltage control loop in the proposed BCSC (i.e., no current control loop), but BCSC is able to regulate the dc-bus voltage and shape the ac-side current. The provided results in both the rectifier operation and the inverter operation demonstrate the effectiveness of the proposed BCSC.**

***Index Terms*—Current sensorless control, full-bride converter.**

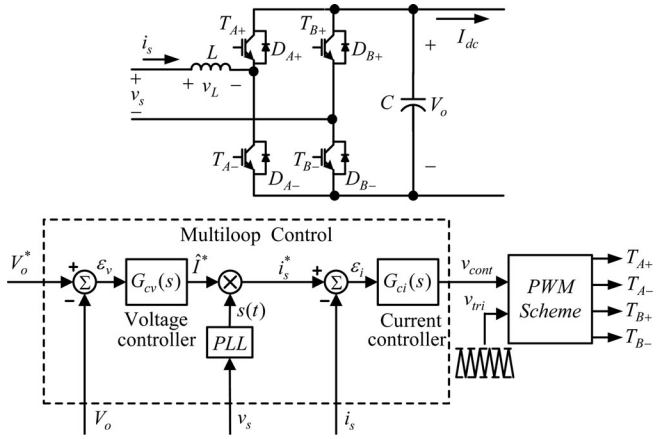

Fig. 1. Full-bridge ac/dc converter with the conventional multiloop control.

I. Introduction

THE four-switch full-bridge converter is a basic circuit topology in the power electronics due to its bidirectional ability in both the dc/dc conversion and the ac/dc conversion. In the past years, the pulse-width-modulation (PWM) rectifiers had been presented to replace the diode rectifiers for their high power-factor ability. Many topologies of PWM rectifiers had been studied. The full-bridge ac/dc converter as shown in Fig. 1 claims to provide the better input current waveform and the ability of the bidirectional operation [1]–[3].

Recently, the full-bridge ac/dc converters are widely used in the single-phase rectifier application and the single-phase inverter applications, such as the power factor correction (PFC) [4], [5], the front end of the motor drive [6], [7], the photovoltaic generation system [8]–[11], the uninterruptible power source [12], and the dc microgrid system [13], [14].

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The multiloop control as shown in Fig. 1 is often used to control the full-bridge ac/dc converter [4]–[19]. There are two control loops cascaded in the multiloop control. The outer voltage control loop regulates the dc-bus voltage V_o and the inner control loop shapes the ac-side current i_s. The ac-side voltage $\mathrm{sign}(I_{\mathrm{dc}})$ is also sensed to obtain the phase information of the ac grid for the inner current control loop.

In [4], the dual hysteresis current control loop was proposed to improve the current shaping performance. Additional switches were connected to the four-switch full-bridge converter to reduce the dc-bus voltage ripple and thus, increase the power density [5]. The multiloop control was modified to reduce the circulating current in parallel full-bridge converters in [6], [7], and [10]. In addition, the maximum power point tracking scheme and the multiloop control were integrated to control the PV-based grid-tied system [8], [9]. For the parallel full-bridge inverters, the multiloop control with the centralized voltage loop and the individual current loops was proposed in [12].

For the thyristor-based bidirectional ac/dc converter in [15], the voltage sensorless concept was implemented with the multiloop control in which both the ac-side voltage and the dc-bus voltage were estimated from the sensed rising/falling rate of the inductor current. A PWM strategy for full-bridge ac/dc converter was proposed in [16] where two switches switch in the carrier frequency and the other two switches switch in the line frequency.

In current control loop, relatively high-resolution current A/D conversion is required over a wide range of the sensed ac-side currents, which increases the complexity, the power

TABLE I
SUMMARIZED RESULTS FOR VARIOUS CURRENT SENSORLESS CONTROL METHODS

		[19]	[20]	[21]	[22]	[23]	Proposed BCSC
Published Year		1995	2000	2004	2009	2010	
Topology	Diode rectifier + Boost converter	V	V	V	V	V	
	Full-Bridge converter						V
Sensorless Control	Multiloop control			V		V	
	Single-loop control	V*	V		V		V
Consideration of	the inductance	V	V	V	V	V	V
	the resistance			V	V		V
	the conduction voltages			V	V		V
	the time delay					V	
Parameters	Inductance (mH)	10		1.2	4.65		4.6
	Capacitance	2200		2200	560		1410
	Switching frequency (kHz)	19.2	2.5	160	25	73	40
	AC-side voltage	115		55	110	220	110
	DC bus voltage (V)	215		100	300		200
	Power (W)	1000		400	500		500

* means that additional load current is measured.

consumption, and the cost of the controller implementation [17]. In [17] and [18], the comparator-based sensing methods without using the real analog-to-digital converters (ADCs) were proposed to save the hardware cost in the multiloop control.

In order to remove the current measurement, numerous approaches were proposed in [19]–[23] and tabulated in Table I. Like the voltage sensorless concept in [15], the inductor current in continuous conducting mode (CCM) was rebuilt by the sensed voltages [23]. All the listed current sensorless control methods were developed for the single-phase diode rectifier plus the boost converter, but not for bidirectional circuits. In addition, because that the rules in CCM are significantly simpler than those in discontinuous conduction mode (DCM), all the listed methods are developed based on CCM. Therefore, to guarantee operating in CCM during the whole cycle, bulky inductors are often selected [19], [21], [22].

Both voltage control loop and current control loop exist in [21] and [23]. But only single voltage loop is included in [19], [20], and [22]. Recently, to obtain the accurate current estimation and reduce the accumulative error, the inductance, the inductor resistance, and the conduction voltage had been considered in [21] and [22]. The time delay had also been considered in [23]. It shows that considering only inductance cannot meet the current sensorless operation of the PFC function. In this paper, the bidirectional current sensorless control (BCSC) for the full-bridge converter is first proposed. Only the voltage control loop is included in the proposed BCSC, and both the inductor resistance and the conduction voltage are considered.

This paper is organized as following. In first, the behavior of a full-bridge converter is studied and it can be simplified to an equivalent single-switch model. Based on the developed model, the BCSC is proposed. By considering the power flow direction and the polarity of the ac-side voltage, the four switching signals are generated. Finally, the provided simulation and the experiment results are able to verify the proposed BCSC.

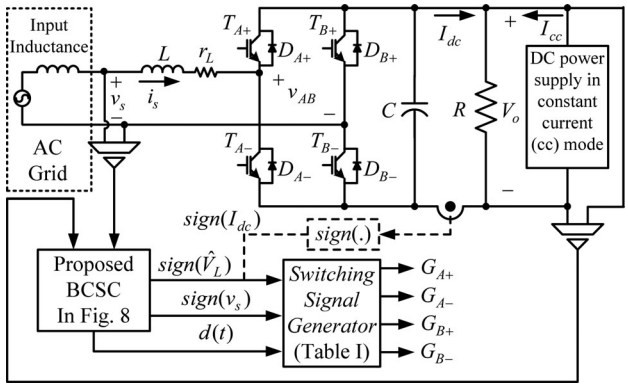

Fig. 2. Full-bridge ac/dc converter with the proposed control method.

II. SINGLE-SWITCH MODEL FOR THE FULL-BRIDGE AC/DC CONVERTER

Fig. 1 shows the full-bridge ac/dc converter with the proposed control configuration. A full-bridge converter with four switches is connected between the ac grid and the dc bus. Both the ac-side voltage v_s and the dc-bus voltage V_o are sensed. The four switching signals $\mathrm{G_{A+}}, \mathrm{G_{A-}}, \mathrm{G_{B+}}$, and $\mathrm{G_{B-}}$ are generated from the switching signal generator according to three input signals $\mathrm{sign}(\hat{V}_L)$, sign (v_s), and $d(t)$. The switching signal $d(t)$ is generated from the proposed BCSC and the sign function $\mathrm{sign}(x)$ is denoted as

$$\mathrm{sign}(x) = \begin{cases} 1, & \text{when } x \geq 0 \\ 0, & \text{when } x < 0 \end{cases}. \tag{1}$$

In order to represent the behavior of the full-bridge converter accurately, the inductor resistance and the voltage drops of the semiconductor devices are also considered in this paper. In addition, CCM is assumed during the line cycle.

A dc power supply operated in constant current (cc) mode is connected to the dc bus to represent the direct power flow to the dc bus. Since the yielded current I_{cc} of the connected dc power supply cannot be negative (i.e., $I_{\mathrm{cc}} \geq 0$), a resistor R is also connected in the dc bus to represent the load power in dc side.

When the power flow $V_o I_{\mathrm{cc}}$ is larger than the load power V_{o}^2/R (i.e., the negative current $I_{\mathrm{dc}} < 0$), the dc-bus voltage V_o would rise due to the capacitor C connected in the dc bus. In order to regulate the dc-bus voltage V_o, excess power should be transferred from dc-side bus to ac grid and thus, the full-bridge converter needs to operate at the inverter mode. Contrarily, the full-bridge converter needs to operate at the rectifier mode when the power flow $V_o I_{\mathrm{cc}}$ is smaller than the load power V_{o}^2/R (i.e., the positive current $I_{\mathrm{dc}} > 0$).

Therefore, the signal $\mathrm{sign}(I_{\mathrm{dc}})$ shown as the dashed line in Fig. 2 is helpful in the derivation of the following single-switch model of the full-bridge converter. However, this signal $\mathrm{sign}(I_{\mathrm{dc}})$ can be equivalently replaced by the other sign value signal in the proposed BCSC. Therefore, the proposed control method does not need to sense any current in fact.

TABLE II
SUMMARY OF SWITCHING SIGNAL COMBINATION

$sign(I_{dc})$	$sign(v_s)$	$d(t)$	G_{A+}	G_{A-}	G_{B+}	G_{B-}	Flowing path
1 (Rectifier)	1 (Positive voltage)	1	OFF	ON	OFF	OFF	T_{A-}, D_{B-}
		0	OFF	OFF	OFF	OFF	D_{A+}, D_{B-}
	0 (Negative voltage)	1	ON	OFF	OFF	OFF	T_{A+}, D_{B+}
		0	OFF	OFF	OFF	OFF	D_{A-}, D_{B+}
0 (Inverter)	1 (Positive voltage)	1	ON	OFF	OFF	OFF	T_{A+}, D_{B+}
		0	ON	OFF	OFF	ON	T_{A+}, T_{B-}
	0 (Negative voltage)	1	OFF	ON	OFF	OFF	T_{A-}, D_{B-}
		0	OFF	ON	ON	OFF	T_{A-}, T_{B+}

According to the switching signal $d(t)$, the sign value sign (v_s) of input voltage v_s and the power direction signal sign $(I_{\rm dc})$, four switching signals G_{A+}, G_{A-}, G_{B+}, and G_{B-} are generated based on the following rules. The summaries of generating rules are tabulated in Table II

$$G_{A+} = \overline{\text{sign}(I_{\rm dc})} \cdot \text{sign}(v_s) + \text{sign}(I_{\rm dc}) \cdot \overline{\text{sign}(v_s)} \cdot d(t) \quad (2)$$

$$G_{A-} = \overline{\text{sign}(I_{\rm dc})} \cdot \overline{\text{sign}(v_s)} + \text{sign}(I_{\rm dc}) \cdot \text{sign}(v_s) \cdot d(t) \quad (3)$$

$$G_{B+} = \overline{\text{sign}(I_{\rm dc})} \cdot \overline{\text{sign}(v_s)} \cdot \overline{d(t)} \quad (4)$$

$$G_{B-} = \overline{\text{sign}(I_{\rm dc})} \cdot \text{sign}(v_s) \cdot \overline{d(t)}. \quad (5)$$

In the following sections, the behaviors at the rectifier mode and the inverter mode are studied, respectively.

A. Rectifier Operation $(\text{sign}(I_{\rm dc}) = 1)$

At the rectifier operation $\text{sign}(I_{\rm dc}) = 1$, only one switch switches with the switching signal $d(t)$ and the other three switches block. When the ac-side voltage is positive $v_s > 0$, only the switch T_{A-} switches with the switching signal $d(t)$ and the other switches keep turning OFF. As the ac-side voltage is negative $v_s < 0$, only the switch T_{A+} switches with the signal $d(t)$.

According to (2)–(5), the gate signals during the positive input voltage $(\text{sign}(v_s) = 1)$ and during the negative input voltage $(\text{sign}(v_s) = 0)$ can be summarized as (6) and (7), respectively. Switching signal $d(t)$ is either $d(t) = 1$ or $d(t) = 0$

$$G_{A+} = 0,\ G_{A-} = d(t),\ G_{B+} = 0,\ G_{B-} = 0,$$
$$\text{when positive voltage } \text{sign}(v_s) = 1 \quad (6)$$

$$G_{A+} = d(t),\ G_{A-} = 0,\ G_{B+} = 0,\ G_{B-} = 0,$$
$$\text{when negative voltage sign}(v_s) = 0. \quad (7)$$

The resulting current flowing paths during positive input voltage and negative input voltage are plotted in Figs. 3 and 4,

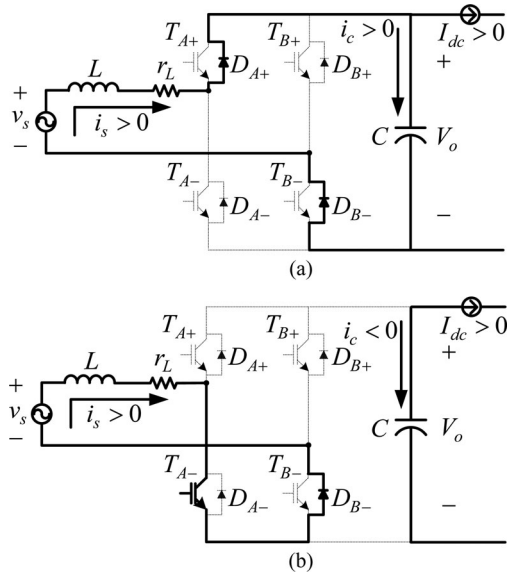

Fig. 3. Current flowing path during positive input voltage $v_s > 0$ (a) when the switching signal $d(t) = 1$, (b) when $d(t) = 0$.

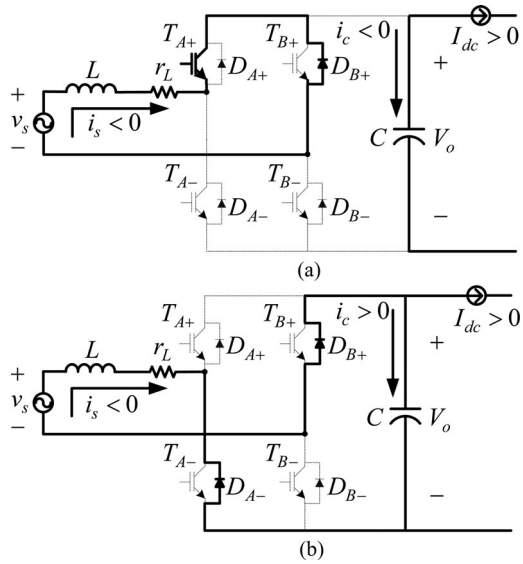

Fig. 4. Current flowing path during negative input voltage $v_s < 0$ (a) when the switching signal $d(t) = 1$, (b) when $d(t) = 0$.

respectively. When the switching signal $d(t) = 1$, the inductor voltage of Figs. 3(a) and 4(a) can be expressed as (8) and (9), respectively

$$v_L = v_s - V_F - r_L i_s, \quad \text{when positive voltage sign}(v_s) = 1 \quad (8)$$

$$v_L = v_s + V_F - r_L i_s, \quad \text{when negative voltage sign}(v_s) = 0 \quad (9)$$

where the constant V_F is assumed to represent the total conduction drops through the flowing path. Then, the inductor voltage in (8) and (9) for $d(t) = 1$ can be combined to the following

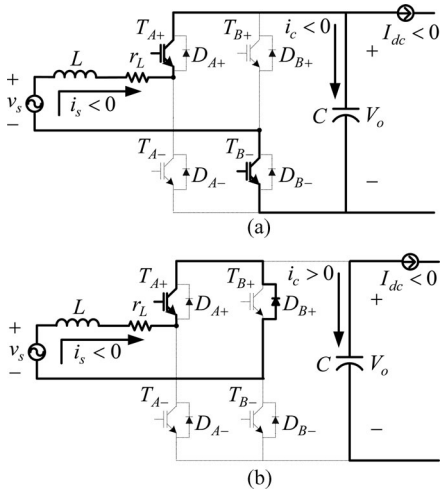

Fig. 5. Current flowing path during positive input voltage $v_s > 0$ (a) when the switching signal $d(t) = 1$, (b) when $d(t) = 0$.

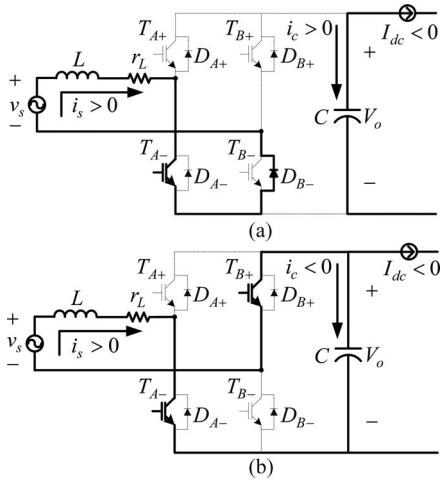

Fig. 6 Current flowing path during negative input voltage $v_s < 0$ (a) when the switching signal $d(t) = 1$, (b) when $d(t) = 0$.

equation:

$$v_L = v_s - [2\text{sign}(v_s) - 1]V_F - r_L i_s, \quad \text{when } d(t) = 1. \tag{10}$$

Similarly, the inductor voltage of Figs. 3(b) and 4(b) for $d(t) = 0$ can be expressed as (11) and (12), respectively

$$v_L = v_s - V_F - r_L i_s - V_o, \quad \text{when positive voltage sign}(v_s) = 1 \tag{11}$$

$$v_L = v_s + V_F - r_L i_s + V_o, \quad \text{when negative voltage sign}(v_s) = 0. \tag{12}$$

These two equations can be combined to the following equation

$$v_L = v_s - [2\text{sign}(v_s) - 1]V_F - r_L i_s - [2\text{sign}(v_s) - 1]V_o, \quad \text{when } d(t) = 0. \tag{13}$$

B. Inverter Operation $(\text{sign}(I_{\text{dc}}) = 0)$

At the inverter operation $\text{sign}(I_{\text{dc}}) = 0$, two switches switch with the switching signal $d(t)$ and the others switch with the line voltage sign. When the ac-side voltage is positive $v_s > 0$, the switch T_{A+} keeps turning ON and the switch T_{B-} switches with the complement switching signal $\overline{d(t)}$. The other two switches T_{B+} and T_{A-} keep turning OFF. As the ac-side voltage turns to negative $v_s < 0$, the switch T_{A-} keeps turning ON and the switch T_{B+} switches with the complement switching signal $\overline{d(t)}$.

The gate signals during the positive input voltage $(\text{sign}(v_s) = 1)$ and during the negative input voltage $(\text{sign}(v_s) = 0)$ can be summarized as (14) and (15), respectively

$$G_{A+} = 1,\ G_{A-} = 0,\ G_{B+} = 0,\ G_{B-} = \overline{d(t)} \tag{14}$$

$$G_{A+} = 0,\ G_{A-} = 1,\ G_{B+} = \overline{d(t)},\ G_{B-} = 0. \tag{15}$$

In addition, the resulting current flowing paths during positive input voltage and negative input voltage are plotted in Figs. 5 and 6, respectively. When $d(t) = 1$, the inductor voltage of Figs. 5(a) and 6(a) can be expressed as (16) and (17), respectively

$$v_L = v_s + V_F - r_L i_s, \quad \text{when positive voltage sign}(v_s) = 1 \tag{16}$$

$$v_L = v_s - V_F - r_L i_s, \quad \text{when negative voltage sign}(v_s) = 0. \tag{17}$$

From (16) and (17), the inductor voltage for $d(t) = 1$ can be simplified to the following equation:

$$v_L = v_s + [2\text{sign}(v_s) - 1]V_F - r_L i_s, \quad \text{when } d(t) = 1. \tag{18}$$

Likewise, from Figs. 5(b) and 6(b), the inductor voltage for $d(t) = 0$ can be represented together

$$v_L = v_s + [2\text{sign}(v_s) - 1]V_F - r_L i_s - [2\text{sign}(v_s) - 1]V_o, \quad \text{when } d(t) = 0. \tag{19}$$

C. Equivalent Single-Switch Model

By considering both (10) at the rectifier mode $\text{sign}(I_{\text{dc}}) = 1$ and (18) at the inverter mode $\text{sign}(I_{\text{dc}}) = 0$, the inductor voltage can be expressed in terms of the power direction signal $\text{sign}(I_{\text{dc}})$ and the voltage polarity signal $\text{sign}(v_s)$.

$$v_L = v_s - K_F V_F - r_L i_s, \quad \text{when } d(t) = 1. \tag{20}$$

Similarly, from (13) and (19), the inductor voltage for $d(t) = 0$ can be expressed as

$$v_L = v_s - K_F V_F - r_L i_s - K_o V_o, \quad \text{when } d(t) = 0. \tag{21}$$

Therefore, according to (20) and (21), the equivalent single-switch model for the bidirectional full-bridge ac/dc converter can be plotted in Fig. 7 where $K_F = [2\text{sign}(I_{\text{dc}}) - 1][2\text{sign}(v_s) - 1]$ and $K_o = [2\text{sign}(v_s) - 1]$ are two gains to represent the effects of the total conduction voltage drop V_F and the dc-side voltage V_o, respectively.

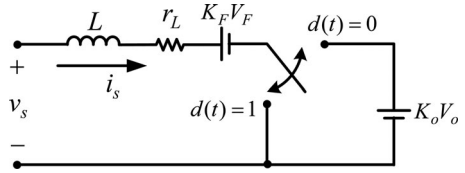

Fig. 7. Equivalent single-switch modeling of the full-bridge AC/DC converter.

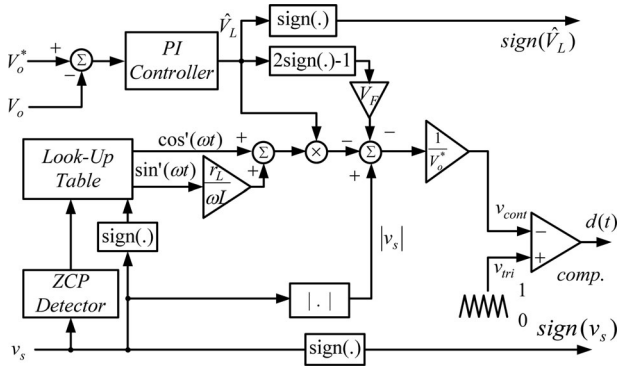

Fig. 8. Proposed BCSC.

III. Proposed Controller

From the developed equivalent single-switch model of the full-bridge ac/dc converter, the average inductor voltage $\langle v_L \rangle_{T_s}$ can be calculated with multiplying (20) by the conducting time $T_s \cdot \langle d(t) \rangle_{T_s}$ and multiplying (21) by the blocking time $T_s \cdot (1 - \langle d(t) \rangle_{T_s})$ where $\langle v_{\rm L} \rangle_{T_s}$ represents the average value of the inductor voltage $v_{\rm L}$ within the switching period T_s.

Then, the average inductor voltage $\langle v_L \rangle_{T_s}$ can be expressed as

$$\langle v_L \rangle_{T_s} = v_s - K_F V_F - r_L i_s - K_o (1 - \langle d(t) \rangle_{T_s}) V_o. \quad (22)$$

A. BCSC

The proposed BCSC is plotted in Fig. 8 where the triangular signal $v_{\rm tri}$ varies between 0 and 1 periodically. A proportional-integral (PI)-type voltage controller is used to regulate the dc-bus voltage V_o and shape the ac-side current waveform effectively. Two signals $\cos'(\omega t)$ and $\sin'(\omega t)$ are generated from the action of the look-up table. Both $\cos'(\omega t)$ and $\sin'(\omega t)$ are synchronized to the zero-crossing instants of the ac-side voltage v_s via the zero-crossing point detector (ZCP Detector).

The switching signal $d(t)$ is obtained from the comparison of the control signal $v_{\rm cont}$ and the triangular signal $v_{\rm tri}$. Thus, the duty ratio of the switching signal $d(t)$ can be expressed as

$$\langle d(t) \rangle_{T_s} = 1 - \langle v_{\rm cont} \rangle_{T_s}. \quad (23)$$

In order to yield a sinusoidal ac-grid current $i_s = \hat{I}_s \sin(\omega t)$ in phase with the ac-grid voltage v_s, the average inductor voltage $\langle v_L \rangle_{T_s}$ must follow the function $\cos(\omega t)$. Thus, the desired average inductor voltage can be expressed as $\langle v_L \rangle_{T_s} = \hat{\rm V}_L \cos(\omega t)$ where the bipolar signal $\hat{\rm V}_L$ represents the inductor voltage amplitude. Since the average inductor voltage $\langle v_L \rangle_{T_s}$ is expressed as $\hat{\rm V}_L \cos(\omega t)$, the yielded average inductor current $\langle i_L \rangle_{T_s}$ would be

$$\langle i_L \rangle_{T_s} = \frac{\hat{\rm V}_L}{\omega L} \sin(\omega t) = \hat{\rm I}_s \sin(\omega t). \quad (24)$$

By substituting $\langle v_L \rangle_{T_s} = \hat{\rm V}_L \cos(\omega t)$, (23) and (24) into (22), the average control signal $\langle v_{\rm cont} \rangle_{T_s}$ needs to be

$$\langle v_{\rm cont} \rangle_{T_s} = \frac{1}{V_o} \left\{ \begin{array}{l} \dfrac{v_s}{[2{\rm sign}(v_s) - 1]} - [2{\rm sign}(I_{\rm dc}) - 1] V_F \\ -\dfrac{\hat{\rm V}_L}{[2{\rm sign}(v_s) - 1]} \left[\cos(\omega t) + \dfrac{r_L}{\omega L} \sin(\omega t) \right] \end{array} \right\}. \quad (25)$$

The average value of the yielded instantaneous power $p_s = \langle v_s \cdot i_s \rangle_{T_s}$ within the switching period T_s becomes

$$p_s = \frac{\hat{V}_s \hat{I}_s}{2} (1 - \cos 2\omega t) = \frac{\hat{V}_s}{2\omega L} \hat{\rm V}_L - \frac{\hat{V}_s}{2\omega L} \hat{\rm V}_L \cos 2\omega t. \quad (26)$$

Furthermore, the average power P from ac grid to dc bus is the average value of the instantaneous power $\langle v_s \cdot i_s \rangle_T$ within the line period ${\rm T} = \omega / 2\pi$.

$$P = \langle v_s \cdot i_s \rangle_T = \frac{\hat{V}_s}{2\omega L} \hat{V}_L. \quad (27)$$

B. Replacement for sign $I_{\rm dc}$

Equation (27) is very important for the proposed BCSC. First, the signal $\hat{V}_L$ is bipolar, and thus, the yielded power flow P is bidirectional. It means that the proposed BCSC is able to operate in both the rectifier operation and the inverter operation.

In addition, the sign value ${\rm sign}(\hat{\rm V}_L) = 1$ means that the average power is positive $P > 0$ (i.e., rectifier operation with ${\rm sign}(I_{\rm dc}) = 1$). Zero value ${\rm sign}(\hat{\rm V}_L) = 0$ means negative average power $P < 0$ (i.e., inverter operation with ${\rm sign}(I_{\rm dc}) = 0$). Therefore, the sign value ${\rm sign}(\hat{\rm V}_L)$ can be used to equivalently replace for the sign value ${\rm sign}(I_{\rm dc})$ shown in Table I, Fig. 2, and (25). The resulting control signal $v_{\rm cont}$ can be obtained by

$$\langle v_{\rm cont} \rangle_{T_s} = \frac{1}{V_o^*} \left\{ |v_s| - [2{\rm sign}(\hat{V}_L) - 1] V_F - \hat{\rm V}_L \left[\cos'(\omega t) + \frac{r_L}{\omega L} \sin'(\omega t) \right] \right\} \quad (28)$$

where $\cos'(\omega t) = K_o \cos(\omega t)$ and $\sin'(\omega t) = K_o \sin(\omega t)$. The first term in the right-hand of (25) is equal to the rectified input voltage $|v_s|$.

Based on (28), the control signal $v_{\rm cont}$ of the proposed BCSC is plotted in Fig. 8. Because that the signal ${\rm sign}(I_{\rm dc})$ is equivalently replaced by the sign value ${\rm sign}(\hat{\rm V}_L)$, the proposed BCSC does not need to sense the dc bus current $I_{\rm dc}$ in fact.

C. PI-Type Controller

The transfer function of the output voltage perturbation ΔV_o due to the controller output signal $\Delta \hat{\rm V}_L$ can be obtained from the instantaneous power balance $p_s = p_C + p_{\rm dc}$ between the ac-side power p_s, the dc-side delivered power $p_{\rm dc}$ and the capacitor power p_C [10].

From (22), the instantaneous power p_s can be written as

$$p_s = \frac{\hat{v}_s}{2\omega L}(\hat{V}_L + \Delta\hat{V}_L)(1 - \cos 2\omega t). \tag{29}$$

The dc-side delivered power $p_{\rm dc}$ with the small perturbation $\Delta p_{\rm dc}$ can be represented by the voltage command ΔV_o^* plus the perturbation ΔV_o

$$p_{\rm dc} = \frac{(V_o^* + \Delta V_o)^2}{R} \approx \frac{(V_o^*)^2}{R} + \frac{2V_o^*\Delta V_o}{R}. \tag{30}$$

The capacitor power p_C can be represented by the voltage perturbation ΔV_o

$$p_C = \frac{d(\frac{1}{2}C(V_o^* + \Delta V_o)^2)}{dt} \approx CV_o^*\frac{d\Delta V_o}{dt}. \tag{31}$$

By neglecting the double line-frequency component in the instantaneous power p_s, substituting (29)–(31) into the balance $p_s = p_C + p_{\rm dc}$ can yield the following small-signal transfer function $G_s(s)$

$$G_s(s) = \frac{\Delta V_{\rm o}(s)}{\Delta\hat{\rm V}_L(s)} = \frac{\hat{V}_s}{2\omega LCV_o^*}\frac{1}{(s + \frac{2}{RC})}. \tag{32}$$

Obviously, the small-signal behavior of the dc-bus voltage can be seen as a first-order model. Thus, the output voltage can be well regulated by including the PI-type controller in the proposed BCSC. After choosing the ratio of proportional gain k_P and the integral gain k_I to the pole of $G_s(s)$

$$\frac{k_I}{k_P} = \frac{2}{RC} \tag{33}$$

the closed-loop transfer function of the output voltage ΔV_o and the output voltage command ΔV_o^* can be obtained

$$\frac{\Delta V_o(s)}{\Delta V_o^*(s)} = \frac{k_P\frac{\hat{V}_s}{2\omega LCV_o^*}}{s + k_P\frac{\hat{V}_s}{2\omega LCV_o^*}}. \tag{34}$$

The closed-loop transfer function (34) can be seen as a low-pass filter. In order to avoid the effect of the double line-frequency voltage ripple in dc voltage bus, the cutoff frequency of (34) is chosen to be far smaller than the double line frequency. Therefore, the proportional gain can be chosen by

$$k_P = \frac{\omega^2 LCV_o^*}{50\hat{V}_s}. \tag{35}$$

IV. Simulation Results

In this section, a series of computer simulations are performed to demonstrate the proposed BCSC. Some nominal values and circuit elements are listed in Table III. The simple PI-type voltage controller is used to regulate the output voltage and shape the current waveform.

In the simulation, a resistor $R = 80\ \Omega$ is connected to the dc bus and a current source $I_{\rm cc}$ is also connected to dc bus to represent the direct power flow to the dc bus. When the current source $I_{\rm cc}$ is zero, the full-bridge ac/dc converter needs to operate in the rectifier mode to transfer the average power 500 W from ac grid to dc bus to regulate the dc-bus voltage. Once the current $I_{\rm cc}$ is larger than 2.5 A, the full-bridge converter needs to operate in the inverter mode to move some power from dc bus to ac grid.

TABLE III
Simulation Parameters

DC-bus Voltage	$V_o^* = 200V$
Input Voltage	$110Vrms$
Input Frequency	$f = 60Hz$
Inductance	$L = 4.6mH$
Equivalent resistance	$r_L = 0.5\Omega$
Capacitance	$C = 1410\mu F$
Conduction voltage	$V_F = 1.61V$.
Switching frequency	$f_{tri} = 40kHz$

A. Pure Sinusoidal Grid Voltage

The simulated waveforms when the full-bridge converter operates in the rectifier mode and in the inverter mode are plotted in Fig. 9(a) and (b), respectively. The input current i_s is sinusoidal in phase with the input voltage v_s and the voltage amplitude $\hat{V}_L$ is tuned to about 12.0 V.

In Fig. 9(a), the current $I_{\rm cc}$ is set to zero, and the dc-side power is near 500 W. To supply the dissipated energy of the resistor $R = 80\ \Omega$, the full-bridge converter needs to provide the power flow near 500 W to dc bus. Two synchronized signals $\cos'(\omega t)$ and $\sin'(\omega t)$ with double line frequency are generated from the alignments to the ZCPs of the ac-grid voltage. The voltage waveform $v_{\rm ab}$ shows that the used PWM method can be seen as the unipolar PWM method, but its ripple frequency is the same as the carrier frequency.

In this simulation, the inductor resistance and the conduction voltages of the semiconductor devices are not set to zero. With consideration of the loss of the full-bridge converter, the yielded average power is near 530 W larger than 500 W.

On the contrary, when the current source $I_{\rm cc}$ is set to 5 A, the total dc-side power now is -500 W. In order to regulate the dc-bus voltage, near 500 W power needs to be transferred from dc bus and thus, the full-bridge ac/dc converter turns to the inverter mode as shown in Fig 9(b). The yielded current is sinusoidal and the steady-state value of the voltage amplitude signal $\hat{V}_L$ is about -9.7 V. It is noted that the net power flow into ac grid is near 470 W smaller than 500 W due to the loss of the full-bridge converter.

Therefore, the steady-state amplitude $\hat{V}_L$ is not equalized. When the system absorbing power from ac grid, the steady state $\hat{V}_L$ is about 12.0 V, but when the system is delivering power to the ac grid, the steady state $\hat{V}_L$ is about -9.7 V, not -12 V.

B. Distorted Grid Voltage

In the practical condition, the input voltage is often distorted due to the input inductance as shown in Fig. 2. To evaluate the performance of the proposed BCSC, the simulated waveforms with distorted input voltage at the rectifier mode and the inverter mode are plotted in Fig. 10(a) and (b), respectively. Although the ac-grid voltage v_s is distorted, the yielded input currents i_s are

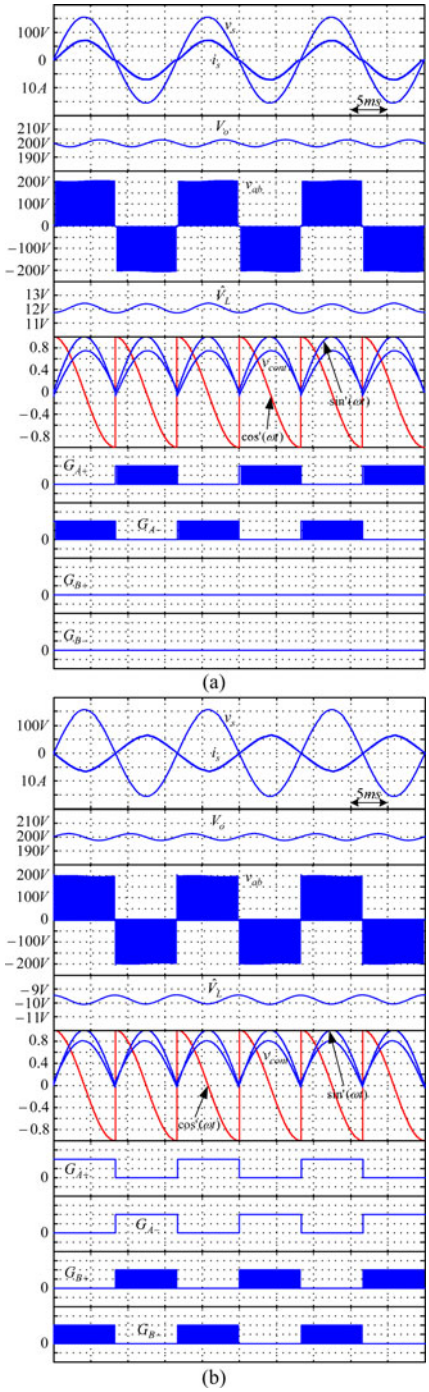

Fig. 9. Simulation results when the full-bridge converter operates (a) in rectifier mode with average input power ≈530 W ($I_{\rm cc} = 0$ A), (b) in inverter mode with average input power ≈−470 W ($I_{\rm cc} = 5$ A).

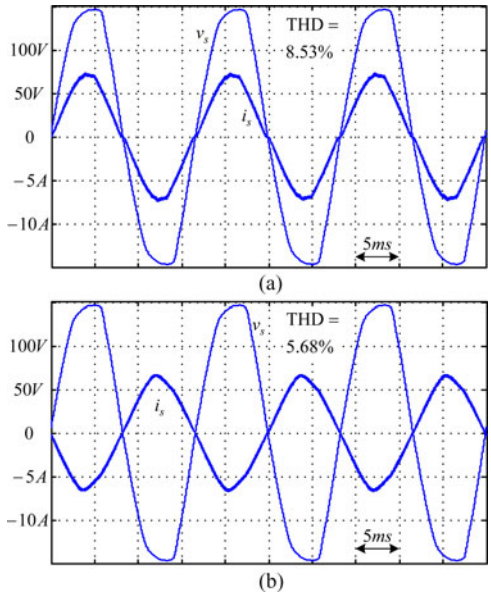

Fig. 10. Simulation results with distorted input voltage (a) in the rectifier mode with the average power ≈530 W (i.e., $I_{\rm cc} = 0$ A), (b) in the inverter mode with the average power ≈−470 W (i.e., $I_{\rm cc} = 5$ A).

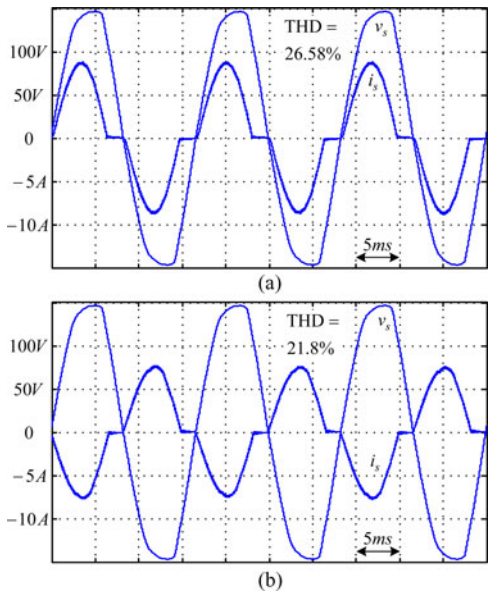

Fig. 11. Simulation results with considering only inductance (a) in the rectifier mode with the average power ≈530 W (i.e., $I_{\rm cc} = 0$ A), (b) in the inverter mode with the average power ≈−470 W (i.e., $I_{\rm cc} = 5$ A).

closed to the sinusoidal waveforms. It shows that the proposed BCSC is also able to work well with the distorted input voltage.

The simulated steady-state waveforms without considering the inductor resistance and the conduction voltage (i.e., with considering only inductance) at the rectifier mode and the inverter mode are plotted in Fig. 11(a) and (b), respectively. The current initiates flowing at one ZCP, but falls to zero prior to the next ZCP. The resulting zero-current duration makes power factor leading and introduces larger current harmonics. The results show that the proposed BCSC without considering the parasitic effects is still stable, but yielded current waveform may not be acceptable.

In practice, the circuit parameters may change due to the heat from the power loss. As the inductor temperature increases, the resistance may increase but the inductance may decrease, which contributes to the circuit uncertainty.

With 10% changes of the circuit parameters $r_L = 0.5\ \Omega \times 1.1, L = 4.6$ mH $\times\ 0.9$ and no change of the control parameters $r_L = 0.5\ \Omega, L = 4.6$ mH, the simulated steady-state

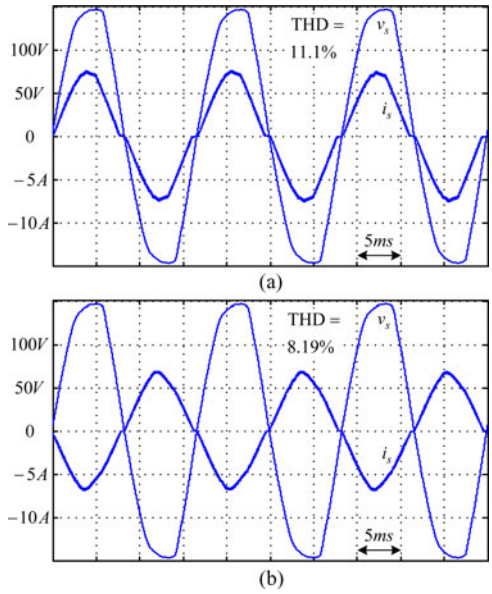

Fig. 12. Simulation results with circuit parameters $r_L = 0.5\ \Omega \times 1.1$ and $L = 4.6$ mH $\times\ 0.9$ (a) in the rectifier mode with the average power ≈530 W (i.e., $I_{\rm cc} = 0$ A), (b) in the inverter mode with the average power ≈−470 W (i.e,. $I_{\rm cc} = 5$ A).

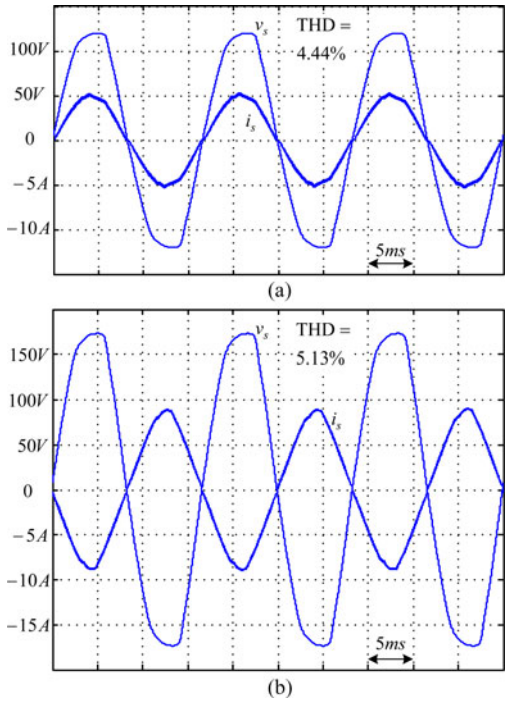

Fig. 13. Simulation results with various power levels and various input voltages (a) with the average power ≈320 W (i.e., $I_{\rm cc} = 1.0$ A) under input voltage 90 Vrms, (b) with the average power ≈−750 W (i.e,. $I_{\rm cc} = 6.5$ A) under input voltage 130 Vrms.

waveforms at the rectifier mode and the inverter mode are plotted in Fig. 12(a) and (b), respectively.

The results show that the proposed BCSC is stable, but the circuit yields larger current harmonics than the uncertainty-free case as shown in Fig. 10. However, the current waveforms in Fig. 12 are better than the special case with considering only inductance as shown in Fig. 11, which also shows the benefits of considering the resistance and the conduction voltage in this paper.

The simulated waveforms with the average power ≈320 W (i.e., $I_{\rm cc} = 1.0$ A) and input voltage 90 Vrms are plotted in Fig. 13(a). Additionally, the simulated waveforms with the average power ≈−750 W (i.e., $I_{\rm cc} = 6.5$ A) under input voltage 130 Vrms are plotted in Fig. 13(b).

The yielded currents initiate flowing at the voltage ZCPs, and returns to zero near the next ZCPs, which shows that the proposed BCSC is able to work under various power levels and various input voltages. However, the reported total harmonic distortion (THD) value in Fig. 13 is smaller than the uncertainty-free case as shown in Fig. 10. It means that the circuit parameters need to be optimized to yield the smallest current harmonics at the rated conditions.

C. Transient Response

In order to evaluate the transient performance of the proposed BCSC, the simulated waveform with the sudden change of dc current source from $I_{\rm cc} = 0$ A to $I_{\rm cc} = 4$ A and from $I_{\rm cc} = 4$ A to $I_{\rm cc} = 0$ A are plotted in Fig. 14(a) and (b), respectively.

In Fig. 11(a), the current $I_{\rm cc}$ increases suddenly from 0 to 4 A, and the dc-side current $I_{\rm dc}$ has a sudden drop from 2 to −2 A. The sudden change contributes to the rapid rise of the dc-bus voltage V_o. It means that the full-bridge ac/dc converter needs to operate at the inverter mode to sweep the power imbalance.

At the same time, the negative voltage error ε_V turns to negative, and thus, the PI-type controller tunes its output $\hat{V}_L$ from the positive value 9.2 V to the negative value −7.9 V in order to regulate the dc-bus voltage V_o. After less than 40 ms, the dc-bus voltage is restored and the yielded input current is near sinusoidal waveform.

Due to the input inductance in the ac grid, the measured voltage v_s in the rectifier operation is the infinite bus voltage minus the voltage drop of the inductor. But in the inverter operation, the voltage drop is negative and the ac-grid voltage v_s would be larger than that in the rectifier operation. Therefore, the peak amplitude of the ac-side voltage v_s increases as shown in Fig. 14(a) after the full-bridge converter changes from the rectifier mode to the inverter mode.

Similarly, when the current $I_{\rm cc}$ decreases suddenly from 4 to 0 A, the dc-bus voltage V_o drops rapidly. In order to regulate the dc-bus voltage, the full-bridge converter needs to operate at rectifier mode and thus, the peak amplitude of the ac-side voltage decreases as shown in Fig. 14(b).

Therefore, the provided simulation results demonstrate the proposed BCSC.

V. Experimental Results

The experimental setup and the FPGA-based implementation of the proposed BCSC are plotted in Fig. 15. The circuit parameters had been tabulated in Table II. A dc power source operating

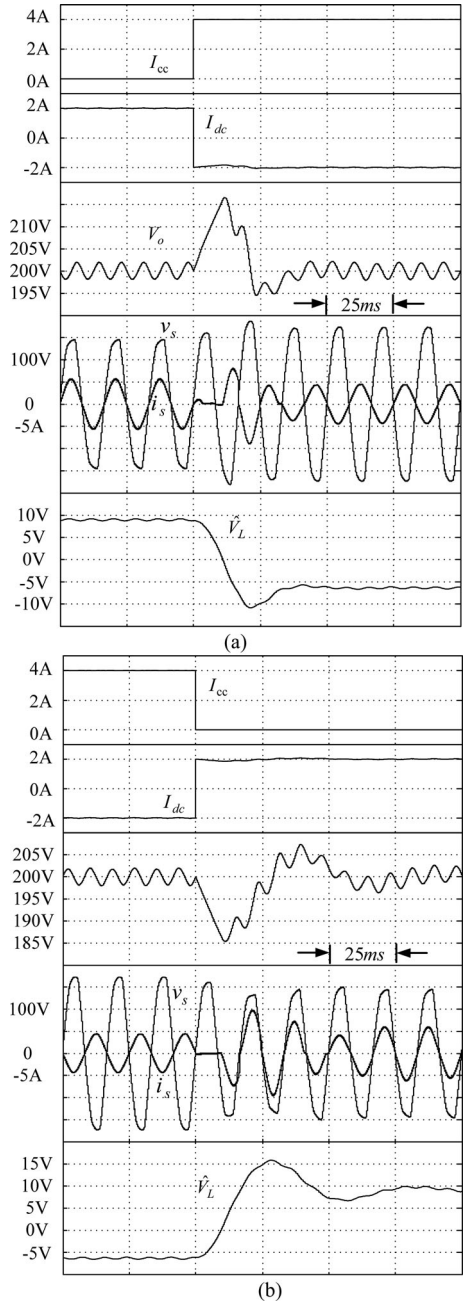

Fig. 14. Simulation results when dc current source suddenly changes (a) from $I_{\rm cc} = 0$ A to $I_{\rm cc} = 4$ A, (b) from $I_{\rm cc} = 4$ A to $I_{\rm cc} = 0$ A.

at CC mode is connected to the dc bus to represent the direct power flow into the dc bus.

Due to no A/D function in a commercial FPGA chip, an external A/D converter is used to sense the output voltage and a zero-crossing detecting circuit is used to detect the zero-crossing of the ac-side voltage. Some D/A converters are used to show the control variables of the implemented BCSC in the scope.

The average current model is the basis of the proposed BCSC and it is developed based on the CCM assumption. When the input ac voltage is at near ZCPs, the circuit often operates in DCM due to the cusp distortion. To meet the assumption of

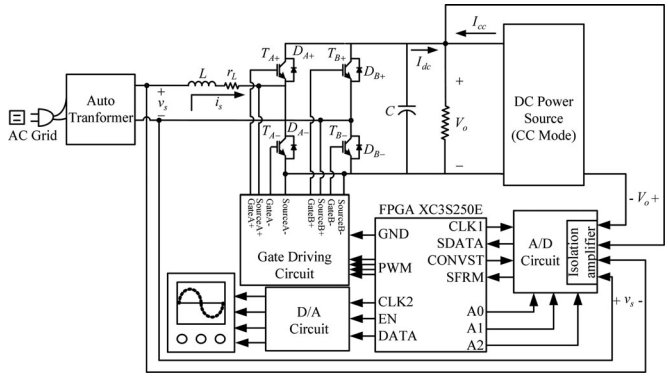

Fig. 15. Experimental setup of the proposed BCSC.

CCM, either high switching frequency or the bulky inductor should be selected.

The switching frequency 40 kHz is first selected based on the concern of PWM resolution in the FPGA-based implementation. Therefore, the bulky inductor 4.6 mH is selected to guarantee the CCM assumption. Those current sensorless control methods in Table I also select bulky inductors.

A. Pure Sinusoidal Grid Voltage

In order to provide a pure sinusoidal voltage waveform, an equipment (named programmable ac voltage source) is directly connected to the ac-side voltage. The current $I_{\rm cc}$ is set to zero and thus, the full-bridge converter needs to operate at rectifier mode. The yielded ac-side current and the dc-bus voltage waveform is plotted in Fig. 16(a).

Because that the programmable ac power source cannot absorb power, no experimental result of the inverter mode with the sinusoidal voltage is provided.

B. Distorted Grid Voltage

By plugging into the ac grid, the yielded waveforms at rectifier mode and at inverter mode are plotted in Fig. 16(b) and (c), respectively. In Fig. 16(b), the current $I_{\rm cc}$ in dc power source is set to zero and the full-bridge converter needs to operate in rectifier mode to regulate the dc-bus voltage. The yielded input current i_s is in phase with the input voltage, and some distortion can be found in Fig. 16(b) due to the distorted grid voltage. The measured THD factor is 4.81%.

In Fig. 16(c), the current $I_{\rm cc}$ in dc power source is set to 5 A and the full-bridge converter needs to transfer some power to ac grid to balance the power. The yielded input current i_s is aligned to the ac-side voltage v_s, and the measured THD factor is 14.84%.

Due to the voltage drop across the input inductance as shown in Fig. 2, the peak amplitude of the measured ac-side voltage v_s at Fig. 16(c) is larger than that in Fig. 16(b).

Since the dc power supply is operated in CC mode, its output current $I_{\rm cc}$ may be disturbed by the variation of the dc-bus voltage. Therefore, as shown in Fig. 14, the current $I_{\rm cc}$ carries double line-frequency ripple due to the double line-frequency voltage ripple in the dc voltage V_o. Thus, when the converter

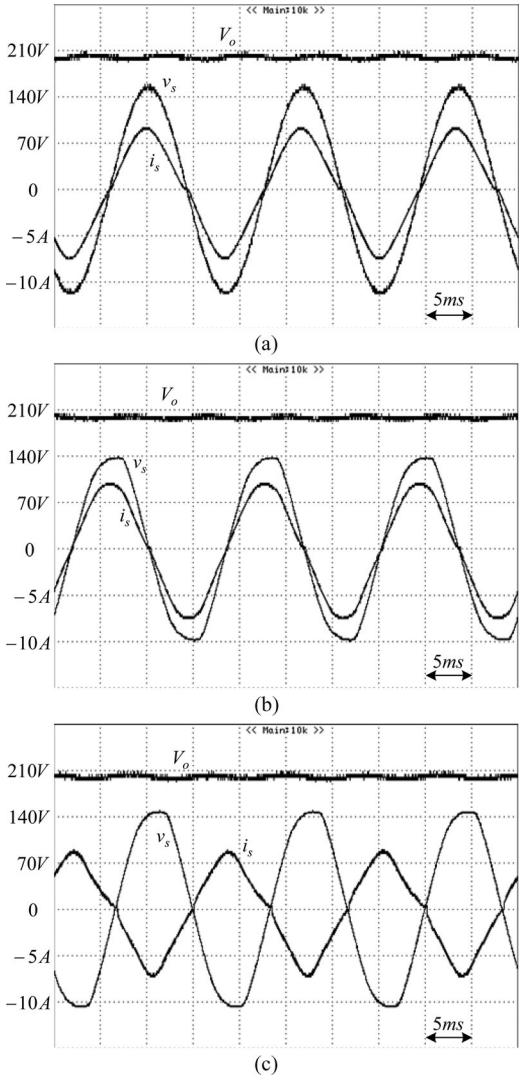

Fig. 16. Experimental waveforms (a) with sinusoidal input voltage (average input power ≈500 W); (b) with distorted input voltage (average input power ≈500 W); (c) with distorted input voltage (average input power ≈−500 W).

operated in inverter operation, the current $I_{\rm cc}$ does not keep fixed.

But the current $I_{\rm cc}$ has no current ripple when the current $I_{\rm cc}$ is set to zero. Therefore, the yielded current waveform of the inverter operation as shown in Fig. 16(c) possesses larger harmonics than that as shown in Fig. 16(b).

The experimental waveforms at distorted input voltages 90 Vrms and 130 Vrms are plotted in Figs. 17 and 18, respectively. The results show that the proposed BCSC is able to work under various input voltage and various power levels.

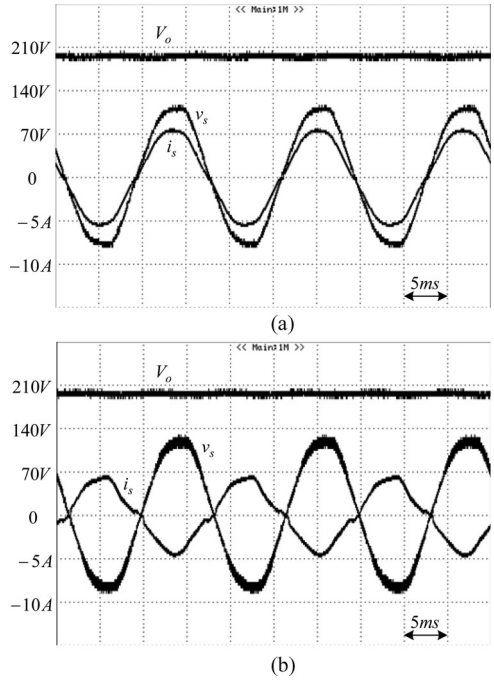

Fig. 17. Experimental waveforms at distorted input voltage 90 Vrms (a) with average input power ≈300 W; (b) with average input power ≈−300 W.

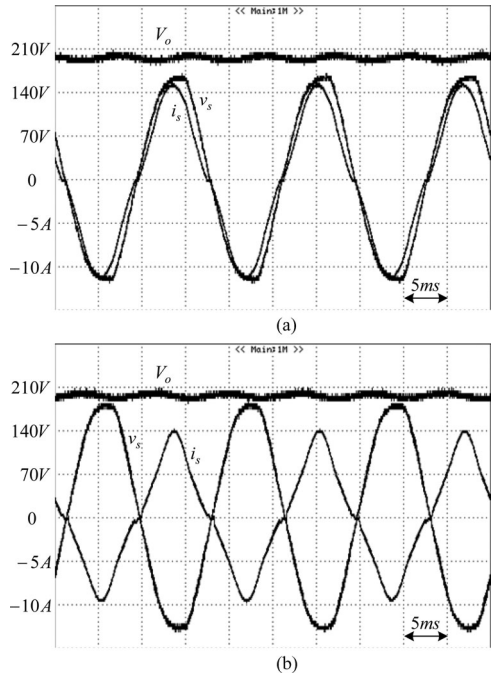

Fig. 18. Experimental waveforms at distorted input voltage 130 Vrms (a) with average input power ≈800 W; (b) with average input power ≈−800 W.

C. Transient Response

The experimental results during the change of power supply current $I_{\rm cc}$ from 0 to 4 A and from 4 to 0 A are plotted in Fig. 19(a) and (b), respectively. The dc-bus voltage V_o is well regulated to 200 V and the yielded input current i_s is in phase with the input voltage. Like the simulation results in Fig. 14, the peak amplitude of the ac-side voltage v_s may changes after the operation mode of the full-bridge converter is changed.

In addition, the real power supply current $I_{\rm cc}$ cannot change suddenly like the simulations in Fig. 14, and it has a significant transient time near 20 ms. In fact, the direct power flow to the dc

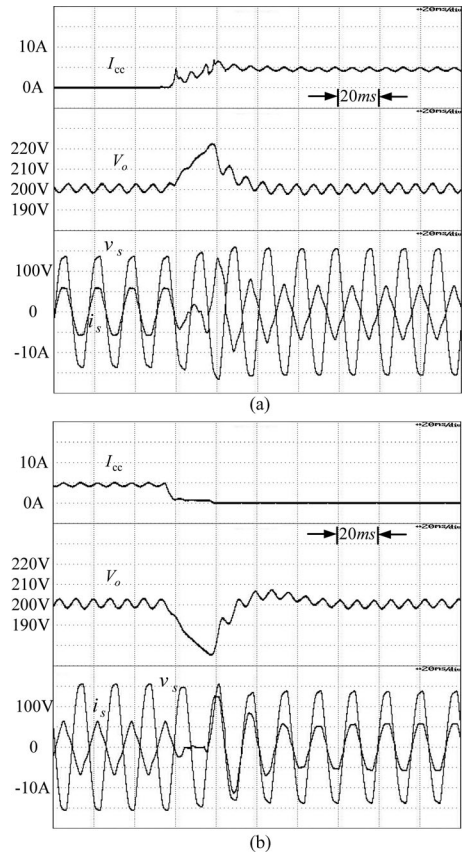

Fig. 19. Experimental waveforms during the change of direct dc power flow (a) from $I_{cc} = 0$ A to $I_{cc} = 4$ A, (b) from $I_{cc} = 4$ A to $I_{cc} = 0$ A.

bus cannot change suddenly and thus, the transient time makes the experiment more closed to the practical condition.

However, these results have verified the feasibility of the proposed system and control scheme.

VI. Conclusion

In this paper, the behavior of the full-bridge ac/dc converter has been studied and its single-switch model is proposed. According to the developed equivalent single-switch model, BCSC has been proposed and implemented. The experiment results show that the proposed BCSC is able to shape the ac-side current and regulate the dc-side voltage. The proposed BCSC with reduced number of sensor can be used to regulate the dc-grid voltage in the household application. However, the waveform in the inverter operation has larger current harmonic than that in the rectifier operation, which needs more attention to improve it.

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