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Metal-layer capacitors in the 65 nm CMOS process and the application for low-leakage power-rail ESD clamp circuit ☆

Po-Yen Chiu, Ming-Dou Ker *

Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

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ABSTRACT

Between the metal–insulator–metal (MIM) capacitor and metal–oxide–metal (MOM) capacitor, the MIM capacitor has a better characteristic of stable capacitance. However, the MOM capacitors can be easily realized through the metal interconnections, which does not need additional fabrication masks into the process. Moreover, the capacitance density of the MOM capacitor can exceed the MIM capacitor when more metal layers are used in nanoscale CMOS processes. With advantages of lower fabrication cost and higher capacitance density, the MOM capacitor could replace MIM capacitor gradually in general integrated circuit (IC) applications. Besides, the MOM capacitor ideally do not have the leakage issue. Thus, the MOM capacitor can be used instead of MOS capacitor to avoid the gate leakage issue of thin-oxide devices in nanoscale CMOS processes. With the MOM capacitor realized in the power-rail electrostatic discharge (ESD) clamp circuit, the overall leakage is decreased from 828 μA to 358 nA at 25 °C, as compared to the traditional design with MOS capacitor in the test chip fabricated in a 65 nm CMOS process.

1. Introduction

Capacitor is one of the basic components in integrated circuit (IC) applications. To meet different purposes of circuit applications, various types of capacitors have been developed with their own characteristics. Due to the limitation of capacitance per unit area, capacitors always occupy a considerable chip area in the whole circuit layout. Therefore, saving the chip area is the important consideration in capacitor selection of CMOS ICs. Nowadays, three kinds of capacitors are commonly used in IC applications, which are MOS capacitor, metal–insulator–metal (MIM) capacitor, and metal–oxide–metal (MOM) capacitor. Among those capacitors, because of thin gate oxide structure, MOS capacitor has the highest capacitance density per unit area. However, due to the disadvantages of non-linearity, higher temperature coefficient, lower breakdown voltage, and sensitive to process variations, it could not be suitable for all circuit applications. As a result, MIM capacitor and MOM capacitor were created to overcome those disadvantages for circuit applications, which need reliable capacitor characteristics [1–6]. However, the capacitance densities of MIM and MOM capacitors are much lower than the MOS capacitor. Consequently, using MIM or MOM capacitors would increase more chip area to IC products.

When the CMOS process shrinks toward nanoscale, the capacitance density of the MOS capacitor ideally will be increased when the gate oxide becomes thinner. But, thinner gate oxide makes the gate-tunneling issue more serious to cause obvious gate leakage current in the devices [7,8]. To avoid leakage current, the simple method is using the thick-oxide device to realize the MOS capacitor. However, without using the dual oxide devices in some special purposes for circuit applications, the capacitors can only be realized by MIM or MOM capacitors. Fortunately, with the dimension shrinkage in advanced CMOS processes, the lateral and vertical intervals between metal interconnects are decreased, and the parasitic capacitance between metal interconnects are increased. This feature assists the MOM capacitor to extend its capacitance density. Furthermore, with the layout structure near the fractal geometries, the MOM capacitor can have the largest capacitance density in advanced CMOS processes [1].

In this paper, the gate-tunneling mechanisms and the impacts of gate leakage current on circuit applications are described in Section 2. Two different metal-layer capacitors of MIM capacitor and MOM capacitor are compared in Section 3. Finally, the experimental verifications in silicon chip including the capacitance measurement and gate leakage in RC-based power-rail ESD clamp circuits are presented in Section 4.

2. Gate-tunneling mechanisms and impacts of gate leakage current on circuit applications in advanced CMOS processes

Three gate-tunneling mechanisms were reported to explain the gate leakage in CMOS technology [7,8]. As shown in Fig. 1, three

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* Corresponding author. Tel.: +886 3 5131573; fax: +886 5 715412.
E-mail address: mdker@ieee.org (M.-D. Ker).

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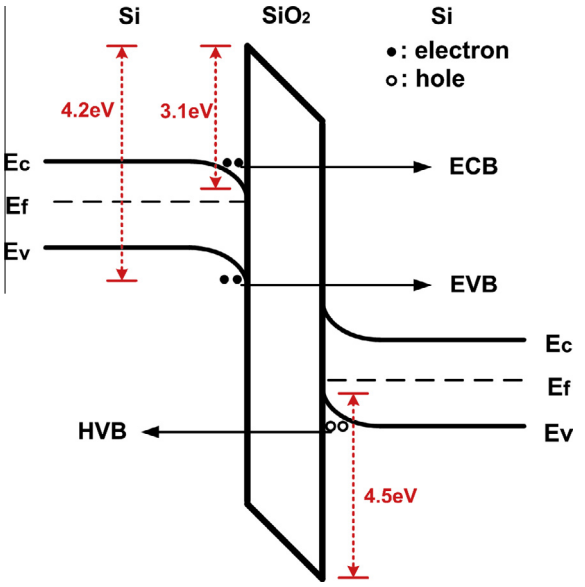

Fig. 1. Gate-tunneling mechanisms in a $Si/SiO_2/Si$ structure [4,5].

mechanisms are electron tunneling from the conduction band (ECB), electron tunneling from the valence band (EVB), and hole tunneling from the valence band (HVB). When the gate oxide thickness is scaled down, the tunneling carriers across the potential barrier are increased with a great proportion to result in the gate leakage current. In nanoscale CMOS processes, the gate oxide thickness of MOS devices was only a few nanometers, which had obvious gate leakage current [7,8]. Since the gate leakage cannot be ignored, the gate-direct-tunneling model had been included in the BSIM4 MOSFET SPICE model for circuit simulation [9]. In the highly integrated digital circuits, the gate leakage current contributes a significant off-state leakage to greatly increase the total power consumption [10–12]. In the analog circuits, the impacts of gate leakage include the limited current gain, mismatch, and noise [13]. Besides, the ESD protection scenarios also suffer the gate leakage issue, which causes large leakage current in the power-rail ESD clamp circuits [14–16].

The typical on-chip ESD protection scheme in a CMOS IC is illustrated in Fig. 2. The power-rail ESD clamp circuit is designed to provide a current discharging path during ESD stresses, and to be kept off under normal power-on conditions. The traditional design of the power-rail ESD clamp circuit is often consisted with an RC-based ESD-detection circuit to detect the ESD event and a huge ESD

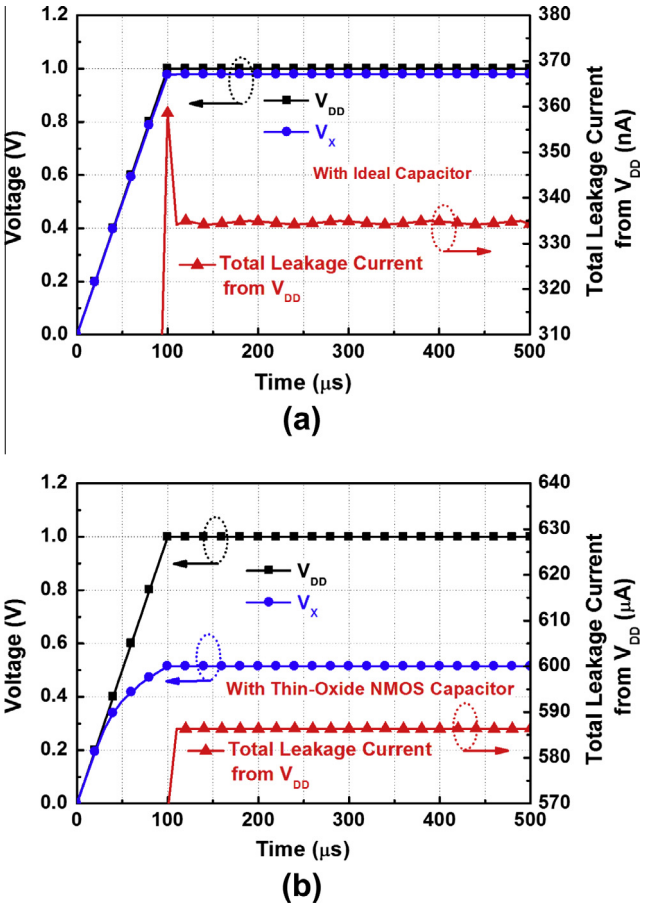

Fig. 3. Simulated transient waveforms of the ESD-detection circuit with (a) ideal capacitor and (b) thin-oxide NMOS capacitor under normal power-on conditions in a 65 nm CMOS process.

clamp device (M_{NESD}) to discharge ESD current. To effectively turn on the circuit during ESD stresses and to completely turn off the circuit under normal power-on conditions, the RC time constant in the ESD-detection circuit should be designed around microseconds (μs) [17]. With consideration of area efficiency and fabrication cost, the capacitor (C_1) in the ESD-detection circuit was often realized by the MOS capacitor. If such a traditional design is realized with the thin-oxide devices in nanoscale CMOS processes, the leaky MOS capacitor will cause serious leakage issue [14]. For example, due to the gate leakage current in the MOS

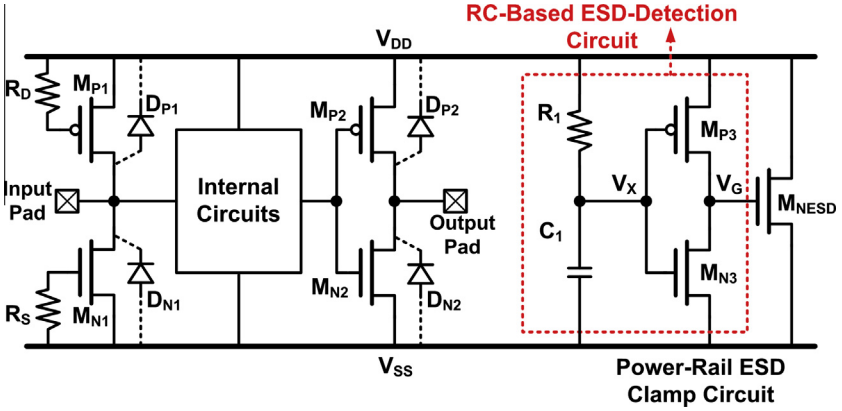

Fig. 2. Typical on-chip ESD protection scheme.

Table 1
Device dimensions used in ESD-detection circuits for HSPICE simulation.

Type	R_1	C_1	M_{P3} (W/L)	M_{N3} (W/L)
With ideal capacitor	100 kΩ	2 pF	$\frac{100\ \mu m}{0.15\ \mu m}$	$\frac{20\ \mu m}{0.15\ \mu m}$
With NMOS capacitor	100 kΩ	2 pF $\left(\frac{29\ \mu m}{28\ \mu m}\right)$	$\frac{100\ \mu m}{0.15\ \mu m}$	$\frac{20\ \mu m}{0.15\ \mu m}$

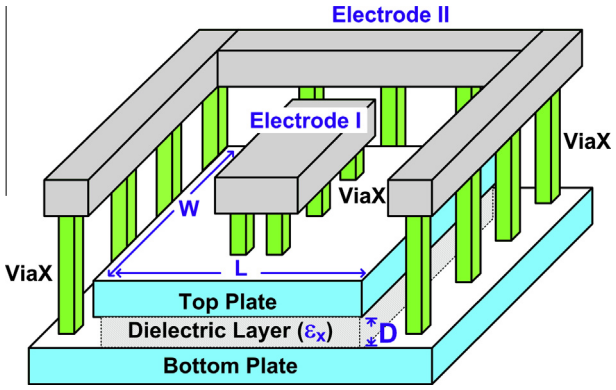

Fig. 4. Schematic of MIM capacitor.

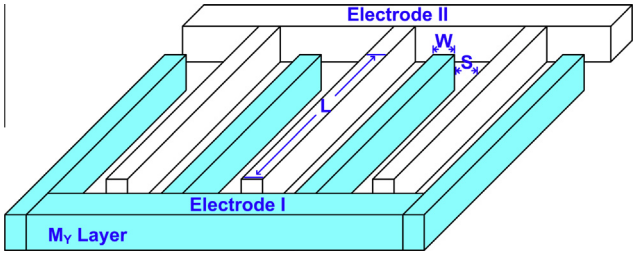

Fig. 5. Schematic of MOM capacitor.

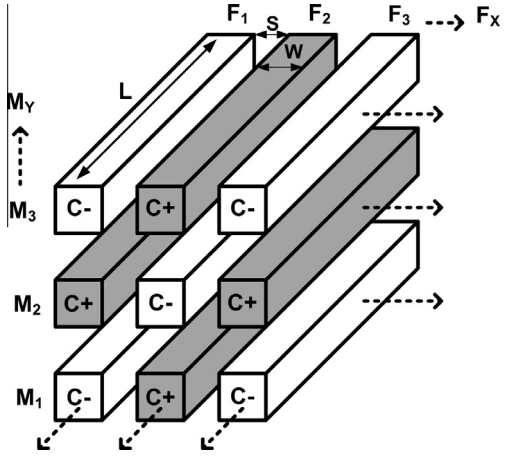

Fig. 6. MOM capacitor structure used in this work.

capacitor, the voltage at the node V_X cannot be fully charged to V_{DD} after power-on. Therefore, the PMOS M_{P3} in ESD-detection circuit cannot be fully turned off, which causes another leakage path through the inverter in the ESD-detection circuit. Consequently, the gate voltage (V_G) of M_{NESD} was not fully biased to V_{SS}. The partially turned-on M_{NESD} (which is usually designed with large device dimension to discharge ESD current) will conduct extra leakage current from V_{DD} to V_{SS} under normal circuit operating conditions. Fig. 3a and b shows the simulated results of ESD-detection circuits in a 65 nm CMOS process to observe the impact of gate leakage issue. The device dimensions used in the simulation are listed in Table 1. Without the gate leakage of an ideal capacitor in the

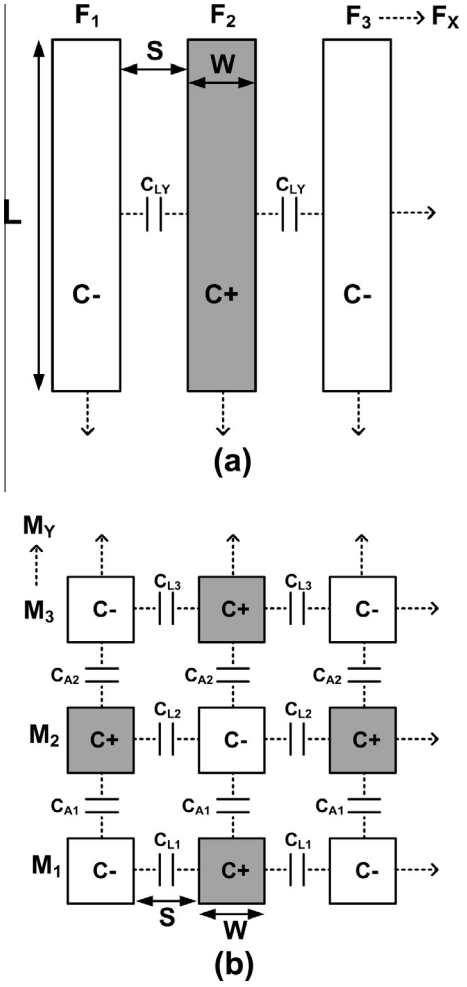

Fig. 7. MOM capacitor structure layout (a) top view and (b) cross-sectional view.

Table 2
Estimated layout area of capacitors with different capacitances in a 65 nm CMOS process.

Type	C_{eq} (pF)	M_Y	Area	C_{eq} per unit area (fF/μm^2)
MOM cap.	~1	3	~27 μm × 28 μm	~1.32
		4	~23 μm × 24 μm	~1.81
		5	~21 μm × 22 μm	~2.16
	~2	3	~36 μm × 37 μm	~1.50
		4	~32 μm × 33 μm	~1.89
		5	~29 μm × 30 μm	~2.30
	~5	3	~57 μm × 58 μm	~1.51
		4	~50 μm × 51 μm	~1.96
		5	~45 μm × 46 μm	~2.42
MIM cap.	~1		~25 μm × 25 μm	~1.60
	~2		~34 μm × 34 μm	~1.73
	~5		~52 μm × 52 μm	~1.85
MOS cap. (NMOS 1 V)	~1		~26 μm × 28 μm	~1.37
	~2		~34 μm × 37 μm	~1.59
	~5		~48 μm × 55 μm	~1.89

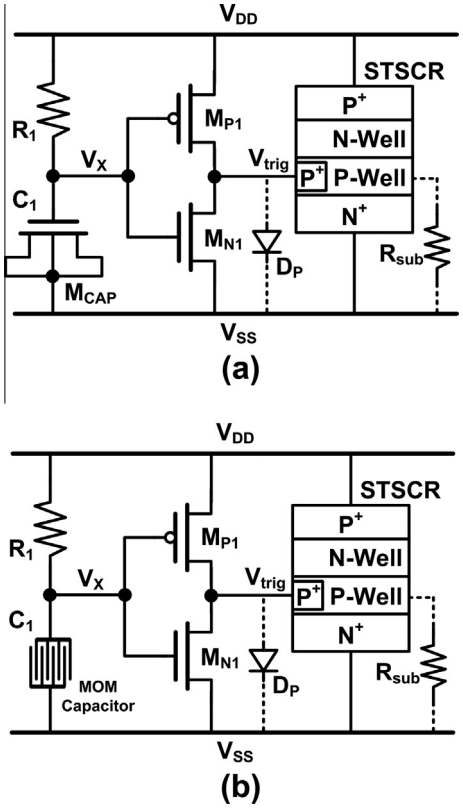

Fig. 8. RC-based power-rail ESD clamp circuit with (a) thin-oxide NMOS capacitor and (b) MOM capacitor.

Table 3
Device dimensions used in the power-rail ESD clamp circuits.

Type	R_1	C_1	M_{P3} (W/L)	M_{N3} (W/L)	STSCR (W/L)
With NMOS capacitor	100 kΩ	34 μm × 37 μm	$\frac{100\ \mu m}{0.15\ \mu m}$	$\frac{20\ \mu m}{0.15\ \mu m}$	$\frac{40\ \mu m}{7.8\ \mu m}$
With MOM capacitor	100 kΩ	36 μm × 37 μm	$\frac{100\ \mu m}{0.15\ \mu m}$	$\frac{20\ \mu m}{0.15\ \mu m}$	$\frac{40\ \mu m}{7.8\ \mu m}$

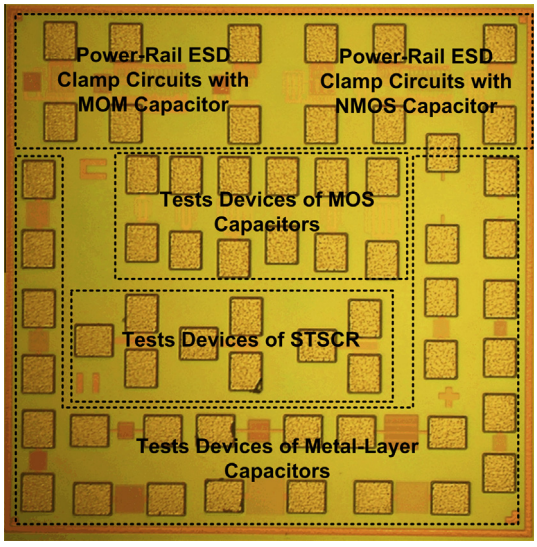

Fig. 9. Chip micrograph of the fabricated test devices and the power-rail ESD clamp circuits in a 65 nm CMOS process.

ESD-detection circuit, the terminal V_X can be biased to near the power-supply voltage (V_{DD}) of 1 V, as shown in Fig. 3a. The simulated overall leakage current from V_{DD} is only 335 nA at 25 °C. However, with the gate leakage of a thin-oxide NMOS capacitor in the ESD-detection circuit, the terminal V_X cannot be biased to V_{DD}, as shown in Fig. 3b. Thus, the simulated overall leakage current is increased up to 586 μA at 25 °C.

Although some circuit techniques had been reported to decrease the impact from the gate leakage current of MOS capacitor [15,16], the effective capacitance was reduced to decrease the trigger ability under ESD stress. To keep enough trigger ability, more layout area of MOS capacitor will be required. Thus, if the MOS capacitor in the traditional RC-based ESD-detection circuit was replaced by another capacitor which has no gate leakage issue, the traditional RC-based ESD-detection circuit can be still useful in nanoscale CMOS processes.

3. Metal-layer capacitors

Two metal-layer capacitors, MIM and MOM capacitors, are widely utilized in CMOS processes. With the parallel-plate structure, the MIM capacitor is composed of two metal plates and a dielectric layer between them, as shown in Fig. 4. In order to realize the structure with a shorter distance (D) and a different dielectric material (ε_X) to enhance the capacitance density, the fabrication of MIM capacitor needs additional fabrication masks to define the top and bottom metal plates. Different to the MIM capacitor, the MOM capacitor is realized through the metal interconnections, as shown in Fig. 5. Ideally, every pair of two metal lines can form the MOM capacitor. In the early generation of CMOS processes, the lateral and vertical intervals between metal layers were not close enough, the capacitance density of MOM capacitor was very low. However, with the dimension shrinkage in advanced CMOS processes, the parasitic capacitance between metal interconnections is increased significantly. For example, in a 0.25 μm CMOS technology, the minimum width (W) and space (S) of metal layers is 0.4 μm. When the technology shrank to 65 nm, the minimum W and S of metal layers were decreased to 0.1 μm. Besides, the MOM capacitor can be stacked with several metal layers (M_Y) to increase the capacitance density in advanced CMOS technology.

Various types of MOM capacitors have been developed with different configurations to increase the horizontal or vertical surface area [18–22]. The structure of MOM capacitor used in this work is shown in Fig. 6 [20]. In the same metal layer, the lateral capacitance (C_{LY}) between the adjacent metal lines is shown in Fig. 7a. In different metal layers, the vertical capacitance ($C_{AY\text{-}1}$) is shown

Table 4
Measured capacitances of MIM and MOM capacitors under the bias voltage of −1 V, 0 V, and 1 V (at reference frequency of 100 kHz).

Type	C_{eq} (pF)	$C_{Measured}$ $V_B = -1$ V	$V_B = 0$ V	$V_B = 1$ V	M_Y	Area	$C_{Measured}$ per unit area (fF/μm²)
MOM cap.	~1	~1.14 pF	~1.14 pF	~1.14 pF	3	~27 μm × 28 μm	~1.51
		~1.15 pF	~1.15 pF	~1.15 pF	4	~23 μm × 24 μm	~2.08
		~1.17 pF	~1.17 pF	~1.17 pF	5	~21 μm × 22 μm	~2.53
	~2	~2.27 pF	~2.27 pF	~2.27 pF	3	~36 μm × 37 μm	~1.70
		~2.30 pF	~2.30 pF	~2.30 pF	4	~32 μm × 33 μm	~2.18
		~2.35 pF	~2.35 pF	~2.35 pF	5	~29 μm × 30 μm	~2.70
	~5	~5.71 pF	~5.71 pF	~5.71 pF	3	~57 μm × 58 μm	~1.73
		~5.72 pF	~5.72 pF	~5.72 pF	4	~50 μm × 51 μm	~2.24
		~5.74 pF	~5.74 pF	~5.74 pF	5	~45 μm × 46 μm	~2.77
MIM cap.	~1	~0.997 pF	~0.997 pF	~0.997 pF		~25 μm × 25 μm	~1.60
	~2	~1.973 pF	~1.973 pF	~1.973 pF		~34 μm × 34 μm	~1.71
	~5	~4.990 pF	~4.990 pF	~4.990 pF		~52 μm × 52 μm	~1.85

Table 5
Measured capacitances of MIM and MOM capacitors under different reference frequencies.

Type	C_{eq} (pF)	$C_{Measured}$			M_Y	Area	$C_{Measured}$ per unit area	
		@100 kHz	@500 kHz	Variation (%)			@100 kHz (fF/μm^2)	@500 kHz (fF/μm^2)
MOM cap.	~1	~1.14 pF	~1.13 pF	~0.88	3	~27 μm × 28 μm	~1.51	~1.49
		~1.15 pF	~1.14 pF	~0.87	4	~23 μm × 24 μm	~2.08	~2.07
		~1.17 pF	~1.16 pF	~0.85	5	~21 μm × 22 μm	~2.53	~2.51
	~2	~2.27 pF	~2.25 pF	~0.85	3	~36 μm × 37 μm	~1.70	~1.69
		~2.30 pF	~2.28 pF	~0.87	4	~32 μm × 33 μm	~2.18	~2.16
		~2.35 pF	~2.33 pF	~0.85	5	~29 μm × 30 μm	~2.70	~2.68
	~5	~5.71 pF	~5.67 pF	~0.70	3	~57 μm × 58 μm	~1.73	~1.72
		~5.72 pF	~5.68 pF	~0.70	4	~50 μm × 51 μm	~2.24	~2.23
		~5.74 pF	~5.69 pF	~0.85	5	~45 μm × 46 μm	~2.77	~2.75
MIM cap.	~1	~0.997 pF	~0.996 pF	~0.10		~25 μm × 25 μm	~1.60	~1.59
	~2	~1.973 pF	~1.972 pF	~0.05		~34 μm × 34 μm	~1.71	~1.71
	~5	~4.990 pF	~4.986 pF	~0.08		~52 μm × 52 μm	~1.85	~1.84

in Fig. 7b. With this kind of arrangement, the MOM capacitor takes the advantage of both the lateral and vertical fields to extend the capacitance density. The capacitance could be estimated as:

$$C_{Lateral} = L \times (F_X - 1) \times C_{LY},$$

$$C_{Vertical} = L \times F_X \times C_{AY-1}, \text{ and}$$

$$C_{Total} = C_{Lateral} + C_{Vertical}. \quad (1)$$

The F_X is finger numbers. L is metal length. C_{LY} is coupling capacitance per unit length between the metal lines in the same metal layer. The C_{AY-1} is area capacitance per unit length between metal layers. Table 2 shows the estimated results of device layout area with different capacitors. With more metal layers stacked, the MOM capacitor can have the smallest area to achieve the same desired capacitance.

4. Experimental results

To investigate the capacitance of different metal-layer capacitors, the test devices of MIM and MOM capacitors had been fabricated in the silicon chip with a 65 nm CMOS process. In addition, for investigating gate leakage issue of thin-oxide MOS capacitor, the test devices of stand-alone PMOS and NMOS capacitors were also included in the test chip. Moreover, to investigate the impact of gate leakage issue in RC-based ESD-detection circuit, power-rail ESD clamp circuits with different capacitors were implemented in the test chip. With the same capacitance of MIM and MOM capacitor realized in power-rail ESD clamp circuit, circuit behaviors would be almost identical under the same RC time constant. For emphasizing the impact of gate leakage issue, only MOM capacitor was composed in the power-rail ESD clamp circuit to observe the gate leakage issue as compared to the thin-oxide MOS capacitor. Thus, two power-rail ESD clamp circuits with thin-oxide NMOS capacitor and MOM capacitor were fabricated in the test chip as shown in Fig. 8a and b, respectively.

All device dimensions used in the power-rail ESD clamp circuits are listed in Table 3. With a capacitance of 2 pF, the layout area of MOM capacitor realized with 3 metal layers is 36 μm × 37 μm. The thin-oxide NMOS capacitor was implemented with a similar layout area of 34 μm × 37 μm (channel width W_C = 29 μm and channel length L_C = 28 μm). Except the capacitor, all devices used in these two circuits have the identical device dimensions. Instead of large NMOS device (M_{NESD}), the substrate-triggered silicon-controlled rectifier (STSCR) was used as the ESD clamp device, because SCR had been proven to have the highest ESD robustness under the smallest silicon area [23]. Without the thin gate oxide in the P–N–P–N structure of SCR, SCR is free from the gate leakage issue. The chip micrograph of test devices and the fabricated power-rail ESD clamp circuits is shown in Fig. 9.

4.1. Measured capacitance of metal-layer capacitors

Table 4 shows the measured capacitance of two metal-layer capacitors under the bias voltage (V_B) at −1 V, 0 V, and 1 V (at a reference frequency of 100 kHz and temperature of 25 °C). Even the temperature was heated to 125 °C, each capacitor has the stable

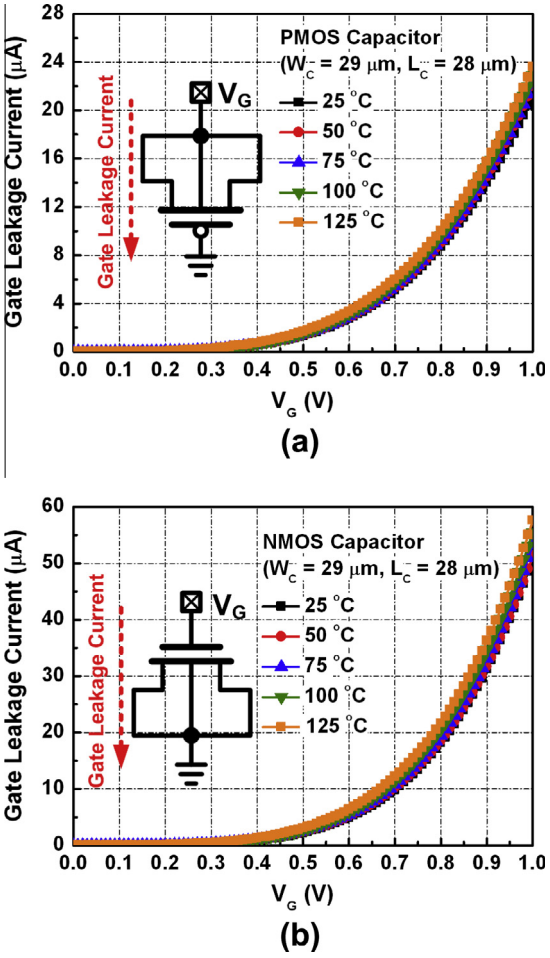

Fig. 10. Measured gate leakage current of the thin-oxide (a) PMOS and (b) NMOS capacitor in a 65 nm CMOS process under different temperatures.

Table 6
Measured leakage currents amount fabricated capacitors under different temperatures.

Leakage current at V_G = 1 V	25 °C	50 °C	75 °C	100 °C	125 °C
NMOS cap. (~2 pF) (layout area of 34 μm × 37 μm)	50.9 μA	51.3 μA	53.3 μA	55.5 μA	57.6 μA
PMOS cap. (~2 pF) (layout area of 34 μm × 37 μm)	21.2 μA	22.0 μA	22.2 μA	22.9 μA	23.6 μA
MIM cap. (~2 pF) (layout area of 34 μm × 34 μm)	<20 pA	<20 pA	<20 pA	<20 pA	<20 pA
MOM cap. (~2 pF) (layout area of 36 μm × 37 μm)	<20 pA	<20 pA	<20 pA	<20 pA	<20 pA

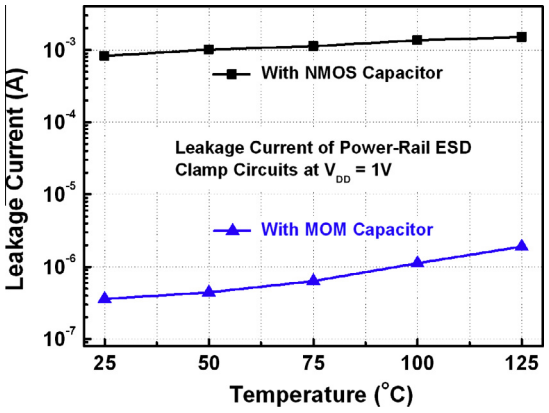

Fig. 11. Measured leakage currents between two fabricated power-rail ESD clamp circuits under different temperatures.

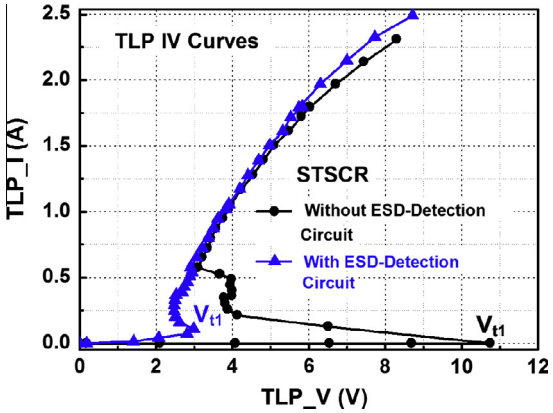

Fig. 12. TLP-measured *I–V* characteristics of the STSCR with and without the ESD-detection circuit.

capacitance as shown in Table 4. However, with the different reference frequencies in the measurement, the capacitance variations of two capacitors are quite different. The measured capacitances under the reference frequencies of 100 kHz and 500 kHz at 0 V bias are summarized in Table 5. As shown in Table 5, more capacitance variation is observed in MOM capacitors when the frequency is increased. The maximum variation in MOM capacitor is 0.88%, but the variation in MIM capacitor is only 0.1%. In addition to the capacitor's structure, the most difference is the dielectric layer within two capacitors. Due to the MOM capacitor is realized from the metal interconnects, the dielectric layers are mainly formed by SiO_2 and low-*k* materials [24]. But, in the MIM capacitor, the dielectric layer was often implemented with the high-*k* materials to increase the capacitance density [25]. Some relative studies had been reported that the frequency dependencies were various with different materials to cause the capacitance loss [2,26]. However, the characteristics of different materials were not further analyzed in this work.

Besides, compared to the evaluated capacitances, more capacitances are measured in MOM capacitors. Thus, the accuracy of capacitance estimation (1) in MOM capacitor should be further improved. However, the occupied area of MOM capacitor actually can be the smallest when more metal layers are used.

4.2. Leakage current

Fig. 10a and b shows the measured gate leakage currents of the stand-alone thin-oxide (1 V) PMOS and NMOS capacitors (W_C = 29 μm and L_C = 28 μm) with the gate oxide thickness of ~20 Å in a 65 nm CMOS process. Under 1 V bias across the MOS capacitor, the gate leakage currents of PMOS and NMOS capacitors at 25 °C are 21.2 μA and 50.9 μA, respectively. The leakage currents among the fabricated capacitors under 1 V bias and different temperatures are summarized in Table 6. With such huge leakage current through the MOS capacitor, the thin-oxide MOS capacitor is no longer suitable for circuit applications in the 65 nm CMOS process. On the contrary, without the thin-oxide structure in MIM and MOM capacitors, these two capacitors' leakage currents are quite low (<20 pA). The leakage currents between two power-rail ESD clamp circuits under different temperatures with V_{DD} of 1 V are compared in Fig. 11. The leakage currents are also summarized in Table 7. Comparing with the leakage current of the stand-alone thin-oxide NMOS capacitor, much higher leakage current (828 μA at 25 °C) is observed in the power-rail ESD clamp circuit with NMOS capacitor, which indicates that the leaky MOS capacitor certainly causes extra leakage paths in the ESD-detection circuit. On the contrary, with almost no leakage current in MOM capacitor, the power-rail ESD clamp circuit with MOM capacitor has the lowest leakage current of only 358 nA. The total leakage current of the power-rail ESD clamp circuit with MOM capacitor is three orders smaller than that with NMOS capacitor from low temperature to high temperature.

4.3. ESD robustness

To investigate the turn-on behavior of the ESD clamp device with ESD-detection circuit during ESD event, the transmission line pulse (TLP) with 100 ns pulse width and 10 ns rise time was used to measure the second breakdown current (I_{t2}) of ESD protection circuits. The TLP-measured *I–V* characteristics of the STSCR with

Table 7
Measured leakage currents and ESD robustness of the power-rail ESD clamp circuits.

Circuit type	Leakage current at V_{DD} = 1 V					ESD robustness	
	25 °C	50 °C	75 °C	100 °C	125 °C	HBM	MM
With NMOS capacitor	828 μA	1.01 mA	1.13 mA	1.36 mA	1.51 mA	4 kV	350 V
With MOM capacitor	358 nA	441 nA	633 nA	1.12 μA	1.91 μA	4 kV	350 V

Table 8
The percentage of capacitance variation within the estimations.

M_Y		3	4	5	3	4	5	3	4	5
$C_{Measured}$		1.14 pF	1.15 pF	1.17 pF	2.27 pF	2.30 pF	2.35 pF	5.71 pF	5.72 pF	5.74 pF
Capacitance variation	In (1)	12.3%	13%	14.5%	11.9%	13%	14.9%	12.4%	12.6%	12.9%
	In (2)	1.8%	2.6%	3.4%	2.6%	2.2%	2.6%	5.8%	4.8%	4.2%

and without the ESD-detection circuit are shown in Fig. 12. Without any trigger signal, the original trigger voltage (V_{t1}) of stand-alone STSCR (width = 40 μm) device is 10.7 V, and the I_{t2} is 2.3 A. With the trigger signal from ESD-detection circuit, the V_{t1} of the STSCR device is significantly reduced to 3 V and the I_{t2} is 2.5 A. The lower V_{t1} of the power-rail ESD clamp circuit ensures its effective ESD protection capability. In addition, the holding voltage of STSCR shown in Fig. 12 is ~2.5 V, so the proposed power-rail ESD clamp circuit is free from latchup issue in the CMOS ICs with V_{DD} of 1 V. The human-body-model (HBM) and machine-model (MM) ESD levels of these two power-rail ESD clamp circuits are evaluated by the ESD simulator. Measured ESD levels are listed in Table 7. The failure criterion is defined as 30% shift in the leakage current under 1 V V_{DD} bias. The power-rail ESD clamp circuit with STSCR of only 40 μm width can achieve ESD robustness of 4 kV in HBM and 350 V in MM, respectively.

5. Discussion

Comparing the evaluated results of MOM capacitor, more capacitance is observed in the measured results (as listed in Table 4). In (1), each finger's edge capacitance was ignored. To obtain more accurate capacitance in this structure, the capacitance estimation of MOM capacitor should be fixed in the following equations, where C_{FE} is the capacitance from all finger's edge. Thus, the maximum capacitance variation is decreased from 14.9% to 5.8%, as shown in Table 8.

$$C_{Lateral} = L \times (F_X - 1) \times C_{LY},$$

$$C_{Vertical} = L \times F_X \times C_{AY-1},$$

$$C_{FE} = F_X \times M_Y \times C_{Edge}, \text{ and}$$

$$C_{Total} = C_{Lateral} + C_{Vertical} + C_{FE}. \quad (2)$$

6. Conclusion

Two metal-layer capacitors, MIM and MOM capacitors, have been investigated in this work with a 65 nm CMOS process. With more metal layers utilized, the occupied silicon area of MOM capacitor can be smaller than MIM capacitor under the same capacitance. Although the MIM capacitor was reported to have the best characteristics in some CMOS processes, it increases the fabrication cost due to the additional masks. Different from the structure of MIM capacitor, the MOM capacitor can be easily realized by the metal interconnections. Without additional mask, the integration complexity and fabrication cost for MOM capacitor are not increased. With the advantages of higher capacitance density and lower fabrication cost, the MOM capacitor is more suitable than the MIM capacitor for general circuit applications in the nanoscale CMOS processes.

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