A Novel Control Strategy of Circulating Currents in Paralleled Single-Phase Boost Converters With Different Power Sharing for Microgrid Applications

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***Abstract*—In this paper, analysis of circulating currents of paralleled single-phase boost converter systems is presented. The dc loop and ac loop circulating currents are clearly explained. In order to eliminate the dc loop circulating currents and reduce switching losses, a simplified pulsewidth modulation strategy is adopted in a paralleled single-phase boost converter. Based on the analysis of circulating currents, common-mode circulating current (CMCC) and differential-mode circulating current (DMCC) are defined. Then, CMCC and DMCC compensators are proposed in a centralized control scheme to reduce the common-mode and differential-mode circulating currents in a parallel system operated in both rectifier and inverter modes with different power sharing for microgrid applications. Converter-paralleled system stability analysis is also presented. Finally, a prototype system is constructed to facilitate the theoretical results as verification. From the experimental results, the proposed control scheme can indeed reduce the circulating currents under equal and/or different power rating conditions in the parallel system.**

***Index Terms*—AC/DC converter, circulating currents, common mode, differential mode, microgrid.**

I. Introduction

RENEWABLE energy processes require high-power converter systems built with a parallel structure [1], [2], [4], [5]. The modularized ac–dc converter with parallel structure to increase system capacity is shown in Fig. 1. The literature [3]–[5] discussed that paralleling converters is more desirable than paralleling the active switch devices. However, since the converters are usually designed individually, the circulating currents problem arises when they are operated in parallel [1], [6]–[9]. The circulating currents result in line-current distortion and unbalanced load sharing. The overall system performance will be degraded.

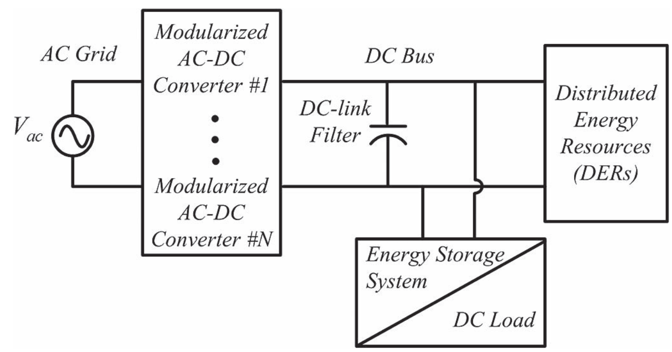

Fig. 1. Modularized ac–dc converter with paralleled structure in the microgrid system.

Traditionally, the isolation approach is a simple method to prevent circulating currents. For example, adopting separate dc or ac sources [1], [10] or an isolation transformer at the ac grid [11], [12]. In such a method, the overall parallel system is expensive and bulky, making this approach impractical. In addition to the isolation approach, there are other methods to deal with the circulating-current problem in the converter-paralleled system. For example, an interphase reactor is utilized to provide high impedance [13], [14] to reduce the circulating current. However, the reactor cannot provide high impedance at low frequency, so that the low-frequency circulating currents cannot be reduced. A space-vector modulation without using zero vectors is used to eliminate the pure zero-sequence current for parallel operation [22]. Furthermore, a new control variable [7] to adjust the zero-vector duration is proposed to suppress circulating currents. However, only dc loop circulating currents are considered, and ac loop circulating currents still exist. A synchronized control scheme has been also used to reduce the circulating currents. This approach basically treats paralleled converters as one converter [12], [15]–[19]. When more converters are connected in parallel, the system becomes complex and is usually difficult to design, particularly when different kinds of converters are used.

Until now, most of the discussions focused on the equal power rating condition [1]–[3], where each converter in the parallel system operates with the same output power. In [20], a coordinate control scheme considering different power rating conditions was proposed. Table I shows the categorization of equal/different power rating conditions in the existing literature.

Manuscript received January 24, 2013; revised June 1, 2013; accepted July 1, 2013. Date of publication November 8, 2013; date of current version March 17, 2014. Paper 2012-ESC-750.R1, presented at the 2013 IEEE/IAS Industrial and Commercial Power Systems Technical Conference, Stone Mountain, GA, USA, April 30–May 3, and approved for publication in the IEEE Transactions on Industry Applications by the Energy Systems Committee of the IEEE Industry Applications Society. This work was supported by the National Science Council of Taiwan under Grant NSC 102-2221-E-346-002 and Grant NSC 103-ET-E-346-001–ET.

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Digital Object Identifier 10.1109/TIA.2013.2289995

TABLE I
LITERATURE CATEGORY OF EQUAL/DIFFERENT POWER RATING OPERATION IN THE PARALLEL SYSTEM

Converter System	*Three phase*	*Single phase*
Equal power rating	[6], [7]	[8]
Different power rating	[20]	*Proposed scheme*

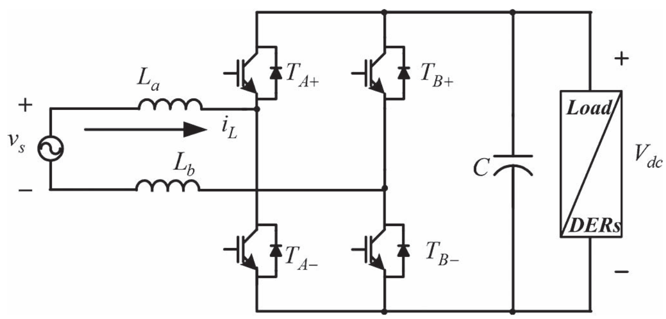

Fig. 2. Single-phase bidirectional boost converter.

TABLE II
SWITCHING COMBINATION OF A SINGLE-PHASE BIDIRECTIONAL BOOST CONVERTER OPERATED IN THE RECTIFIER MODE

	Status	T_{A+}	T_{A-}	T_{B+}	T_{B-}	Inductor status
$v_s > 0$	A	**OFF**	**OFF**	**ON**	**OFF**	$v_{La}, v_{Lb} > 0$
	B	**OFF**	**ON**	**OFF**	**OFF**	
	E	**OFF**	**OFF**	**OFF**	**OFF**	$v_{La}, v_{Lb} < 0$
$v_s < 0$	C	**ON**	**OFF**	**OFF**	**OFF**	$v_{La}, v_{Lb} < 0$
	D	**OFF**	**OFF**	**OFF**	**ON**	
	E	**OFF**	**OFF**	**OFF**	**OFF**	$v_{La}, v_{Lb} > 0$

TABLE III
SWITCHING COMBINATION OF A SINGLE-PHASE BIDIRECTIONAL BOOST CONVERTER OPERATED IN THE INVERTER MODE

	Status	T_{A+}	T_{A-}	T_{B+}	T_{B-}	Inductor status
$v_s > 0$	F	**ON**	**OFF**	**OFF**	**OFF**	$v_{La}, v_{Lb} > 0$
	G	**OFF**	**OFF**	**OFF**	**ON**	
	H	**ON**	**OFF**	**OFF**	**ON**	$v_{La}, v_{Lb} < 0$
$v_s < 0$	I	**OFF**	**ON**	**OFF**	**OFF**	$v_{La}, v_{Lb} < 0$
	J	**OFF**	**OFF**	**ON**	**OFF**	
	K	**OFF**	**ON**	**ON**	**OFF**	$v_{La}, v_{Lb} > 0$

II. CIRCULATING CURRENTS OF PARALLEL SYSTEMS

A. Single-Phase Boost Converter Operation

A single-phase boost converter is shown in Fig. 2. In order to reduce circulating-current loops in the parallel system, a simplified pulsewidth modulation (PWM) strategy is adopted in each converter. The simplified PWM switching combination is shown in Tables II and III corresponding to the rectifier and inverter modes, respectively. To achieve power factor correction, one can choose some available current increasing/decreasing statuses for the input inductors during grid voltage $v_s > 0$ or $v_s < 0$.

B. DC and AC Circulating-Current Loops

In order to understand the circulating-current problem, consider two paralleled single-phase boost converters, as shown in Fig. 3, with line inductors at each phase in each converter. When the switches T_{A1+}, T_{B1+}, T_{A2+}, and T_{B2-} are turned on, one can find that two different kinds of circulating-current loops exist, i.e., dc and ac circulating-current loops. In this condition, the dc and ac circulating-current loops are described as follows:

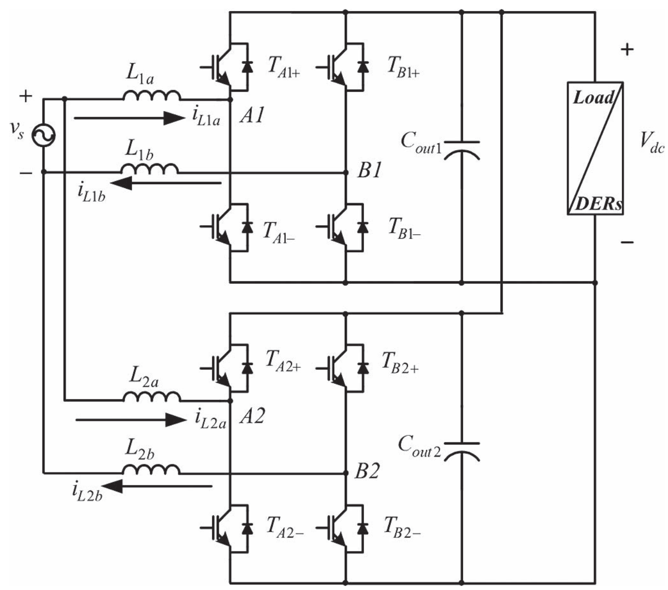

Fig. 3. Two paralleled single-phase bidirectional boost converters with inductors at each phase in each converter.

$$\text{dc loop}: V_{\mathrm{dc}}^{+} \rightarrow T_{B1+} \rightarrow B1 \rightarrow v_s^{-} \rightarrow B2 \rightarrow T_{B2-} \rightarrow V_{\mathrm{dc}}^{-}$$

$$\text{ac loop}: v_s^{+} \rightarrow A2 \rightarrow T_{A2+} \rightarrow V_{\mathrm{dc}}^{+} \rightarrow T_{B1+} \rightarrow B1 \rightarrow v_s^{-}$$

where the dc circulating-current loop is defined as the current loop caused by the output voltage V_{dc} without passing through V_s. The ac circulating-current loop is defined as the current loop caused by the input voltage V_s without passing through V_{dc}. Both the dc and ac circulating-current loops are undesired loops in the paralleled converter system. The switching constraint method [21] is proposed to eliminate the dc circulating-current loop and provide control for the ac circulating-current loop to prevent circulating currents. However, the switching constraint method only takes effect under the equal power rating condition. If the paralleled converters are operated under different power rating distributions, the switching constraint method is not valid for preventing circulating currents.

This paper presents a novel common-mode and differential-mode circulating-current control strategy. The proposed control strategy can reduce the circulating currents in a paralleled converter system regardless whether the system is operated in equal power rating or different power rating conditions.

III. PROPOSED CONTROL SCHEME

The circulating current can be divided into two different components, i.e., common-mode and differential-mode circulating currents. The common-mode circulating current is defined as the difference between leg A and leg B line currents in the individual converter as follows:

$$i_{\mathrm{cmcc}\_x} = i_{Lxa} - i_{Lxb} \quad x \in \{1, 2, 3, \ldots, n\}. \tag{1}$$

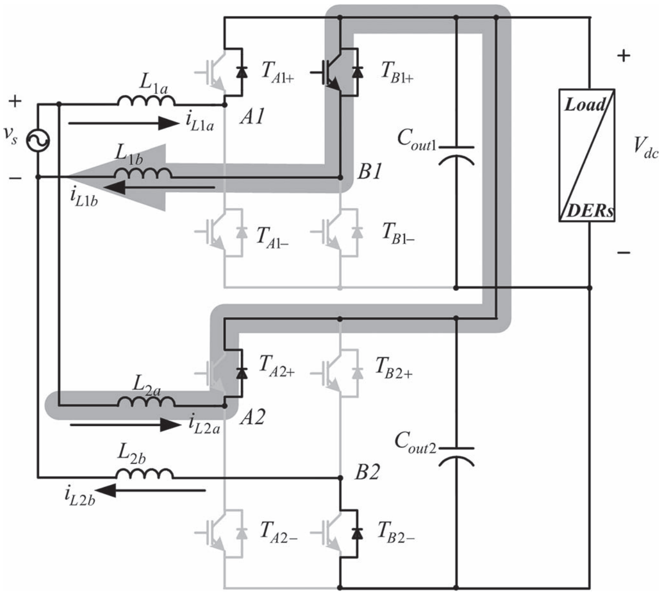

Fig. 4. Two paralleled single-phase boost converters operated in status (A, E).

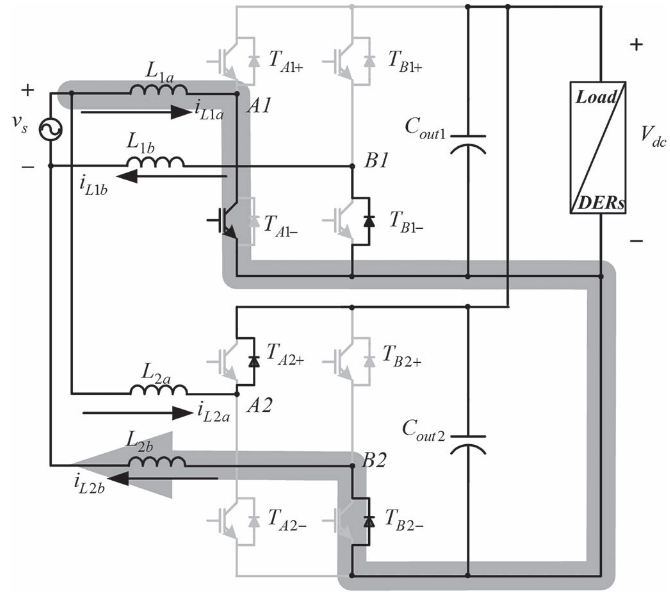

Fig. 5. Two paralleled single-phase boost converters operated in status (B, E).

Next, the differential-mode circulating current $i_{\text{dmcc\_}jm}$ is defined as the difference of line currents connected to leg A between the jth converter and the mth converter, i.e.,

$$i_{\text{dmcc\_}jm} = \sigma_m i_{Lja} - \sigma_j i_{Lma} \qquad j, m \in \{1, 2, 3, \ldots, n\}, \quad j \neq m \quad (2)$$

where σ_x is the distribution factor $(0 \leq \sigma_x \leq 1)$ and is defined as

$$\sigma_x = \frac{P_x}{\sum_{k=1}^{n} P_k} = \frac{P_x}{P_{\text{total}}} \quad x \in \{1, 2, 3, \ldots, n\} \quad (3)$$

where P_{total} is the total output power of the parallel system, and P_x is the output power of the xth converter.

A common-mode controller and a differential-mode controller are proposed based on the common-mode and differential-mode circulating currents as follows.

A. Common-Mode Controller

A simple explanation is given to explain how to eliminate the common-mode circulating currents as follows. The paralleled system is operated in status (A, E), as shown in Fig. 4. The common-mode circulating current $i_{\text{cmcc\_1}} < 0$ due to $i_{L1a} < i_{L1b}$. To reduce the common-mode circulating current in converter 1, the switching signals of converter 1 are changed from status A to status B, which makes the common-mode circulating current direction in the ac loop change from counterclockwise to clockwise, as shown in Fig. 5. The switching signals that reduce the common-mode circulating currents are summarized in Tables IV and V.

The common-mode circulating-current (CMCC) controller is proposed to adjust the line current in each converter in the parallel system. The CMCC control scheme in the parallel converter system is shown in Fig. 6. The detailed switching signal generator block diagram is shown in Fig. 7, and the CMCC controller is shown in Fig. 8.

TABLE IV
SWITCHING SIGNALS CORRESPONDING TO DIFFERENT KINDS OF COMMON-MODE CIRCULATING-CURRENT CONDITIONS IN PARALLEL SYSTEM OPERATED IN RECTIFIER MODE

Condition	$i_{cmcc\_x} > 0$		$i_{cmcc\_x} < 0$	
V_{cont_x}	$>V_{tri\_x}$	$<V_{tri\_x}$	$>V_{tri\_x}$	$<V_{tri\_x}$
$V_s > 0$	A	E	B	E
$V_s < 0$	E	C	E	D

Note: V_{cont_x} is the control signal and V_{tri_x} is the triangular carrier signal of x-th converter.

TABLE V
SWITCHING SIGNALS CORRESPONDING TO DIFFERENT KINDS OF COMMON-MODE CIRCULATING-CURRENT CONDITIONS IN PARALLEL SYSTEM OPERATED IN INVERTER MODE

Condition	$i_{cmcc\_x} > 0$		$i_{cmcc\_x} < 0$	
V_{cont_x}	$>V_{tri\_x}$	$<V_{tri\_x}$	$>V_{tri\_x}$	$<V_{tri\_x}$
$V_s > 0$	F	H	G	H
$V_s < 0$	K	J	K	I

Signal $CCRSx$ behavior corresponding to v_s during a cycle period is shown in Fig. 9. The CMCC controller makes the signal $CCRSx$ to be 1 at most of the time in the $v_s > 0$ period and 0 at most of the time in the $v_s < 0$ period. The controller allows the $CCRSx$ signal to become 0 at the $v_s > 0$ period to cancel the common-mode circulating current. It also allows the $CCRSx$ signal to become 1 at the $v_s < 0$ period to cancel the common-mode circulating current.

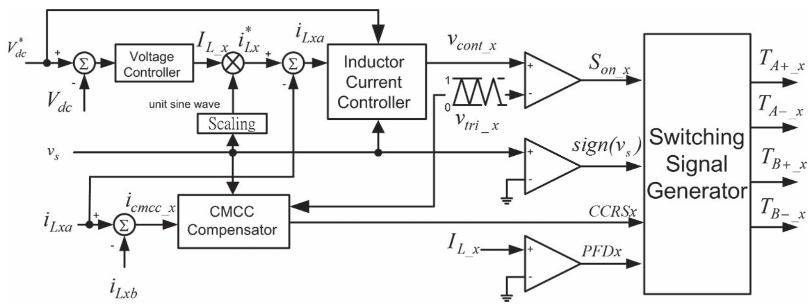

Fig. 6. Control scheme of the CMCC controller in the parallel converter system.

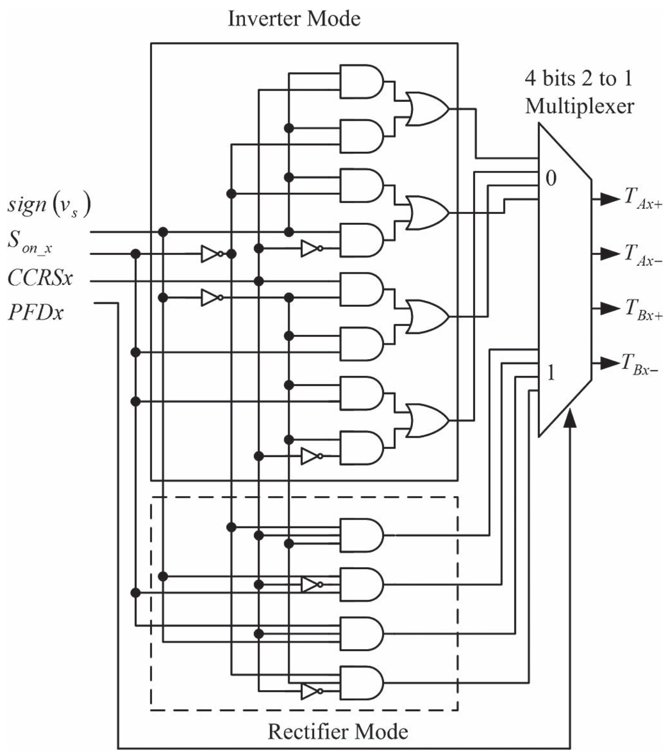

Fig. 7. Detailed subblock diagram of the switching signal generator.

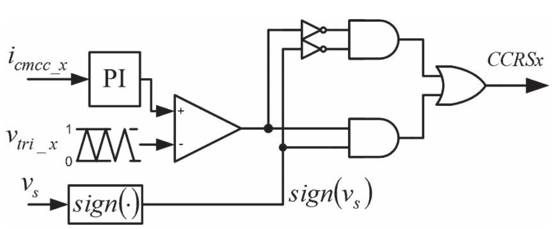

Fig. 8. Construction of CMCC controller.

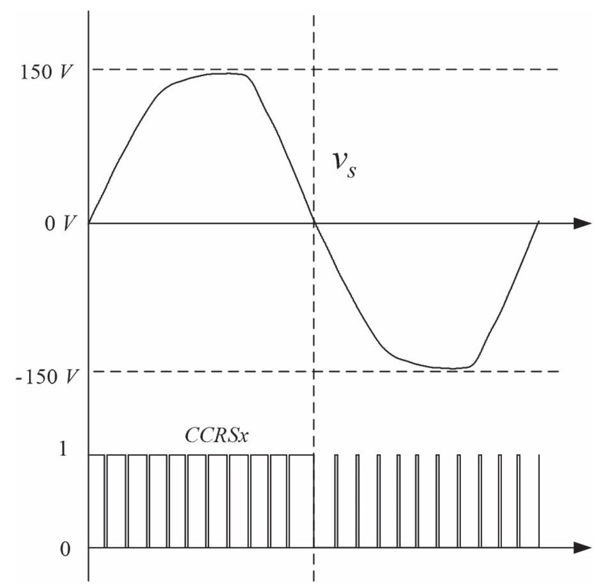

Fig. 9. Behavior of signal $CCRSx$ corresponding to V_s.

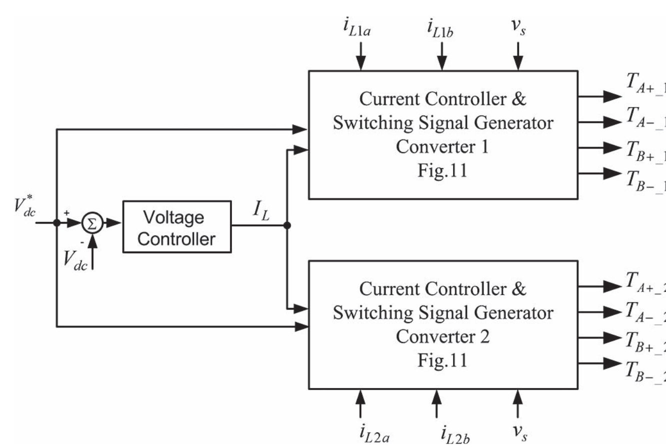

Fig. 10. Centralized control scheme of the parallel system.

B. Differential-Mode Controller

Due to different paralleled converter switching timing, the differential-mode circulating currents will exist leading to unbalanced load sharing. A centralized controller scheme is developed to deal with this problem. The centralized controller is easily constructed based on the proposed CMCC controller, as shown in Figs. 10 and 11.

In the centralized control scheme, a voltage controller is used (see Fig. 10), and the current command I_L generated by the voltage controller is sent to the current controller modules of each converter. By utilizing the distribution factor σ_x $(0 \leq \sigma_x \leq 1)$ defined in (3), the current sharing can be easily obtained by multiplying the current command I_L and distribution factor σ_x, as shown in Fig. 11.

Although the power ratings of the two converters in the parallel system are not the same, the common-mode and differential-mode circulating currents will be simultaneously reduced in the proposed circulating-current control strategy.

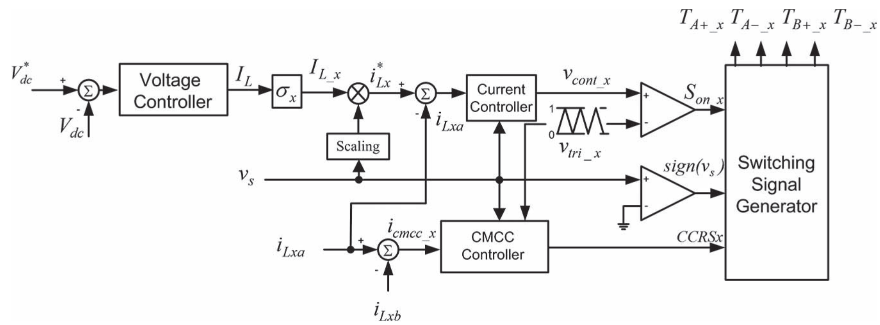

Fig. 11. Construction of DMCC and CMCC controller of each converter in the parallel system.

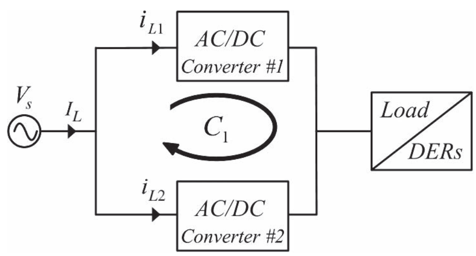

Fig. 12. Two paralleled converter system.

C. Stability Analysis

In order to understand the influence of circulating currents on the converter-paralleled system, consider the model for one converter.

1) Modeling of a Single-Phase Bidirectional Boost Converter: From the simplified PWM and switching combination as listed in Tables II and III, the ac line current of a single-phase bidirectional boost converter is controlled in the charge and discharge statuses. Using Kirchhoff's voltage law in Fig. 2, one can obtain two equations corresponding to the charge and discharge statuses as follows:

$$v_s = L_a \frac{d}{dt} i_L + R_a i_L + V_o + L_b \frac{d}{dt} i_L + R_b i_L \tag{4}$$

$$v_s = L_a \frac{d}{dt} i_L + R_a i_L + 0 + L_b \frac{d}{dt} i_L + R_b i_L \tag{5}$$

where L_j and R_j are the inductance and equivalent series resistances (ESRs) of the jth leg in the converter, respectively. $j \in \{a, b\}$. Assume D is the duty-ratio function of the active switch for adjusting the inductor charge and discharge status. By introducing the state-space averaged technique, the state-space averaged equation for a single-phase bidirectional boost converter can be derived as follows:

$$v_s = (pL_a + R_a)i_L + (pL_b + R_b)i_L + DV_o \tag{6}$$

where p is the differentiation operator.

2) Stability of the Paralleled System: For simplification, consider the block diagram of two paralleled converters, as shown in Fig. 12. Assume that each converter is well-designed, and the inductance with the ESR of each converter is the same. According to the aforementioned single-phase boost converter model, one can express the state-averaged equations for converters 1 and 2, respectively, as follows:

$$v_s = (pL_a + R_a)i_{L1} + (pL_b + R_b)i_{L1} + D_1 V_o \tag{7}$$

$$v_s = (pL_a + R_a)i_{L2} + (pL_b + R_b)i_{L2} + D_2 V_o. \tag{8}$$

The definition of the circulating current [20] states that one can obtain the circulating current of the kth converter as the difference between the actual current and the assigned current reference as follows:

$$C_k \equiv i_{Lk} - \sigma_k I_L. \tag{9}$$

From the circulating current definition (9) and (7) and (8), the following circulating current model for converter 1 can be derived, i.e.,

$$C_1 \equiv (1 - 2\sigma_1)\frac{v_s}{p(L_a + L_b) + R_a + R_b} + \frac{V_o\left[D_2\sigma_1 - D_1(1 - \sigma_1)\right]}{p(L_a + L_b) + R_a + R_b}. \tag{10}$$

It follows from (10) that one can find that, when two paralleled converter system are operated at equal rating conditions, only the dc link voltage V_o contributes to the circulating currents. If the two paralleled converter systems are operated at different power rating conditions, both the ac grid voltage V_s and the dc link voltage V_o contribute to the circulating currents. In this case, the system stability problem may occur, and the stability is determined by the pole $p = -(R_a + R_b)/(L_a + L_b)$ of the circulating-current system. Therefore, when the ESR $(R_a + R_b)$ is decreased, the stability margin of the paralleled system is decreased. The lowest stability margin occurs when the ESR $(R_a + R_b)$ is equal to zero. Under this condition, the paralleled converter system easily descends into oscillation by external disturbances, which come from the ac grid voltage V_s and/or dc link voltage V_o. Fortunately, ESR always exists in the connective transmission line. Thus, the pole of the circulating-current system lies inside the left half s-plane and the stability of the paralleled system due to the circulating current is confirmed.

IV. Experimental Results

To verify the validity of the proposed method, a prototype of the paralleled system was constructed. The parallel system was tested under different power rating conditions as follows:

TABLE VI
PARAMETERS OF THE PARALLEL SYSTEM FOR EXPERIMENT

Parameters	Converter 1	Converter 2
Switching frequency	40kHz (0^0)	40kHz (180^0)
L_{xa}	0.8210mH	0.8865mH
L_{xb}	0.8278mH	0.7860mH
Capacitor	1.4140mF	1.4140mF
Load/DERs	100Ω/3A	
P_{o1}/P_{o2}	2 : 1	
Input voltage v_s	AC grid with 110 *Vrms*, 60 Hz fundamental Frequency, $THD_v \approx 5\%$	
Output voltage V_{dc}	300 V	

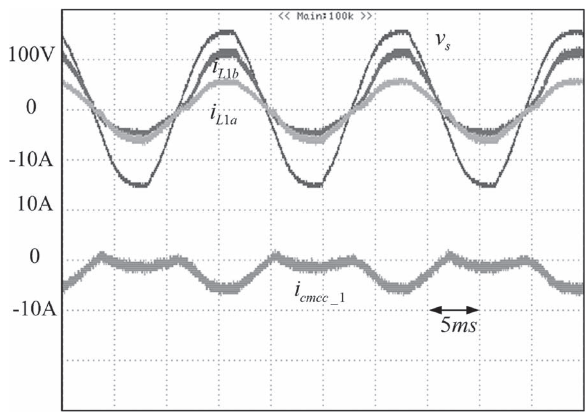

Fig. 13. Measured waveforms without circulating current control of the parallel system in different power rating conditions operated in rectifier mode. (Top: input voltage V_s, input line current i_{L1a} [gray], and i_{L1b} [black]. Bottom: common-mode circulating current $i_{\mathrm{cmcc\_1}}$).

(a) without circulating current control; (b) with switching constraint control in the parallel system; and (c) with proposed common-mode and differential-mode control schemes corresponding to the function block, as shown in Fig. 11. The implementation parameters for the parallel system are listed in Table VI.

Figs. 13 and 14 show the experimental results without circulating current control under different power rating conditions operated in rectifier mode. The measured waveforms of grid voltage V_s, line currents (i_{L1a}, i_{L1b}), and corresponding common-mode circulating current $i_{\mathrm{cmcc\_1}}$ of converter 1 are shown in Fig. 13. In addition, the measured waveform of grid voltage V_s, line currents (i_{L1a}, i_{L2a}) and corresponding differential-mode circulating current $i_{\mathrm{dmcc\_12}}$ are shown in Fig. 14. From Figs. 13 and 14 one can find that prominent common-mode and differential-mode circulating currents exist in the parallel system operated in rectifier mode.

Figs. 15 and 16 show the experimental results with the switching constraint method under different power rating conditions operated in rectifier mode. The measured waveforms of grid voltage V_s, line currents (i_{L1a}, i_{L1b}), and the corresponding common-mode circulating current $i_{\mathrm{cmcc\_1}}$ of converter 1 are shown in Fig. 15. In addition, the measured waveform of grid voltage V_s, line currents (i_{L1a}, i_{L2a}), and corresponding differential-mode circulating current $i_{\mathrm{dmcc\_12}}$ are shown in Fig. 16. From Figs. 15 and 16 one can find that, although the differential-mode circulating current is close to zero due to the switching constraint method, common-mode circulating currents still exist in the parallel system. This implies that

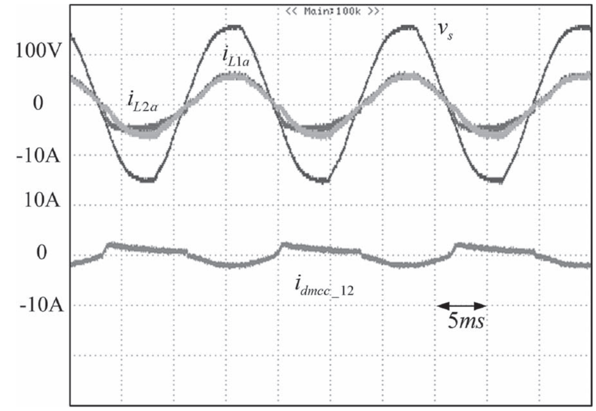

Fig. 14. Measured waveforms without circulating current control of the parallel system in different power rating conditions operated in rectifier mode. (Top: input voltage V_s, input line current i_{L1a} [gray], and i_{L2a} [black]. Bottom: differential-mode circulating current $i_{\mathrm{dmcc\_12}}$).

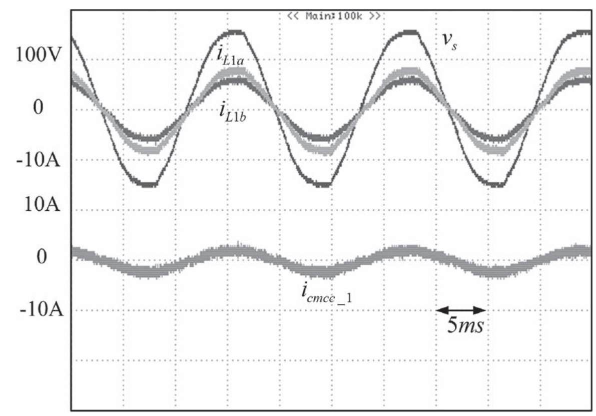

Fig. 15. Measured waveforms with switching constraint method of the parallel system in different power rating conditions operated in rectifier mode. (Top: input voltage V_s, input line current i_{L1a} [gray], and i_{L1b} [black]. Bottom: common-mode circulating current $i_{\mathrm{cmcc\_1}}$).

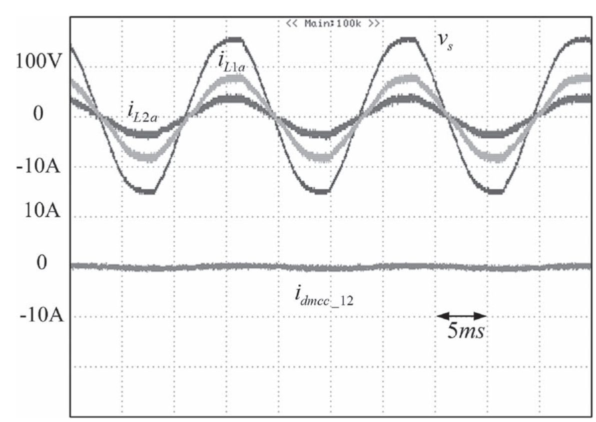

Fig. 16. Measured waveforms with switching constraint method of the parallel system in different power rating conditions operated in rectifier mode. (Top: input voltage V_s, input line current i_{L1a} [gray], and i_{L2a} [black]. Bottom: differential-mode circulating current $i_{\mathrm{dmcc\_12}}$).

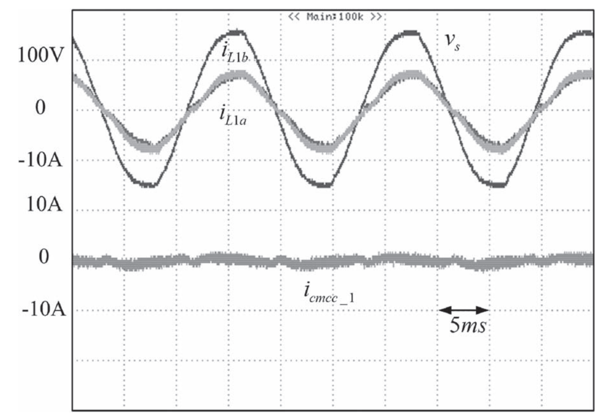

Fig. 17. Measured waveforms with proposed circulating current control scheme of the parallel system in different power rating conditions operated in rectifier mode. (Top: input voltage V_s, input line current i_{L1a} [gray], and i_{L1b} [black]. Bottom: common-mode circulating current $i_{\mathrm{cmcc\_1}}$).

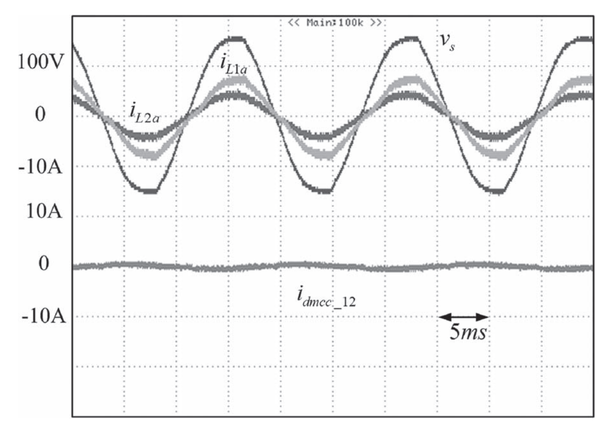

Fig. 18. Measured waveforms with proposed circulating current control scheme of the parallel system in different power rating conditions operated in rectifier mode. (Top: input voltage V_s, input line current i_{L1a} [gray], and i_{L2a} [black]. Bottom: differential-mode circulating current $i_{\mathrm{dmcc\_12}}$).

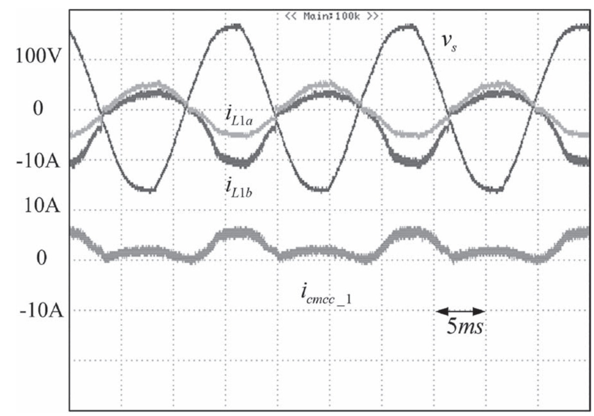

Fig. 19. Measured waveforms without circulating current control of the parallel system in different power rating conditions operated in inverter mode. (Top: input voltage V_s, input line current i_{L1a} [gray], and i_{L1b} [black]. Bottom: common-mode circulating current $i_{\mathrm{cmcc\_1}}$).

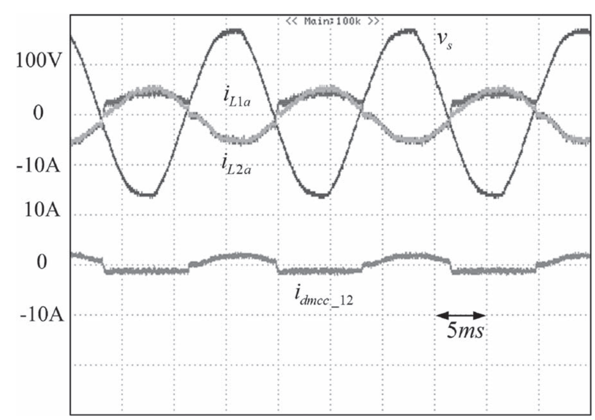

Fig. 20. Measured waveforms without circulating current control of the parallel system in different power rating conditions operated in inverter mode. (Top: input voltage V_s, input line current i_{L1a} [gray], and i_{L2a} [black]. Bottom: differential-mode circulating current $i_{\mathrm{dmcc\_12}}$).

the switching constraint method only has an effect on the differential-mode circulating currents and cannot control the common-mode circulating currents in the parallel system operated in rectifier mode.

Figs. 17 and 18 show the experimental results with the proposed common-mode and differential-mode control schemes under different power rating conditions operated in rectifier mode. The measured waveforms of grid voltage V_s, line currents (i_{L1a}, i_{L1b}), and corresponding common-mode circulating current $i_{\mathrm{cmcc\_1}}$ of converter 1 are shown in Fig. 17. In addition, the measured waveforms of grid voltage V_s, line currents (i_{L1a}, i_{L2a}), and corresponding differential-mode circulating current $i_{\mathrm{dmcc\_12}}$ are shown in Fig. 18. From Figs. 17 and 18 one can find that the common-mode and differential-mode circulating currents are close to zero. This implies that the proposed circulating current control method has an effect on the differential-mode circulating currents and also effects the common-mode circulating currents in the parallel system operated in rectifier mode.

A parallel system operated in the inverter mode is considered next. Figs. 19 and 20 show the experimental results without circulating current control under different power rating conditions operated in the inverter mode. The measured waveforms of grid voltage V_s, line currents (i_{L1a}, i_{L1b}), and the corresponding common-mode circulating current $i_{\mathrm{cmcc\_1}}$ of converter 1 are shown in Fig. 19. In addition, the measured waveform of grid voltage V_s, line currents (i_{L1a}, i_{L2a}), and the corresponding differential-mode circulating current $i_{\mathrm{dmcc\_12}}$ are shown in Fig. 20. From Figs. 19 and 20 one can find that prominent common-mode and differential-mode circulating currents exist in the parallel system operated in the inverter mode.

Figs. 21 and 22 show the experimental results with switching constraint method under different power rating conditions operated in the inverter mode. The measured waveforms of grid voltage V_s, line currents (i_{L1a}, i_{L1b}), and the corresponding common-mode circulating current $i_{\mathrm{cmcc\_1}}$ of converter 1 are shown in Fig. 21. In addition, the measured waveform of grid voltage V_s, line currents (i_{L1a}, i_{L2a}), and corresponding differential-mode circulating current $i_{\mathrm{dmcc\_12}}$ are shown in Fig. 22. From Figs. 21 and 22, one can find that, although the differential-mode circulating current is close to zero due to the switching constraint method, common-mode circulating currents still exist in the parallel system. This implies that the switching constraint method has an effect only on the

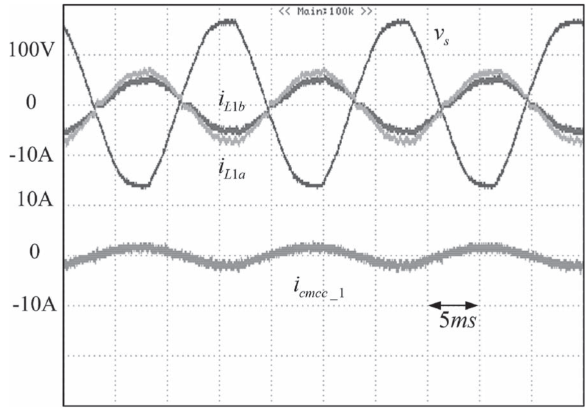

Fig. 21. Measured waveforms with switching constraint method of the parallel system in different power rating conditions operated in inverter mode. (Top: input voltage V_s, input line current i_{L1a} [gray], and i_{L1b} [black]. Bottom: common-mode circulating current $i_{\mathrm{cmcc\_1}}$).

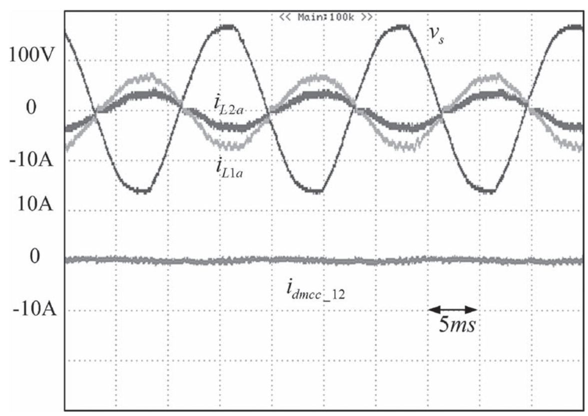

Fig. 22. Measured waveforms with switching constraint method of the parallel system in different power rating conditions operated in inverter mode. (Top: input voltage V_s, input line current i_{L1a} [gray], and i_{L2a} [black]. Bottom: differential-mode circulating current $i_{\mathrm{dmcc\_12}}$).

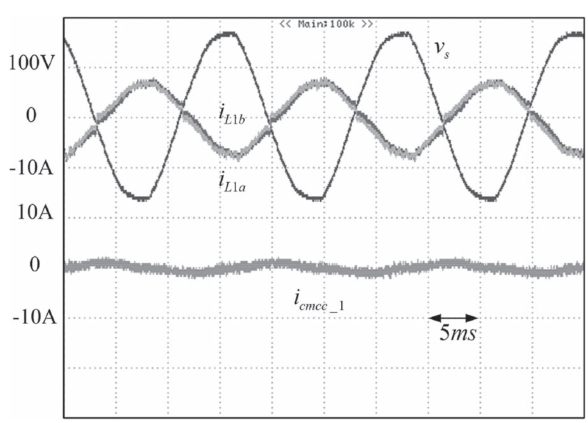

Fig. 23. Measured waveforms with proposed circulating current control scheme of the parallel system in different power rating conditions operated in inverter mode. (Top: input voltage V_s, input line current i_{L1a} [gray], and i_{L1b} [black]. Bottom: common-mode circulating current $i_{\mathrm{cmcc\_1}}$).

differential-mode circulating currents and cannot control the common-mode circulating currents in a parallel system operated in the inverter mode.

Figs. 23 and 24 show the experimental results with proposed common-mode and differential-mode control schemes under different power rating conditions operated in the inverter mode. The measured waveforms of grid voltage V_s, line currents (i_{L1a}, i_{L1b}), and the corresponding common-mode circulating current $i_{\mathrm{cmcc\_1}}$ of converter 1 are shown in Fig. 23. In addition, the measured waveforms of grid voltage V_s, line currents (i_{L1a}, i_{L2a}), and the corresponding differential-mode circulating current $i_{\mathrm{dmcc\_12}}$ are shown in Fig. 24. From Figs. 23 and 24, one can find that both the common-mode and differential-mode circulating currents are close to zero. This implies that the proposed circulating current control method has an effect on the differential-mode circulating currents and effects the common-mode circulating currents in a parallel system operated in the inverter mode.

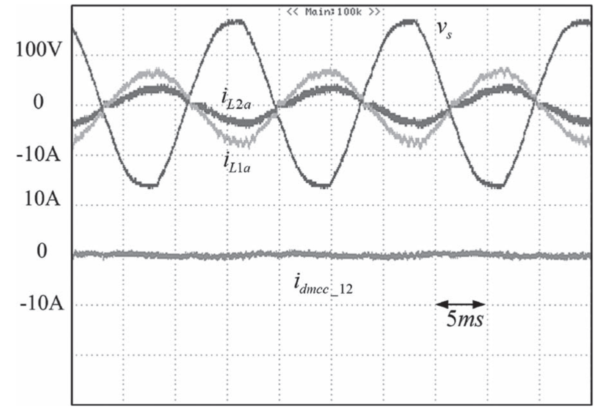

Fig. 24. Measured waveforms with proposed circulating current control scheme of the parallel system in different power rating conditions operated in inverter mode. (Top: input voltage V_s, input line current i_{L1a} [gray], and i_{L2a} [black]. Bottom: differential-mode circulating current $i_{\mathrm{dmcc\_12}}$).

V. CONCLUSION

This paper has proposed definitions for CMCC and DMCC. Then, CMCC and DMCC compensators in a centralized control scheme were also proposed to reduce the common-mode and differential-mode circulating currents in a paralleled system. In addition, a prototype system was constructed and experimental results were given to verify the validity of the proposed control scheme. From the experimental results, the proposed control scheme can indeed reduce the circulating currents under different power rating conditions in a parallel system. The shape of the input line currents of the paralleled system was controlled in sinusoidal waveform and in phase with the input voltage.

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