77–110 GHz 65-nm CMOS Power Amplifier Design

Kun-Long Wu, Kuan-Ting Lai, Robert Hu, Christina F. Jou, Dow-Chih Niu, and Yu-Shao Shiao

***Abstract*—This paper details the development of our millimeter-wave wideband power amplifier design. By treating the power combiner as an impedance transformer which allows different loading impedance to be taken into account, a compact wideband power-combining network can be constructed. With small transmission-line attenuation being sustained and maximum output power easily extracted from the transistors over the 77–110 GHz frequency range, a power amplifier can then be designed using 65-nm CMOS process to cover the whole *W*-band. In the on-wafer measurement, the gain is around 18 dB, the output reflection coefficients is below −10 dB, and the output-referred 1 dB compression point can reach 12 dBm at 1.2 V bias condition; when the bias is increased to 2.5 V, a 18 dBm output power is recorded. To our knowledge, this is the first CMOS power amplifier that covers the whole *W*-band.**

***Index Terms*—CMOS, impedance transformation, millimeter-wave, power amplifier, power combining, wideband.**

I. Introduction

In THE DESIGN of silicon power amplifiers, several techniques have been employed to increase the output power level such as current combining where the Wilkinson power combiner is probably the most well-known [1]–[6], voltage combining [7]–[13], or the phase-array spatial combining [14]–[16]. With very low-loss antennae, which need to be fabricated separately from the amplifier circuit, the radiation efficiency and aggregate power level of the phase-array power amplifier system can be impressive. Since the current or voltage combining approach can be developed independently and then integrated with the phase-array technique on the system level, we would like to explore in this paper the possibility of designing an optimized millimeter-wave wideband PA circuit using either current- or voltage-combining for maximum output power delivery over the intended bandwidth, which is 77–110 GHz in this case.

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As with $Z_{\rm L}$ the loading impedance and n the total number of amplification branches, the equivalent loading impedance for each branch will be $n \cdot Z_{\rm L}$ in the current-combining case and $Z_{\rm L}/n$ in voltage-combining. Therefore, it is the impedance-dividing property in voltage combining that allows large current, and thus power, extraction from individual transistor. This preferred large current swing is more obvious in the submicron era, where low breakdown voltage tends to limit the available output power of each transistor. However, the complexity of circuit layout and the parasitics of the transformer itself will make the voltage-combining technique to be narrow-band. By contrast, the simplicity in current-combining layout renders the design of millimeter-wave wideband PA a less daunting task as long as the $n \cdot Z_{\rm L}$ constraint can be properly handled. In this paper, by treating the combining circuit as impedance transformer, it is found that, under parallel-RC loading condition, a very compact and low-loss current combiner can be constructed over wide bandwidth. At the combiner's output, a broadband network will provide this specific RC value from the nominal 50 Ω loading impedance; while at its input, another matching circuit can maximize the power extraction from the transistor. Theoretical analysis and simulation regarding this capacitive-loading power combiner and the matching circuits are carried out first; power combiners for other loading conditions, such as parallel-RL, series-RC, and series-RL, will also be compared and discussed. A 77–110 GHz 65-nm, CMOS power amplifier is then designed using this combining technique and measured on-wafer. Though the delivered output power is still lower than those of narrow-band amplifiers, this 77–110 GHz PA demonstrates the potential of silicon circuits in millimeter-wave wideband applications.

II. Analysis of Capacitive Power-Combining Circuit

Fig. 1(a) shows the schematic of an ideal n-way power combining circuit where the output loading is a $R_{\rm L}C_{\rm L}$ parallel circuit. With identical (common-mode) input signals, an equivalent single-branch configuration can be constructed, as illustrated in Fig. 1(b). By assuming the line impedance to be $Z_{\rm T}$ and its electrical length $\theta_{\rm T}$, the corresponding input impedance $Z_{\rm in}$ can be derived as

$$Z_{\rm in} = Z_{\rm T}\frac{nZ_{\rm L} + jZ_{\rm T}\tan\theta_{\rm T}}{Z_{\rm T} + jnZ_{\rm L}\tan\theta_{\rm T}}, \tag{1}$$

with

$$Z_{\rm L} = \left(\frac{1}{R_{\rm L}} + j\omega C_{\rm L}\right)^{-1}. \tag{2}$$

If we treat the power combining circuit as a multi-input single-output impedance transformer that allows the loading

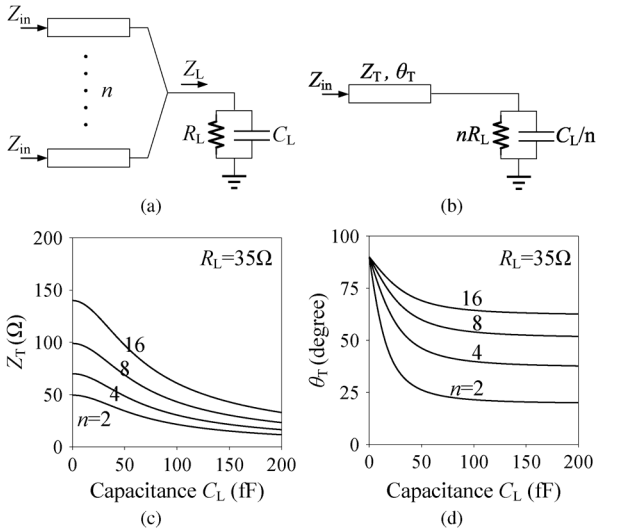

Fig. 1. Capacitive power-combining circuit. (a) In the n-way power-combining circuit, the loading impedance $Z_{\rm L}$ is made of $R_{\rm L}$ in parallel with $C_{\rm L}$. (b) Equivalent single-branch circuit where $Z_{\rm T}$ is the characteristic impedance of the transmission line and $\theta_{\rm T}$ is this line's electrical length. (c) Optimized $Z_{\rm T}$ for the 2-, 4-, 8-, and 16-way power combining circuits where the loading resistance $R_{\rm L}$ is fixed at 35 Ω and $C_{\rm L}$ varies from 0 to 200 fF; the frequency of interest is 94 GHz. (d) The corresponding $\theta_{\rm T}$.

impedance to be replicated at the input ports, i.e., $Z_{\rm in} = Z_{\rm L}$, we then have

$$Z_{\rm T} = R_{\rm L}\sqrt{\frac{n}{1+\omega^2 R_{\rm L}^2 C_{\rm L}^2}} \tag{3}$$

$$\theta_{\rm T} = \tan^{-1}\left(\frac{n-1}{2}\cdot\frac{1}{\omega C_{\rm L} Z_{\rm T}}\right). \tag{4}$$

Fig. 1(c) and (d) displays the calculated $Z_{\rm T}$ and $\theta_{\rm T}$ versus different loading capacitance for 2-, 4-, 8-, and 16-way power combining circuits where the loading resistance $R_{\rm L}$ is fixed at 35 Ω and the frequency of interest is 94 GHz. Here we choose 35 Ω rather then 50 Ω is because the output resistance of the 40×1.8 μm 65-nm CMOS transistor used in our PA design is close to 35 Ω; therefore, it will be more convenient using 35 Ω from the beginning of the analysis. In the zero-$C_{\rm L}$ case, the resulting $Z_{\rm T}$ for $n = 2$ is the well-known $\sqrt{2}R_{\rm L}$ and $\theta_{\rm T}$ is 90°. However, if $C_{\rm L}$ is increased to 80 fF, then $Z_{\rm T}$ and $\theta_{\rm T}$ become 26 Ω and 22°, i.e., capacitive output loading allows wider and shorter transmission lines to be used for power-combining purpose. It is also interesting to observe that the $\theta_{\rm T}$ will remain constant for larger value of $C_{\rm L}$.

When compared with the conventional quarter-wavelength resistive power-combining circuit, the shorter and wider transmission lines used in the capacitive power combiner means the related power loss can be reduced. Such benefit, however, will be compromised if discernible bandwidth degradation is observed. To evaluate the resemblance of $Z_{\rm in}$ to $Z_{\rm L}$, the deviation parameter $\Delta_{\rm T}$ in decibels can be defined as

$$\Delta_{\rm T} = 20\log\left|\frac{Z_{\rm L}-Z_{\rm in}}{Z_{\rm L}+Z_{\rm in}}\right|. \tag{5}$$

The smaller the $\Delta_{\rm T}$, the better the impedance transformation. As shown in Fig. 2(a), the solid curves on the Smith chart are the 77–110 GHz capacitive output loading impedance where $R_{\rm L}$ is 35 Ω and $C_{\rm L}$ is 0, 25, 50, and 100 fF, respectively; the dashed curves are the corresponding input impedance of the two-way power combining circuit with $Z_{\rm T}$ and $\theta_{\rm T}$ optimized at 94 GHz. Fig. 2(b) shows the $\Delta_{\rm T}$ where the perfect impedance transformation at 94 GHz makes $\Delta_{\rm T} = 0$, i.e., $-\infty$dB, at that specific frequency point and less than -20 dB elsewhere. Since the capacitive power combining technique is more than capable of covering the whole *W*-band from the $\Delta_{\rm T}$ perspective, $Z_{\rm T}$ other than the ideal value can be used to accommodate some layout constraints, as demonstrated in Fig. 2(c). Here the solid curve is the output loading of 35 Ω ($= R_{\rm L}$) in parallel with 80 fF ($= C_{\rm L}$); the dashed curve 1 is the $Z_{\rm in}$ where the line impedance used in the power combiner is the optimized 26 Ω and electrical length 22°. Since 26 Ω line (of 13 μm line width) is a little too wide to implement in the silicon circuit, we instead choose $Z_{\rm T} = 41$ Ω (of 5 μm line width) while keep $\theta_{\rm T}$ the same 22°, and the resulting $Z_{\rm in}$ is the dashed curve 2. Surely there is no reason that the $\theta_{\rm T}$ cannot be finessed too, and so curve 3 is for $Z_{\rm T} = 41$ Ω and $\theta_{\rm T} = 18°$. Fig. 2(d) shows the corresponding $\Delta_{\rm T}$, and we can see that the adoption of 41 Ω transmission line is just fine.

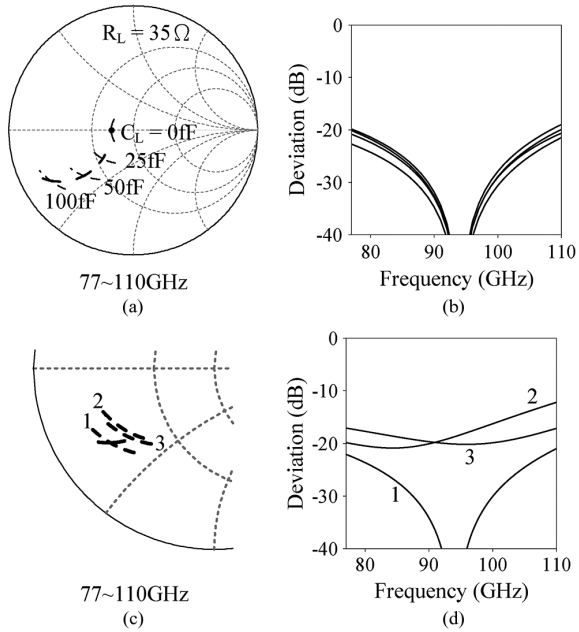

Fig. 2. Frequency response of the two-way capacitive power combining circuit in 77–110 GHz. (a) Impedance displayed on the Smith chart where the solid curves have their $R_{\rm L}$ fixed at 35 Ω and $C_{\rm L} = 0, 25, 50$, and 100 fF, respectively; the dashed curves are the input impedance $Z_{\rm in}$ of the power combiner which is optimized at 94 GHz. (b) Deviation of $Z_{\rm in}$ from $Z_{\rm L}$. (c) Solid curve is for $R_{\rm L} = 35$ Ω and $C_{\rm L} = 80$ fF; the dashed curve 1 is for $Z_{\rm in}$ of the power combiner with optimized $Z_{\rm T} = 26$ Ω and $\theta_{\rm T} = 22°$; the dashed curve 2 is with $Z_{\rm T}$ changed to 41 Ω and $\theta_{\rm T}$ is still the same 22°; the dashed curve 3 is with $Z_{\rm T} = 41$ Ω and $\theta_{\rm T}$ changed to 18°. (d) Corresponding deviation $\Delta_{\rm T}$ in decibels.

Theoretically, the bandwidth constraint of the capacitive power combiner can also be determined by the Bode–Fano criteria, which states

$$\int_0^\infty \ln\frac{1}{|\Gamma(\omega)|}d\omega \le \frac{\pi}{R_{\rm L}C_{\rm L}}. \tag{6}$$

If we assume the in-band reflection is -20 dB, i.e., $|\Gamma| = 0.1$, and total reflection for out-of-band, then we have

$$2\pi\Delta f \cdot \ln\frac{1}{0.1} \le \frac{\pi}{35\cdot 80\cdot 10^{-15}}. \tag{7}$$

The allowed impedance transformation bandwidth will be 77.5 GHz, which is much larger than $110 - 77 = 33$ GHz.

From the DC perspective, since the output power-combining circuit is often used for drain-bias purpose too in most power amplifier design, short and low-impedance microstrip lines means the DC voltage drop can be reduced and thus more efficient operation of the amplifier is expected. In terms of RF, the millimeter-wave power loss is surely proportional to the line's physical length while its dependence on linewidth is less critical. For a transmission line of physical length l $(= \lambda\cdot\theta_{\rm T}/2\pi)$, both its characteristic impedance $Z_{\rm T}$ $(= 1/Y_{\rm T})$ and propagation constant γ can be derived from the $ABCD$ matrix as [17]

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh\gamma l & Z_{\rm T}\sinh\gamma l \\ Y_{\rm T}\sinh\gamma l & \cosh\gamma l \end{bmatrix} \tag{8}$$

therefore,

$$Z_{\rm T} = \sqrt{\frac{B}{C}} \tag{9}$$

$$\gamma = \alpha + j\beta = \frac{1}{l}\sinh^{-1}\sqrt{BC}. \tag{10}$$

Fig. 3(a) illustrates the profile of the 65-nm CMOS transmission line where the top metal is made of thick copper while the bottom metal is a thin aluminum sheet. Fig. 3(b) is the characteristic impedance calculated at 77, 94, and 110 GHz, respectively, and they all render the same result. Fig. 3(c) is the simulated attenuation constant and here we have taken into account the metal, dielectric, and radiation losses. Among the three loss factors, the metal loss dominates while the radiation loss is very small and can be neglected. If we further split the metal loss into the top-metal loss and the bottom-metal loss, then it is found that the top-metal loss decreases with wider linewidth while, due to more concentrated current density along the bottom metal, the bottom-metal loss increases with wider linewidth. As a result, the attenuation constant reveals a very weak dependence on linewidth in this frequency range. Fig. 3(d) shows the effective relative dielectric constant $\epsilon_{\rm eff}$ which is defined as

$$\epsilon_{\rm eff} = \left(\frac{\beta\lambda_0}{2\pi}\right)^2 \tag{11}$$

where λ_0 is the free-space wavelength.

Fig. 4(a) is the schematic of the cascaded two-way power combining circuit. The total power loss (in dB) along the $2\theta_{\rm T}$ transmission-lines can be calculated as

$$\text{Power Loss} = 20\log(\mathrm{e}^{\alpha\cdot\lambda\cdot 2\theta_{\rm T}/2\pi}). \tag{12}$$

Fig. 4(b) shows the simulated results where the solid curve corresponds to $Z_{\rm T} = 41\ \Omega$ and $\theta_{\rm T} = 22°$, which is used for loading impedance $Z_{\rm L}$ equal to 35 Ω in parallel with 80 fF; the dashed curve is with $Z_{\rm T} = \sqrt{2}\cdot 35 \simeq 50\ \Omega$ and $\theta_{\rm T} = 90°$, and is used for $Z_{\rm L} = 35\ \Omega$. Apparently, power loss of the capacitive power-combining circuit is about 1 dB less than that of the conventional quarter-wave power-combining circuit. Fig. 4(c) and (d) shows the schematic and the simulated results of the direct four-way power-combining circuit and, again, the capacitive combining approach presents a smaller power loss. Though there is a strong incentive in the resistive power-combining case to use direct four-way than cascaded two-way, as the former requires a 90° electrical length while the latter demands $2\cdot 90° = 180°$, there is no such preference in the capacitive power-combining situation.

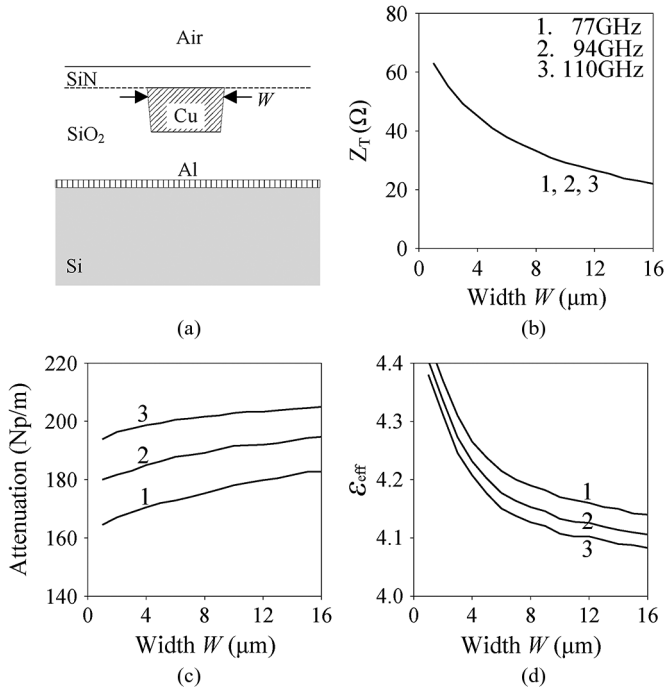

Fig. 3. Property of the transmission line used in the power combining circuit. (a) Profile of the 65-nm CMOS transmission line where the top metal is made of copper with conductivity $\sigma = 5.8\times 10^7$ S/m, while the bottom metal sheet is aluminum with $\sigma = 3.8\times 10^7$ S/m. Loss tangent $\delta_{\rm D}$ for silicon nitride and silicon oxide used in the simulation are 0.008; the conductivity of silicon substrate is $\sigma = 10$ S/m. (b) Simulated characteristic impedance of the transmission line which is independent of frequency. (c) 77, 94, and 110 GHz attenuation constant versus linewidth W. (d) Effective relative dielectric constant.

Finally, we would like to inquire whether other loading arrangements, such as series $R_{\rm L}C_{\rm L}$, parallel $R_{\rm L}L_{\rm L}$, or series $R_{\rm L}L_{\rm L}$, can render similar results. For series $R_{\rm L}C_{\rm L}$ loading with $Z_{\rm L} = 1/j\omega C_{\rm L} + R_{\rm L}$, the characteristic impedance and electrical length of the transmission line are

$$Z_{\rm T} = R_{\rm L}\sqrt{n\left(1+\frac{1}{\omega^2 R_{\rm L}^2 C_{\rm L}^2}\right)}$$

$$\theta_{\rm T} = \tan^{-1}\left(\frac{n-1}{2n}\cdot\omega C_{\rm L} Z_{\rm T}\right). \tag{13}$$

For parallel $R_{\rm L}L_{\rm L}$ loading with $Z_{\rm L} = (1/j\omega L_{\rm L} + 1/R_{\rm L})^{-1}$, we have

$$Z_{\rm T} = R_{\rm L}\sqrt{n\left(1+\frac{R_{\rm L}^2}{\omega^2 L_{\rm L}^2}\right)^{-1}}$$

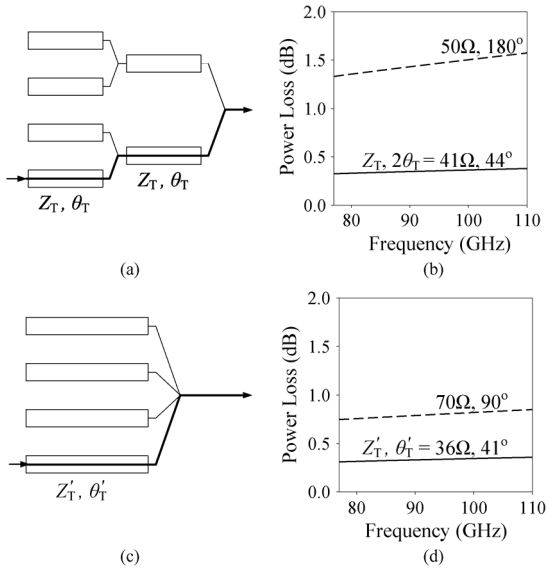

Fig. 4. Cascaded two-way and direct four-way power combining circuits. (a) Schematic of the cascaded two-way power combiner. (b) Total power loss of the cascaded two-way's. The solid curve corresponds to transmission line with $Z_{\rm T} = 41\ \Omega$ and $\theta_{\rm T} = 22°$, which is used for output loading of $R_{\rm L} = 35\ \Omega$ and $C_{\rm L} = 80$ fF. The dashed curve is with $Z_{\rm T} = 50\ \Omega$ and $\theta_{\rm T} = 90°$, and is used for $R_{\rm L} = 35\ \Omega$ and $C_{\rm L} = 0$. (c) Schematic of the direct four-way combiner. (d) The corresponding power loss where the solid curve is for $R_{\rm L} = 35\ \Omega$ and $C_{\rm L} = 80$ fF, while the dashed curve is for $R_{\rm L} = 35\ \Omega$ and $C_{\rm L} = 0$.

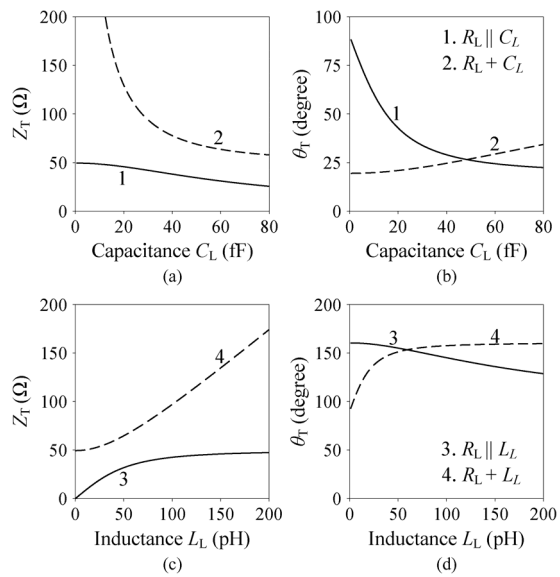

Fig. 5. Characteristic impedance and electrical length of the transmission line used in power combining circuit with different loading conditions. (a) Theoretical $Z_{\rm T}$ where the solid curve is for parallel $R_{\rm L}C_{\rm L}$ loading while the dashed curve is for series $R_{\rm L}C_{\rm L}$ loading. Here $R_{\rm L}$ is fixed at 35 Ω and the frequency is 94 GHz. (b) $\theta_{\rm T}$ for parallel and series $R_{\rm L}C_{\rm L}$ loadings. (c) Theoretical $Z_{\rm T}$ where the solid curve is for parallel $R_{\rm L}L_{\rm L}$ loading while the dashed curve is for series $R_{\rm L}L_{\rm L}$ loading. (d) Corresponding $\theta_{\rm T}$.

and

$$\theta_{\rm T} = \tan^{-1}\left(\frac{n-1}{-2}\cdot\frac{\omega L_{\rm L}}{Z_{\rm T}}\right). \tag{14}$$

While for series $R_{\rm L}L_{\rm L}$ loading with $Z_{\rm L} = j\omega L_{\rm L} + R_{\rm L}$, there is

$$Z_{\rm T} = R_{\rm L}\sqrt{n\left(1+\frac{\omega^2 L_{\rm L}^2}{R_{\rm L}^2}\right)}$$
$$\theta_{\rm T} = \tan^{-1}\left(\frac{n-1}{-2n}\cdot\frac{Z_{\rm T}}{\omega L_{\rm L}}\right). \tag{15}$$

Fig. 5(a) and (b) shows the $Z_{\rm T}$ and $\theta_{\rm T}$ used in the two-way power combining circuit with parallel and series $R_{\rm L}C_{\rm L}$ loadings. For small capacitor, say, $C_{\rm L}$ smaller than 40 fF, the transmission-line impedance used for series $R_{\rm L}C_{\rm L}$ loading is just too large; as $C_{\rm L}$ increases, the corresponding electrical length $\theta_{\rm T}$ will increase and soon surpass that used in the parallel $R_{\rm L}C_{\rm L}$ case. Fig. 5(c) and (d) shows the parallel and series $R_{\rm L}L_{\rm L}$ loadings: the larger-than-quarter-wavelength transmission line deems both unrealistic. It then becomes clear that the parallel $R_{\rm L}C_{\rm L}$ is the preferred loading of choice for power-combining circuit design.

III. 77–110 GHz Power Amplifier Design

This power amplifier is designated to operate in the linear, i.e., class-A, region, with three amplification stages, where each stage is made of two common-source transistors so that flat gain response can be obtained in 77–110 GHz. In the simulation, wideband input matching is made possible by fine-tuning the input transistors' loading impedance. Four common-source transistors are arranged, using the aforementioned combining technique, to deliver the power simultaneously. To ensure sufficient power gain at 110 GHz, each transistor is made of two paralleled $20 \times 1.8\ \mu$m ones, i.e., $2 \cdot 20 \cdot 1.8 = 72\ \mu$m, with the corresponding $f_{\rm max}$ reaching 200 GHz [18]; at 1.2 V drain bias voltage, the transistor's current density is 34 mA/72 μm and its output resistance $R_{\rm ds}$ $(= 1/{\rm Re}[Y_{\rm ds}])$ will be close to 35 Ω in 77–110 GHz. Since it is the current swing rather than voltage swing that tends to constrain the circuit's performance in this low impedance situation, the maximum output power can be determined through conjugate impedance matching. Fig. 6 is the schematic of the 77–110 GHz power amplifier where the output impedance $Z_{\rm ds}$ of the final-stage transistors in this frequency range can be modelled as a paralleled $R_{\rm ds}C_{\rm ds}$ circuit with $R_{\rm ds} = 35\ \Omega$ and $C_{\rm ds} = 80$ fF. For efficient power delivery over such wide bandwidth, the capacitive power-combining technique and two additional tuning circuits are employed here. The output-load tuning circuit converts the nominal 50Ω system impedance into a shunt $R_{\rm L}C_{\rm L}$, with $R_{\rm L} = 35\ \Omega$ and $C_{\rm L} = 80$ fF, to be used as the power combiner's loading impedance $Z_{\rm L}$. The two-stage capacitive power-combining circuit, with $Z_{\rm T} = 41\ \Omega$ and $\theta_{\rm T} = 22°$, then makes its $Z_{\rm in}$ to be close to $Z_{\rm L}$, which happens to be $Z_{\rm ds}$. The power-match tuning circuit transforms $Z_{\rm in}$ to its complex-conjugate counterpart $Z_{\rm in}^*$ $(= Z_{\rm ds}^*)$, thus facilitates maximum power extraction from the transistors.

Fig. 7(a) and (b) shows the schematic and simulated results of the output-load tuning circuit. Due to the existence of the pad capacitor $C_{\rm pad}$, the output impedance presented to this amplifier is not a pure 50 Ω but rather resembles that of point $Z_{\rm A}$ on the Smith chart. At 94 GHz, the series inductor $L_{\rm series}$ or a short transmission line will transform $Z_{\rm A}$ to $Z_{\rm B}$. The parasitic shunt capacitance of the DC-blocking capacitor, $C_{\rm shunt}$, then

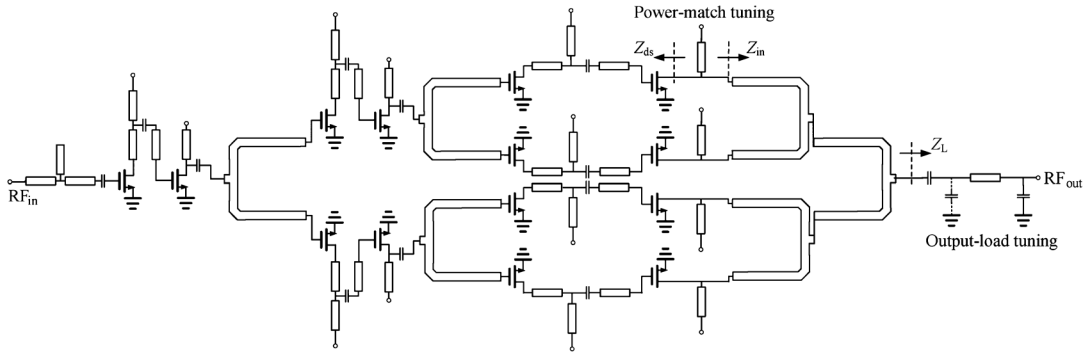

Fig. 6. Schematic of the 77–110 GHz power amplifier. The output-load tuning circuit will transform the 50 Ω system impedance to paralleled RC loading, thus facilitates the use of capacitive power-combining network. The power-match tuning circuit allows efficient wideband power extraction from the output transistors.

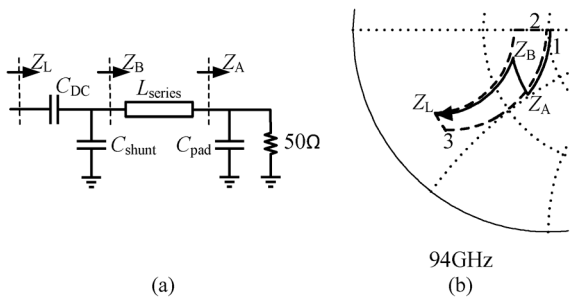

Fig. 7. Output-load tuning circuit. (a) Schematic where $C_{\rm shunt}$ is the parasitic capacitance of the large DC-blocking capacitor.(b) The solid curve 1 is the intended tracking contour that moves from the origin of the Smith chart to point $Z_{\rm A}$ and then $Z_{\rm B}$, and finally to $Z_{\rm L}$, with $C_{\rm pad} = 25$ fF, $L_{\rm series} = 20$ pH, and $C_{\rm shunt} = 55$ fF. Dashed curve 2 is with zero-$C_{\rm pad}$, $L_{\rm series}$ being a quarter-wave transmission line, and a large $C_{\rm shunt}$. Dashed curve 3 has large $C_{\rm pad}$, short transmission line, and zero-$C_{\rm shunt}$.

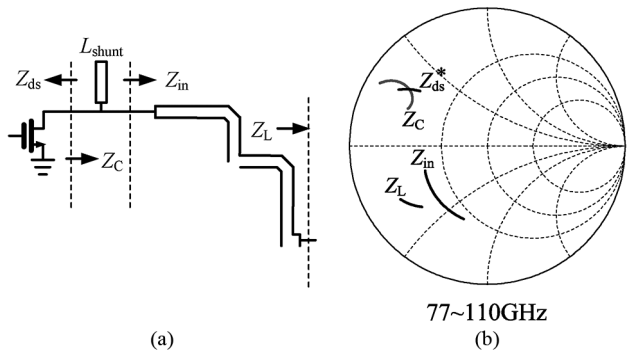

Fig. 8. Power-match tuning circuit. (a) Schematic. (b) The 77–110 GHz $Z_{\rm L}$ will be transformed by the two-stage power-combining network into $Z_{\rm in}$ where the total electrical length equal to $22^\circ + 18^\circ$. The shunt inductor $L_{\rm shunt}$ (= 18 pH) then converts $Z_{\rm in}$ to $Z_{\rm C}$, which is close to the complex conjugate of the transistor's output impedance, i.e. $Z_{\rm ds}^*$.

moves $Z_{\rm B}$ to the intended $Z_{\rm L}$, which has the impedance of 35Ω in parallel with 80 fF. The solid curve 1 corresponds this tuning process. If zero-$C_{\rm pad}$ is allowed, an assumption that holds true only theoretically in the CMOS but is feasible in GaAs or InP processes, then a quarter-wave transmission line can be employed to transform the 50 Ω to the intended 35 Ω; a $C_{\rm shunt}$ of 80 fF can then be added to reach $Z_{\rm L}$, as indicated by the dashed curve 2. On the other hand, if the DC-blocking capacitor can be completely removed, then a slightly larger $C_{\rm pad}$ followed by a short $L_{\rm series}$ could also convert the nominal 50 Ω loading to $Z_{\rm L}$, as illustrated by the dashed curve 3. Of the three approaches, the $L_{\rm series}$ used in curve 3 has the smallest value and therefore is the most preferred one from the power conservation perspective; however, the omission of on-chip DC-blocking capacitor may cause problems or other inconveniences. The zero-$C_{\rm pad}$ approach of curve 2, though simple in analysis, is lossy since it requires a quarter-wave transmission line. By contrast, our tuning method of curve 1 is the most feasible one, as both DC-blocking capacitance and RF pad capacitance have been taken into account. Fig. 8(a) and (b) is the schematic and simulated results of the power-match tuning circuit, which is located between the output transistors and the power combiner. The cascaded two-way power combiner will convert $Z_{\rm L}$ to $Z_{\rm in}$. The shunt inductor $L_{\rm shunt}$ then moves $Z_{\rm in}$ to $Z_{\rm C}$, which is close to $Z_{\rm ds}^*$, thus allows efficient power extraction. For better illustration, the $Z_{\rm L}$, $Z_{\rm in}$, $Z_{\rm C}$ and $Z_{\rm ds}^*$ contours at 77–110 GHz are all displayed on the Smith chart and it is clear that this tuning circuit is up to the task. As for the loss of the output network, it can be obtained through EM simulation. At 94 GHz, the shunt stub accounts for 0.6 dB power loss, the cascaded 2-way power combiner has $0.3 + 0.3 = 0.6$ dB loss, the DC-blocking contributes 0.3 dB loss and the final tuning line takes away another 0.3 dB; therefore, the total output-network loss is 1.8 dB.

Surely we would like to ask whether there is a more direct way for complex-conjugate power match, or is it possible to have $\mathrm{Im}[Y_{\rm in}]$ of the power combiner to be the negative value of $\mathrm{Im}[Y_L]$ so that the additional shunt stub can be omitted, and the answer is yes. In the case of $Y_{\rm L} = j\omega C_{\rm L} + 1/R_L$ and $Y_{\rm in} = -j\omega C_{\rm L} + 1/R_{\rm in}$, then the impedance and electrical length of the transmission line in the n-way power combiner can be determined as

$$Z_{\rm T} = R_{\rm L}\sqrt{n\left(k + \frac{n-k}{nk-1}\omega^2 {R_{\rm L}}^2 {C_{\rm L}}^2\right)^{-1}}$$
$$\theta_{\rm T} = \tan^{-1}\left(\frac{nk-1}{k-1}\cdot\frac{1}{\omega C_{\rm L} Z_{\rm T}}\right) \tag{16}$$

and $k = R_{\rm L}/R_{\rm in}$. Now if we have $R_{\rm L} = 50$ Ω and $R_{\rm in} = 35$ Ω, these calculated results are displayed in Fig. 9. For a 4-way direct-power-match combiner, as shown in Fig. 10, the transmission line impedance and electrical length are 47 Ω and

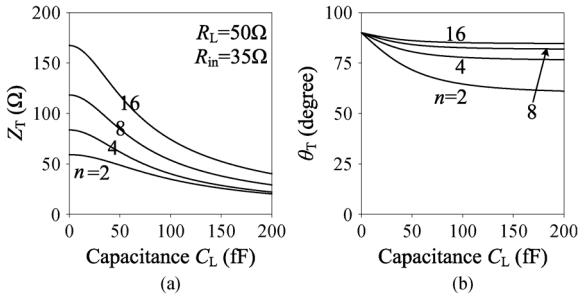

Fig. 9. Impedance and electrical length of the power combiner which transforms the negative value of $\mathrm{Im}[Y_L]$ to $\mathrm{Im}[Y_{in}]$, thus allows direct power match with the transistor's output.

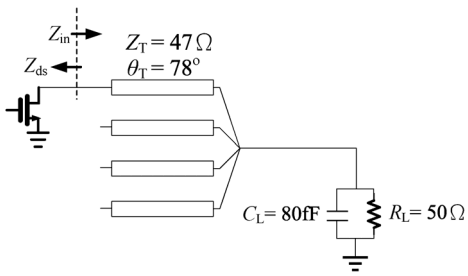

Fig. 10. Schematic of the 4-way direct-power-match power combiner. Here $Z_{in} = Z_{ds}^*$, and Z_L is paralleled RC circuit.

78°, respectively, and that causes $Z_{in} = Z_{ds}^*$ at 94 GHz and therefore the shunt stub can be omitted completely. Though capable of direct power match, this combining technique tends to be narrowband or medium-bandwidth at most, as demonstrated in Fig. 11(a). Here Z_C is from our proposed capacitive power combining method while Z_{in} is using the direct-power-match combiner; apparently, the Z_C contour is closely following Z_{ds}^* over the 77–110 GHz frequency range. Even worst for the direct-power-match method is that, for frequency below 75 GHz, its transformed input impedance will be on the lower half of the Smith chart, i.e., capacitive now. A measure of the bandwidth for complex-conjugate power match can also be through the deviation parameter, which is defined as

$$\Delta_M = 20 \log \left| \frac{Z_{in} - Z_{ds}^*}{Z_{in} + Z_{ds}^*} \right| \tag{17}$$

and Z_{in} needs to be changed to Z_C for capacitive power combiner. Fig. 11(b) shows the simulated results and it is clear that our proposed capacitive power combiner, as solid curve, allows effective power extraction from the transistor in 77–110 GHz. On the other way, in terms of loss, the direct-power-match combiner has 1.8 dB loss at 94 GHz. If we further include the additional 0.2 dB loss from the quarter-wavelength shunt stub used for drain bias, the total loss will approach 2 dB at 94 GHz, which is slightly larger than the 1.8 dB obtained from our proposed method.

Fig. 12 is the photograph of the 77–110 GHz power amplifier using 65-nm CMOS process where the chip size is 950 × 600 μm^2. Since metal–insulator–metal (MIM) capacitors are not available from the foundry during the time of designing this circuit, we instead use custom-made multilayer interdigital metal–oxide–metal (MOM) capacitor, which has its res-

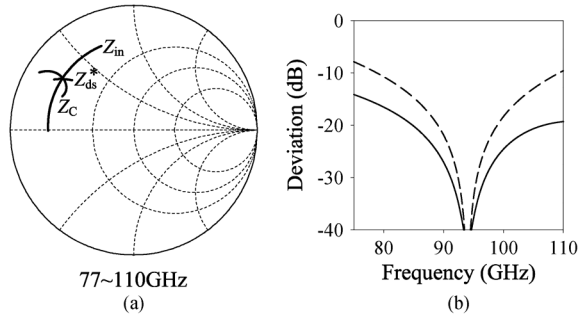

Fig. 11. Comparison of capacitive power combiner with direct-power-match power combiner. (a) Z_C is the input impedance of the capacitive power combiner while Z_{in} comes from the direct-power match combiner. Z_{ds}^* is the complex conjugate of the transistor's output impedance. (b) the solid curve is the deviation of Z_C from Z_{ds}^*, while the dashed curve is the deviation of Z_{in} from Z_{ds}^*.

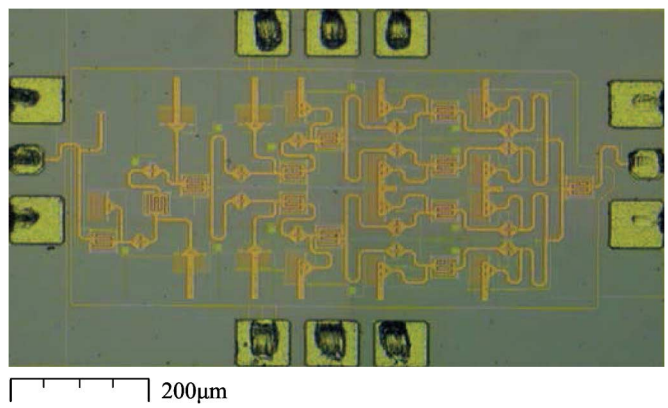

Fig. 12. Photograph of the 77–110 GHz power amplifier with 65-nm CMOS process. The chip size is 950 × 600 μm^2. With 1.2 V and 480 mA drain bias, the total power consumption is 576 mW. The capacitors are all custom-made multi-layer MOM capacitors. The two V_d pads, and V_g pads too, on both sides of the chip are internally connected.

onance frequency well above 120 GHz and thus is valid for use at *W*-band. With DC bias of 1.2 V and 480 mA, the total power consumption is 576 mW. The *W*-band *S*-parameters, as measured on-wafer, are displayed in Fig. 13(a) where the solid curves correspond to 1.2 V bias while the dashed curves are with 2.6 V bias; apparently, this amplifier can effectively cover 70–110 GHz from the small-signal perspective and is unconditionally stable, as is judged by the stability factor. The DC-140 GHz *S*-parameters with 1.2 V bias are shown in Fig. 13(b). Due to the limits of the instrument, the measured results are only to 110 GHz while the simulation can be up to 140 GHz. If we decrease the transistor's gate resistance by 5 Ω, then the S_{21} peaking toward 110 GHz will be observed in the simulation; this reduction of gate resistance in the modelling can also explain why the measured noise figure is 2 dB lower than its simulated counterpart. As for the large-signal measurement, Fig. 14(a) shows both the measured and simulated output power versus input power at 77 GHz and 110 GHz, which can then be used to derive their respective output-referred 1 dB compression point, or OP1 dB. Fig. 14(b) displays the OP1 dB of 77–110 GHz; due to the constraint imposed by the waveguide port of the power meter, the amplifier's power performance below 77 GHz has not been measured. In the simulation, the peak of OP1 dB oc-

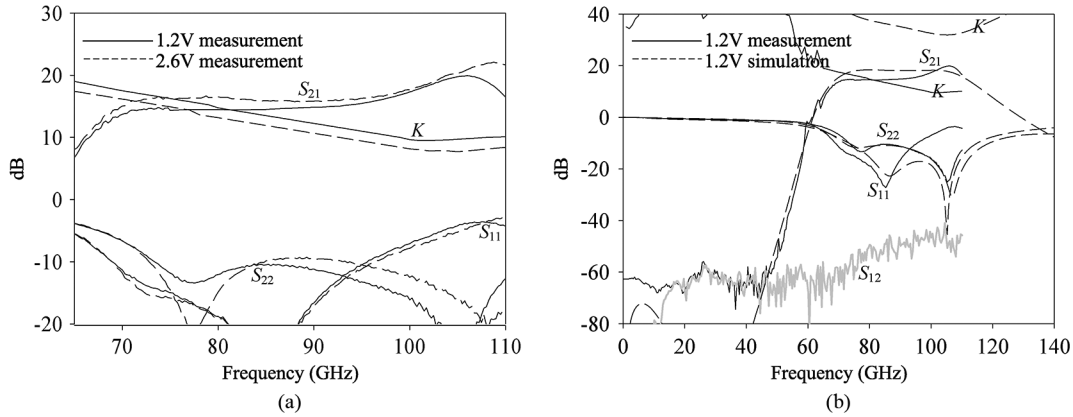

Fig. 13. S-parameters of the power amplifier. (a) The solid curves are measurement with $V_{\rm d} = 1.2$ V and $I_{\rm d} = 480$ mA while the dashed curves are measurement with $V_{\rm d} = 2.6$ V and $I_{\rm d} = 620$ mA. The stability factors are displayed in $10\log_{10} K$. (b) DC-140 GHz S-parameters and K factor in the 1.2 V case where the solid curves are measured results while the dashed curves are their simulated counterparts. The simulated S_{12} is far below −80 dB and not displayed here. The 3 dB bandwidth for S_{21} in the simulation covers 70–110 GHz.

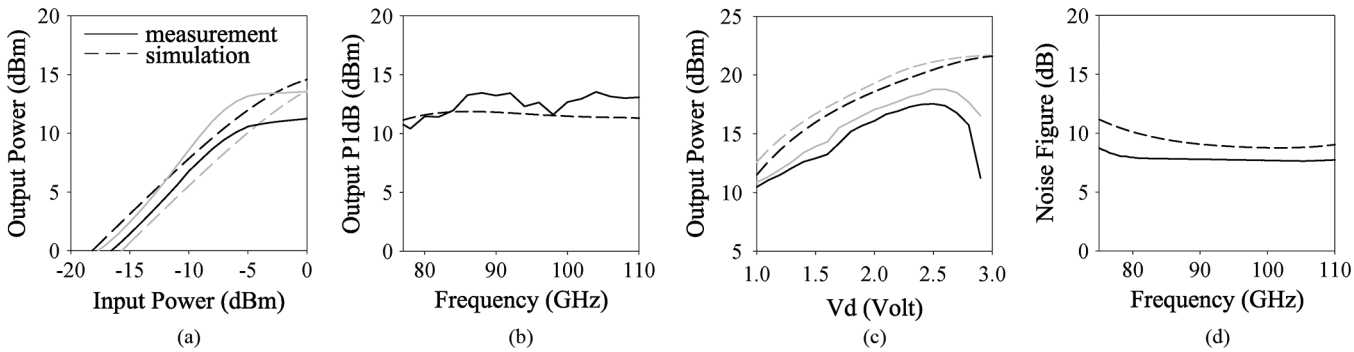

Fig. 14. Measured and simulated performance of the power amplifier. (a) Output power versus input power at 77 GHz (black curves) and 110 GHz (gray curves) with bias of $V_{\rm d} = 1.2$ V and $I_{\rm d} = 480$ mA. (b) The output-referred 1 dB compression point from 77 to 110 GHz, as measured with 2 GHz frequency step. The 1 dB bandwidth for OP1 dB is 76–114 GHz in the simulation. (c) 77 GHz (black curves) and 110 GHz (gray curves) output power at different drain bias voltages where the input power is fixed at 0 dBm. (d) Noise figure. In all the plots, the solid curves are the measured results while the dashed curves are their simulated counterparts.

TABLE I
W-BAND SILICON-BASED POWER AMPLIFIER COMPARISON

References	[12]	[19]	[20]	[21]	[22]	[1]	[5]	[23]	[24]	This work
Freq. (GHz)	71-81	80–90	80–100	85–100	101–117	70–85	77–86	79–88	73-97	77-110
BW (GHz)	10	10	20	15	16	15	9	9	24	33
Supply (V)	1	2	1.2	1.2	1.2	1.8	4	2.5	2.5	1.2
Gain (dB)	24.2	11	13	10	14	17	25	27	8	18
OP1dB (dBm)	16.4	12	6	7	11.6	14.5	12.5	16	na	12
Psat (dBm)	19.3	12	10	13	14.8	17.5	14.7	18	21	14
PAE (%)	19.2	14.2	7.3	4	9.4	12.8	8.1	9	3.6	4.5
Combining	8-way	1-way	1-way	4-way	4-way	2-way	2-way	4-way	4-way	4-way
Gain Topology	4-stage CS	2-stage Cascode	4-stage CS	3-stage Cascode	2 Cascode plus 1 CS	4-stage CE	2-stage Cascode	1 Cascode plus 2 CB	8-stage Cascode	6-stage CS
Process Technology	65nm CMOS	45nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	0.12μm SiGe	0.18μm SiGe	0.13μm SiGe	0.13μm SiGe	65nm CMOS

curs at 87 GHz and it is 11.8 dBm, and the frequency points for OP1 dB of $11.8 - 1 = 10.8$ dBm are 76 and 114 GHz; given that the 3 dB bandwidth of S_{21} is 70–110 GHz, it becomes appropriate characterizing this PA as 77–110 GHz. Surely, by increasing the drain bias voltage $V_{\rm d}$, the available output power of this PA can be steadily boosted, as is demonstrated in Fig. 14(c); with 0 dBm input power at 110 GHz, the corresponding output will increase from 13 to 18 dBm when the bias is changed from 1.2 to 2.5 V. Fig. 14(d) is the noise figure of this amplifier where the measurement is 2 dB lower than the simulation, and this may be coming from the overestimation of the gate resistance in transistor modeling.

A comparison with other CMOS or SiGe power amplifiers covering similar frequency range is tabulated in Table I. It is true that a transformer is capable of pulling more current from the transistors; however, the resulting millimeter-wave PA tends to be of moderate bandwidth, as symmetric circuit layout is difficult to maintain now [12], [21]–[23]. On the other hand, it has

been proposed using a tapered transmission-line in the power combining circuit to obtain wider bandwidth, and the resulting power amplifier can effectively cover 73–97 GHz [24]; however, by using capacitive power combining method, we have demonstrated that an even wider-band PA can be constructed without line tapering. As for the PAE, our 4.5% may not be impressive. This is because, in order to sustain large enough gain across such wide bandwidth, a total of ten transistors has been used for gain amplification while only four are for output power delivery. If lower gain or narrower bandwidth can be accepted or more advanced process such as SiGe is adopted, then the PAE can be increased accordingly.

IV. Conclusion

The capacitive power-combining theory has been proposed and analyzed in this paper, which allows a low-loss power-combining network to be constructed over broad bandwidth. A 77–110 GHz power amplifier using 65-nm CMOS process is designed using this technique and then measured on-wafer. It shows an OP1 dB of 12 dBm under 1.2 V bias condiction, and the output power can reach 18 dBm at 2.5 V bias.

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