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Performance comparison of titanium-oxide resistive switching memories using GeO_x and AlO_x capping layers for flexible application

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To meet the requirements of flexible memory applications, we have compared two capping layers of GeO_x and AlO_x on a TiO_y resistive random access memory (RRAM) at room temperature. A Ni/GeO_x/TiO_y/TaN RRAM shows a large resistance window of $>10^2$, 85 °C retention, a high-resistance-state (HRS) activation energy (E_a) of 0.52 eV, and a good DC cycling of 10^3 cycles, which are significantly better than those of a Ni/AlO_x/TiO_y/TaN RRAM, which has a high-defect-density dielectric of AlO_x. © 2014 The Japan Society of Applied Physics

1. Introduction

Flexible electronics are attractive for next-generation display technology. One challenge in the fabrication of flexible electronics is the lack of a nonvolatile memory (NVM) for system-on-chip (SoC) function. The conventional floating-gate or charge-trapping flash memory[1,2] is difficult to integrate into flexible substrates owing to the severely degraded gate oxide quality at low temperatures.[3,4] Therefore, several NVM types such as ferroelectric random-access memories (FeRAMs),[4] magnetic random-access memories (MRAMs), and resistive random-access memories (RRAMs)[5–17] are being investigated. RRAMs have attracted much attention for next-generation NVM applications owing to their simple structure, small cell size, and high speed. On the other hand, RRAMs have inherent merits of a lower-temperature process and a simpler structure for flexible electronics applications.[18–24] However, they require costly noble metal electrodes and poor resistance distribution. Such a poor distribution prevents further memory array realization, in sharp contrast to the existing sub-tera-bit flash memory. To address these issues, we previously developed ultralow-power RRAMs[6–8] to lessen the dielectric stress. The Ni/GeO_x/high-κ/TaN RRAMs show a negative temperature coefficient (TC), opposite to other conductive-filament-type RRAMs owing to ion migration.

In this paper, we present a room-temperature Ni/GeO_x/TiO_y/TaN RRAM device with 0.28 μW set power, low 25 μW reset power, fast switching (10 μs) and a stable endurance in the 1000 cycling test. For comparison, we also investigate a room-temperature Ni/AlO_x/TiO_y/TaN RRAM device, which has a similar switching power but markedly poor endurance and poor switching uniformity owing to the defect-rich AlO_x dielectric processed at room temperature. The present results demonstrate that the room-temperature Ni/GeO_x/TiO_y/TaN RRAM has high potential for future flexible memory applications.

2. Experimental procedure

The RRAM devices were fabricated on standard Si wafers. For VLSI backend integration, the process was started by depositing a 200-nm-thick SiO_2 layer on the Si substrates. Then, 100 nm TaN was prepared by physical vapor deposition (PVD). After patterning the bottom TaN electrode, a 15-nm-thick TiO_y film and a 6-nm-thick GeO_x layer were deposited at room temperature to form the stacked structure of GeO_x/TiO_y. Lastly, a 50-nm-thick Ni layer was deposited and patterned to form the top electrode with an area of 11300 μm^2 in the RRAM device. For comparison, the Ni/AlO_x/TiO_y/TaN RRAM device was also fabricated with a 6-nm-thick AlO_x capping layer on TiO_y. Here, Ni provides a low-cost solution for a high-work-function (5.1 eV) electrode, which has been implemented in high-κ DRAM capacitors.[25]

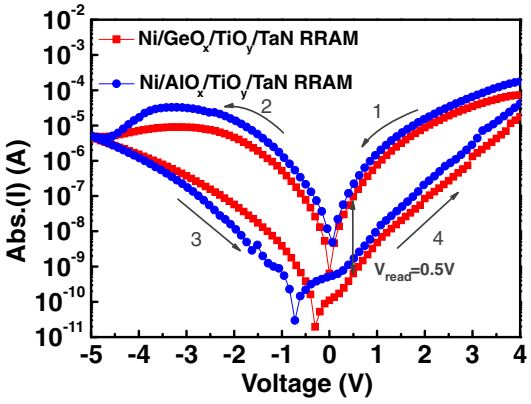

Fig. 1. (Color online) Swept I–V curves of Ni/GeO_x/TiO_y/TaN and Ni/AlO_x/TiO_y/TaN RRAM devices.

3. Results and discussion

Figure 1 shows the current–voltage (I–V) switching characteristics of Ni/GeO_x/TiO_y/TaN and Ni/AlO_x/TiO_y/TaN RRAM devices on the SiO_2 isolation layer. The forming-free and self-compliance current switching characteristics are measured, which are vital for simplifying the circuit design without the need for a high-current forming process and extra current compliance. The low self-compliance set currents of 78 and 73 μA at 4 V and low reset currents of 2.3 and 5 μA at −5 V are measured in AlO_x/TiO_y and GeO_x/TiO_y RRAM devices, respectively. The switching windows at a reading voltage of 0.5 V for AlO_x/TiO_y and GeO_x/TiO_y RRAM devices are 130× and 152×, respectively. From resistive I–V curves, these two RRAM devices show close switching high/low-resistance-state (HRS/LRS) currents and resistance windows. Although the AlO_x/TiO_y RRAM and GeO_x/TiO_y RRAM devices have similar switching characteristics, the AlO_x/TiO_y RRAM device shows poor endurance character-

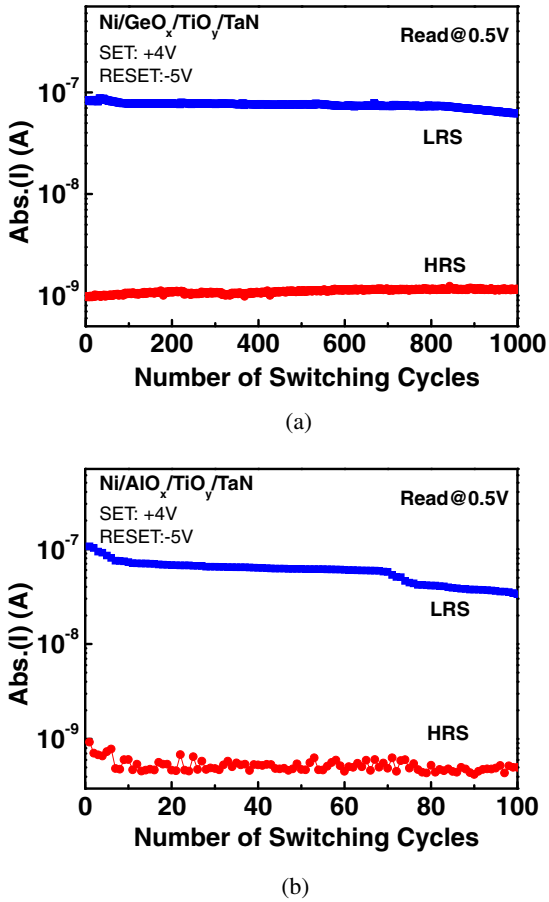

Fig. 2. (Color online) Endurance cycling of (a) Ni/GeO$_x$/TiO$_y$/TaN and (b) Ni/AlO$_x$/TiO$_y$/TaN RRAM devices.

istics [Fig. 2(b)] in the 100 cycling test under set/reset conditions of 4 V/−5 V. The degraded resistance windows after cycling 100 times are about 42% in the AlO$_x$/TiO$_y$ RRAM device. The step like deteriorations at LRS may be caused by electron trapping near the Ni/AlO$_x$ interface, which results in unstable switching behavior and window shrinking during continued cycling. Unlike the degraded memory window of the AlO$_x$/TiO$_y$ RRAM device, the GeO$_x$/TiO$_y$ RRAM exhibits stable *I*–*V* switching at both HRS and LRS currents and large HRS/LRS ratio. In contrast to GeO$_x$/TiO$_y$, an unstable HRS current and a gradually reduced LRS current are obtained in AlO$_x$/TiO$_y$ RRAMs, which indicates that the presence of defect centers in the AlO$_x$/TiO$_y$ stack or near the electrode interface affects resistive switching characteristics. From the endurance results, it is demonstrated that the poor HRS/LRS switching behaviors during cycling are dominated by trap-controlled Frenkel–Poole (FP) conduction through trapping and detrapping effects.

To understand the low switching power, we have analyzed the current conduction mechanism, as shown in Fig. 3. We apply a negative voltage to the top Ni electrode for electron injection for us to measure and fit *I*–*V* characteristics under HRS conditions. The good agreement between the measured and fitting HRS currents suggests that the currents are conducted via the FP emission mechanism:

$$J \propto E \exp\left(\frac{\sqrt{q^3 E/\pi\varepsilon}}{k_B T}\right). \quad (1)$$

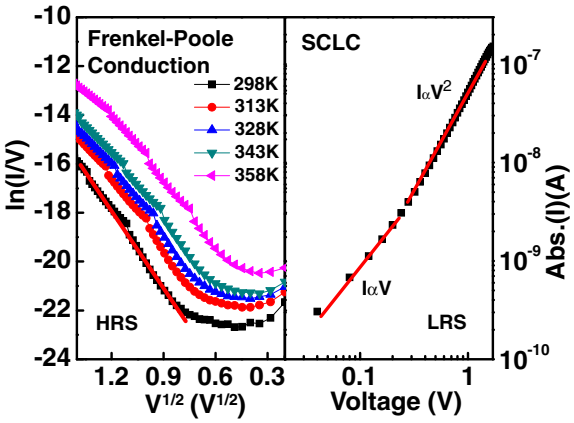

Fig. 3. (Color online) *I*–*V* curves of the HRS and LRS of Ni/GeO$_x$/TiO$_y$/TaN RRAM obtained by fitting with FP and space-charge-limited current mechanisms.

Here, J is the current density; E, the applied electric field; q, the elementary charge; ε, the dynamic permittivity; k_B, Boltzmann's constant; and T, the temperature. The increasing HRS current with increasing temperature is due to the high hopping emission rate, which increases FP conduction.[26] In order to reach LRS, a positive voltage is applied to the top Ni electrode, where electrons were injected from the bottom TaN electrode. At a low electric field, LRS exhibits space-charge-limited current (SCLC) with trap control, since the slopes are proportional to V.

We have further conducted X-ray photoelectron spectroscopy (XPS) to study the current conduction mechanism. To precisely analyze material bonding, the film samples of TiO$_x$, AlO$_x$, and GeO$_x$ are pretreated by in situ Ar bombardment for 10 s under 6 to 8 × 10^{-8} Torr to remove the native oxide on the sample surface. Figures 4(a) and 4(b) show the Ti 2p, and O 1s, and Ge 2p$_{3/2}$ and Al 2p XPS spectra, respectively. The nonstoichiometric TiO dielectric has different titanium energy peaks such as Ti 2p$_{3/2}$ (Ti^{4+}) and Ti 2p$_{3/2}$ (Ti^{3+}), as shown in Fig. 4(a). The different Ti ion chemical states were measured in the TiO dielectric, indicating the formation of charged oxygen vacancies, which is favorable for resistance switching in RRAM devices under appropriate biasing conditions. In Fig. 4(b), the Ge 2p$_{3/2}$ XPS spectrum reveals that the composition of the room-temperature-processed GeO dielectric is close to stoichiometric. However, the Al 2p XPS spectrum shows three different binding energies corresponding to different valence bonds, namely, Al$_2$O$_3$ (Al^{3+} = 74.5 eV),[27] Al–Al bonds (Al^{2+} = 71.8 eV), and AlO$_x$ (72.5 eV) of the AlO dielectric. The different Al ion chemical states indicate the formation of charged oxygen vacancies and an oxygen-deficient dielectric layer, which may lead to temperature-dependence leakage current even with a large bandgap.

Good uniformity is the fundamental challenge in the fabrication of RRAM devices for NVM array applications. Only few RRAM papers showed the cycle-to-cycle (C2C) distribution in the same device, rather than the NVM-array-required device-to-device (D2D) distribution among different devices.[5–21] Figures 5(a) and 5(b) show the C2C and D2D current distributions of the GeO$_x$/TiO$_y$ and AlO$_x$/TiO$_y$ RRAM devices, respectively. Because of the different mean

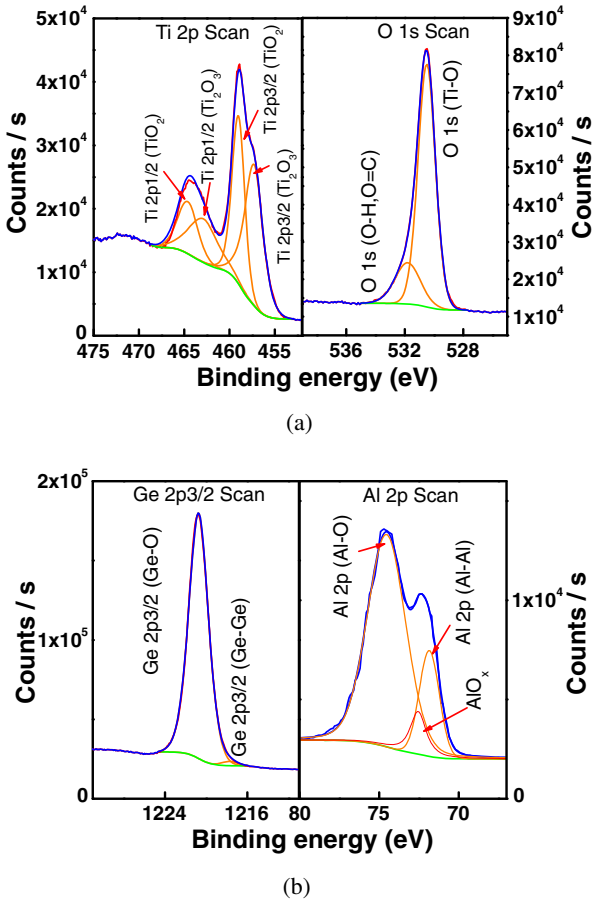

Fig. 4. (Color online) XPS spectra of (a) Ti 2p and O 1s, and (b) Ge 2p3 and Al 2p of Ni/GeO_x/TiO_y/TaN and Ni/AlO_x/TiO_y/TaN RRAM devices.

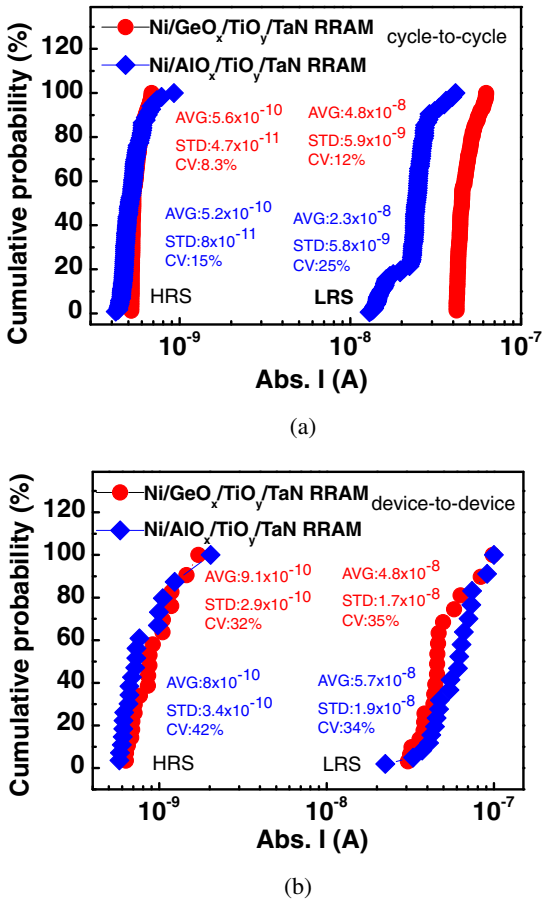

Fig. 5. (Color online) (a) C2C and (b) D2D current distributions of Ni/GeO_x/TiO_y/TaN and Ni/AlO_x/TiO_y/TaN RRAM devices.

values, the coefficient of variation (CV) was used to evaluate the distribution. The CV is a normalized measure of dispersion of a probability distribution, defined as the ratio of standard deviation (σ) to mean value (μ). The C2C current CVs of LRS for AlO_x/TiO_y and GeO_x/TiO_y RRAMs are 25 and 12%, whereas the C2C current CVs of HRS for AlO_x/TiO_y and GeO_x/TiO_y RRAMs are 15 and 8.3%, respectively. In Fig. 5(a), the AlO_x/TiO_y RRAM shows poor current distribution in bulk-limited self-compliance LRS. The unstable resistance switching can be attributed to the defect-rich AlO_x capping layer that affects bulk vacancy control in LRS. Figure 5(b) shows the D2D current distributions of the GeO_x/TiO_y and AlO_x/TiO_y RRAMs. In HRS, the AlO_x/TiO_y RRAM shows the worse D2D distribution, resulting from the poor surface coverage uniformity of the defect-rich AlO_x layer. The only way to improve the poor HRS/LRS distributions in AlO_x/TiO_y RRAM is oxygen annealing to remove defects, but high-temperature annealing is not allowed for flexible electronics.

To study the conduction mechanism, we have measured the temperature-dependent current at LRS and HRS. The LRS activation energy (E_a) of 0.43 eV for GeO_x/TiO_y RRAM is close to that of negative TC in highly defective Si governed by hopping conduction,[28] which suggests LRS mechanism are related by hopping via defects in GeO_x/TiO_y RRAMs, as shown in Fig. 6(a). Such hopping conduction and negative TC were observed previously in GeO.[29] Oxygen vacancies can be formed at a very low temperature, which degrade GeO_2/Ge MOSFETs,[30] but they are very useful for RRAMs. However, a much lower LRS activation energy (0.27 eV) is obtained for the AlO_x/TiO_y RRAM, where the HRS/LRS resistance change may be dominated by electron tunneling via shallow traps in the thin defect-rich AlO_x tunneling barrier.

Good retention and endurance are the essential characteristics for NVM. Figure 6(b) shows the retention of GeO_x/TiO_y and AlO_x/TiO_y RRAM devices. From the results, the AlO_x/TiO_y RRAM shows a very poor data retention characteristic such that the memory window is closed after 10^4 s at low 60 °C retention, compared wuth the GeO_x/TiO_y RRAM. Besides, the degraded HRS current at 60 °C retention can be attributed to the E_a in HRS (0.4 eV) being lower than 0.52 eV of the GeO_x/TiO_y RRAM device. This is because a high-temperature annealing for defect removal in the AlO_x dielectric is necessary. The electrons pile up near the Ni/AlO_x interface from the defect-rich AlO_x layer, leading to window shrinking in LRS. In HRS, the defect-related current leakage from the defect-rich AlO_x layer leads to window shrinking during the high-temperature retention test. Although the Al_2O_3 dielectric has a large bandgap of 8.8 eV, the defect-rich AlO_x layer processed at room temperature still cannot be prevented from having a degraded HRS current owing to thermally assisted tunneling via a lowered Ni/AlO_x barrier under the high-temperature retention test.

4. Conclusions

The Ni/GeO_x/TiO_y/TaN RRAM provides good switching

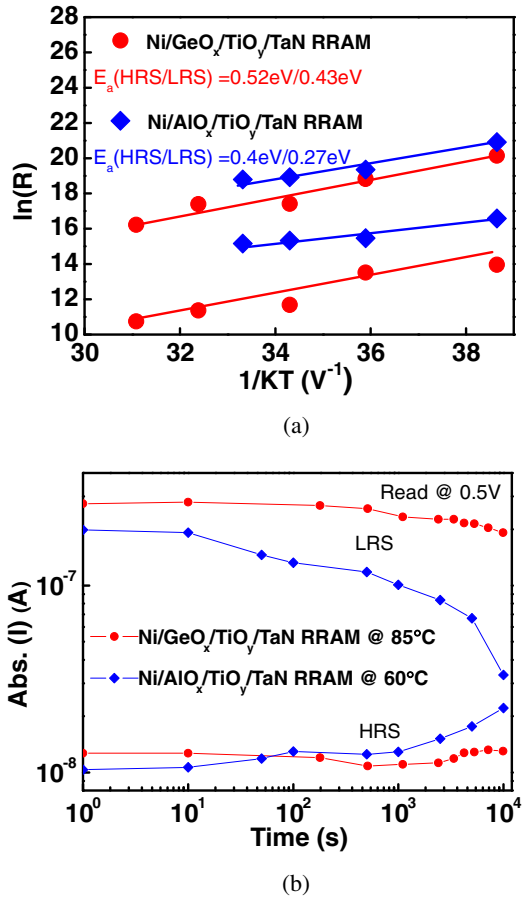

Fig. 6. (Color online) (a) Activation energy and (b) retention of Ni/GeO$_x$/TiO$_y$/TaN and Ni/AlO$_x$/TiO$_y$/TaN RRAM devices.

characteristics with a low self-compliance set current of 73 μA at 4 V and a low reset current of 5 μA at −5 V, a good switching window of 152×, and stable data retention at 85 °C for 10^4 s. Such good RRAM performance characteristics compared with Ni/AlO$_x$/TiO$_y$/TaN are related to the well-bonded GeO$_x$ dielectric deposited by room-temperature fabrication using a very suitable room-temperature flexible RRAM process. The room-temperature Ni/GeO$_x$/TiO$_y$/TaN RRAM with such good characteristics shows great promise in future flexible memory applications.

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