Current-Mode Synthetic Control Technique for High-Efficiency DC–DC Boost Converters Over a Wide Load Range

Yi-Ping Su, Yean-Kuo Luo, Yi-Chun Chen, and Ke-Horng Chen, *Senior Member, IEEE*

***Abstract*— This paper proposes a current-mode synthetic control (CSC) technique for the design of boost converters to overcome the difficulty in designing a current-ripple hysteresis boost converter and to maintain high conversion efficiency over a wide load range. The CSC technique has a high accuracy because of the additional voltage path through the error amplifier. A smooth load transient response is maintained when the operation transits from continuous conduction mode with a nearly constant switching frequency to discontinuous conduction mode with a load-dependent switching frequency. Generally, ripple performance, light-load efficiency, and switching frequency are traded off in the design of hysteresis control regulator. In this paper, a balance among the load-dependent switching frequencies at light loads results in high power conversion efficiency compared with conventional pulsewidth modulation converter and attains compact ripple performance. The experimental results show that the output voltage ripple can be kept <50 mV over a wide load current range from 10 to 400 mA, where as power conversion efficiency is maintained at 78% at a load current of 10 mA when the switching frequency is decreased from 5 to 2 MHz.**

***Index Terms*— Boost converter, current-mode synthetic control (CSC), hysteresis control regulator.**

I. Introduction

PORTABLE electronics products, such as cellular phones, laptops, and diverse multimedia equipment, use battery as the main power source. To extend the battery life, portable devices stay in sleep mode with a very low static current but require a fast wakeup response to reach the normal mode, which consumes much higher operating current. Therefore, suitable converters used in portable devices require fast transient response from the standby to normal mode [1]–[5]. Furthermore, high efficiency must be guaranteed over a wide load range [6]. Basically, hysteresis control, either in current- or voltage-ripple control mode, can address fast transient requirement [7]–[9]. In addition, hysteresis control is self-stabilized if the equivalent series resistance (ESR) of the output capacitor is large enough.

Basically, the voltage-ripple hysteresis mode modulator must regulate the output voltage within the voltage hysteresis window [9]–[11]. Its transient response is fast due to the fast operation of the comparator, but it is difficult to interleave (multiphase) due to complexity in derivation of the clock signal [11]–[16]. Another disadvantage is that the output ripple must be large enough to increase noise margin [8], [9], [11]; hence, a larger ESR value is necessary. In other words, interference immunity must be enhanced by a large ESR, but it suffers from large transient voltage variation. Selection of the output capacitor is limited with large ESR.

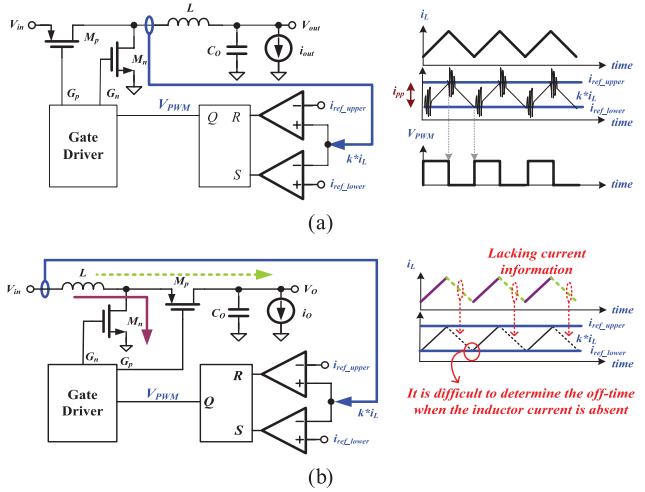

Fig. 1. Examples of current-ripple hysteresis control in (a) buck and (b) boost converter.

On the other hand, the current-ripple hysteresis mode modulator requires a current sensing circuit to obtain current information [17]–[20]. Fig. 1(a) shows an example of a current-ripple hysteresis buck converter. Inductor current, i_L, is regulated within the hysteresis window. Large ESR value is not necessary. It is, however, hard to determine the switching clock because of ground bounce and switching noise at the intersection region. In other words, the low noise immunity seriously affects the regulation performance. In addition, the advantage of current-ripple hysteresis control is not suitable for a boost converter because it is difficult to determine the off- and on-time even if the switching noise is ignored [17]–[19]. The reason is that a conventional current sensor, which uses a scaled sensing MOSFET, senses inductor current only when the low-side power switch turns on. Thus, it cannot provide a full-range sensing mechanism, as shown in Fig. 1(b). Even if the current sensing can be obtained by a sensing resistor in series with the inductor, conversion efficiency will be greatly deteriorated because of large conduction loss.

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The authors are with the Institute of Electrical Control Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan (e-mail: susu.supy@gmail.com; q1892111@nckualumni.org.tw; m432567.ece97g@nctu.edu.tw; khchen@cn.nctu.edu.tw).

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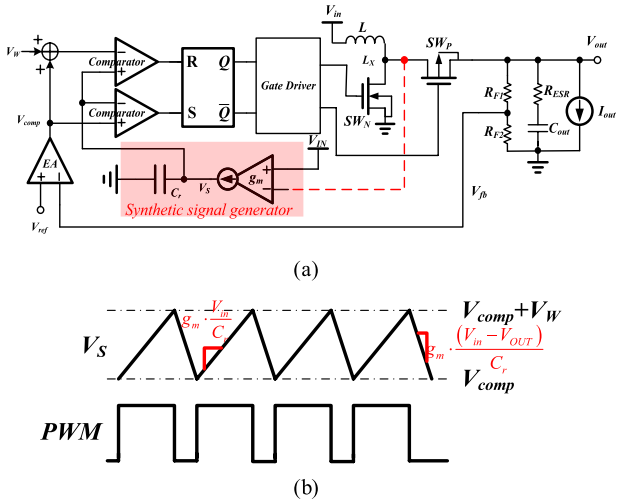

Fig. 2. (a) Synthetic current-ripple regulator. (b) Inductor current is emulated by the synthetic ripple which is a much cleaner signal.

To improve noise immunity and conquer the difficulty of realizing current-ripple control in boost converter, the synthetic-ripple modulator, which is shown in Fig. 2(a), is proposed to obtain an almost noise-free synthetic current ripple by integration [21], [22]. The synthetic-ripple capacitor C_r adopted in synthetic ripple generator is used to filter out the noise, as shown in Fig. 2(a). The waveform of synthetic current-ripple signal, V_s, is shown in Fig. 2(b). In addition, the introduction of the error amplifier can enhance regulation accuracy. The system, however, contains two poles, thus requiring a complex compensation network, such as the proportional–integral–differential (PID) compensator.

With the disadvantages in prior arts, the ripple-controlled technique should have the following advantages: the switching frequency should be nearly constant under steady-state condition and can be easily obtained for multiphase operation. In addition, the switching frequency can be extended to further reduce the switching power loss at light loads during standby operation. The accuracy of the load regulation has to be improved. In addition, dependence on large ESR, which improves noise immunity, should be minimized, thereby reducing transient voltage variation and output ripple.

This paper introduces a current-mode synthetic control (CSC) technique to include the dc inductor current information for simplifying compensation network. Because the noise immunity is improved by the CSC technique, the output ripple can be kept smaller than those in the prior arts with a small ESR value. Because a nearly constant switching frequency in steady state is maintained, the capability of the multiphase architecture is easily achieved. Furthermore, optimum and smooth transition between pulsewidth modulation (PWM) and pulse frequency modulation (PFM) modes is realized. That is, the switching period with CSC technique is extended to reduce the switching power loss and prolong the battery life of the portable devices during standby mode. The proposed CSC technique is introduced in Section II. The system stability analysis is described in Section III, showing the simplified compensation network. Circuit implementation is described in Section IV. The experimental results are shown in Section V. Finally, a conclusion is summarized in Section VI.

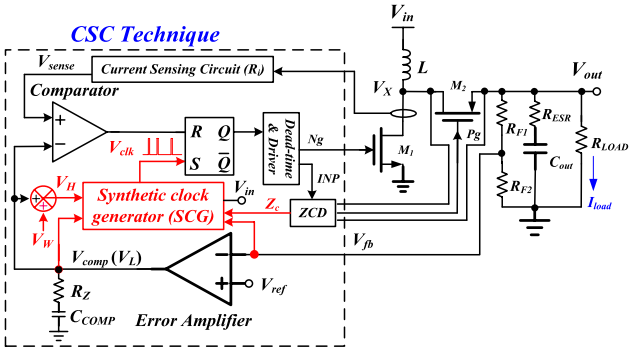

Fig. 3. Architecture of the proposed CSC circuit.

II. CSC Technique

The proposed CSC technique is shown in Fig. 3. Because the dc inductor current information is introduced, the compensation network is simplified from PID to PI compensator, which contains a resistor, R_Z, and a capacitor, $C_{\rm COMP}$. The inductor current is sensed by the current sensing circuit, R_i, to generate current sense signal, $V_{\rm sense}$, which contains dc inductor value and current ripple. The ripple of $V_{\rm sense}$ can be limited in the hysteresis window, V_W, equivalently. The error amplifier is adopted for load regulation improvement. Because the noise immunity is improved by the CSC technique, the output ripple can be kept smaller than those of the prior arts with small ESR value. In addition, the CSC technique contains a synthetic clock generator (SCG), which generate system clock, $V_{\rm clk}$, providing the nearly constant switching frequency during continuous conduction mode (CCM) operation and variable switching frequency during discontinuous conduction mode (DCM) operation for high efficiency. The zero-current detector (ZCD) is activated in the DCM operation.

A. Detail Operation of CSC

The current-mode hysteresis window is composed of the upper and the lower bound voltage, V_H and V_L, respectively. The hysteresis window of the proposed synthetic current-mode control is designed as the V_W, which is a constant value. The relationship between V_H and V_L can be shown in (1)

$$V_H = V_L + V_W$$

where

$$V_L = V_{\rm comp}. \tag{1}$$

Because worse load regulation performance in conventional current-mode hysteresis control comes from the lack of voltage regulation loop, V_L is equal to $V_{\rm comp}$ which is the output of the error amplifier in CSC control. That is, the proper definition of $V_L = V_{\rm comp}$ improves load regulation. During the increasing inductor current subinterval, the duty cycle is determined adequately by comparing the current sense signal, $V_{\rm sense}$, and $V_{\rm comp}$, as shown in Fig. 4(a). During the decreasing inductor current subinterval, SCG circuit emulates and follows the

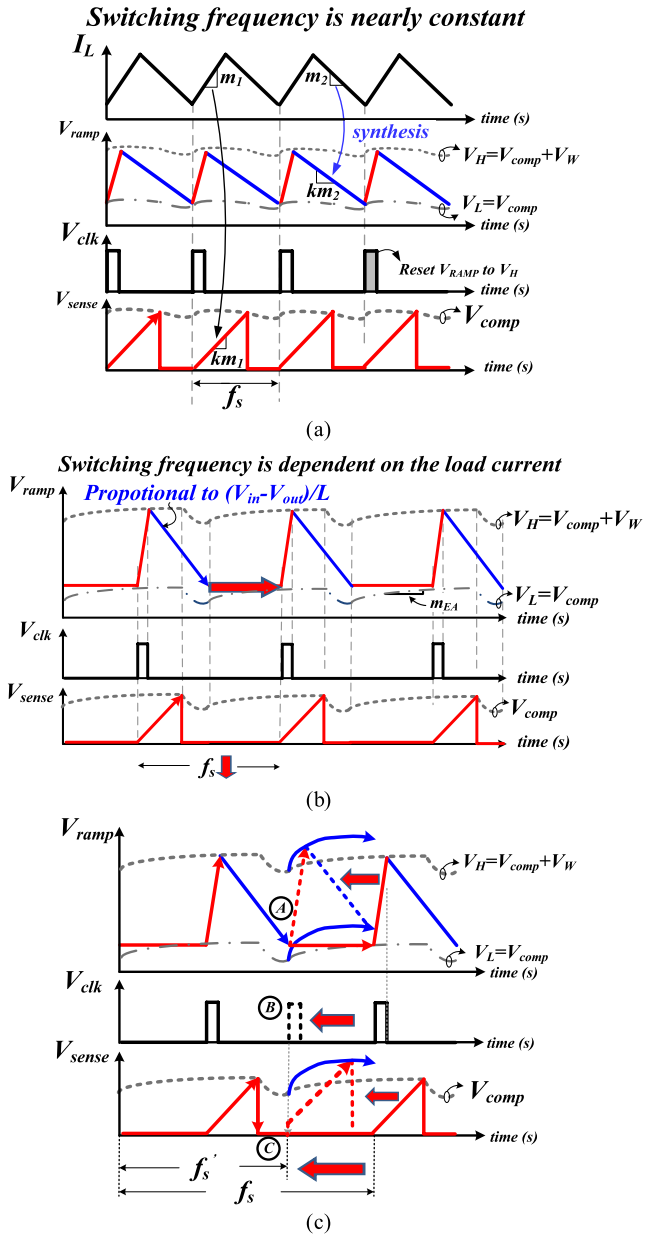

Fig. 4. CSC technique forces the system to operate in (a) CCM operation at heavy loads and (b) DCM operation at light loads for power saving. (c) Smooth transition between CCM and DCM operations.

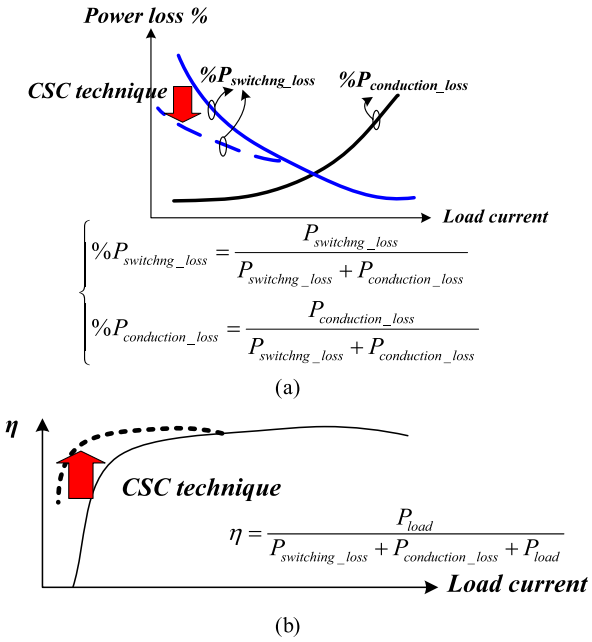

Fig. 5. CSC technique can (a) reduce the switching power loss and thus (b) improve the power conversion efficiency.

decreasing inductor current to generate the synthetic current ripple, V_{ramp}, with the slope which is proportional to m_2 by using the difference between V_{in} and V_{out}. To determine the switching frequency of CSC in CCM operation, V_{ramp} is limited in the hysteresis window, V_W. The switching frequency is expressed as (2)

$$f_{s(\text{CCM})} = \frac{\text{km}_2}{V_W}$$

where

$$m_2 = \frac{(V_{\text{out}} - V_{\text{in}})}{L} \propto (V_{\text{out}} - V_{\text{in}}) \tag{2}$$

where V_{in} is the input voltage, V_{out} is the output voltage, L is the inductor value, m_2 is the slope of decreasing inductor current, and k is the proportionality constant. It can be observed that switching frequency in CCM operation is nearly constant with a fixed hysteresis window and input and output conditions.

By the SCG circuit, the synthetic clock signal, V_{clk}, which shows the beginning of each switching period, maintains nearly constant switching frequency and output voltage ripple in CCM. To ensure the accuracy of switching frequency, V_{clk} should be a small pulse to reset V_{ramp} to its initial state V_H. A large V_{clk} width causes a frequency deviation because of the offset between V_{ramp} and V_{sense}.

B. Modulation Method in Different Load Conditions

At heavy loads, the system is in CCM operation. The system switching frequency depends on hysteresis window V_W. Fig. 4(a) shows that the switching frequency is nearly constant during CCM operation to ensure high driving capability and constant frequency operation. Accuracy is guaranteed compared with the prior arts.

On the other hand, the system is in DCM operation at light loads. In contrast to the PWM control, the switching period is extended to reduce switching power loss in DCM operation. Fig. 4(b) shows that during the DCM operation, the synthetic current-mode waveform is kept constant once the inductor current becomes zero, as detected by the ZCD. In other words, the off-time is extended if the signal Z_C is equal to one when ZCD detects zero inductor current. The output load is simply supplied by the output capacitor, C_{out}, because both M_1 and M_2 in Fig. 3 are switched off. The decreasing output voltage gradually causes the increasing in V_{comp} to be higher than the V_{ramp}, again. Therefore, the switching frequency during the DCM operation is reduced to further minimize switching power loss and increase the conversion efficiency at light loads, as shown in Fig. 5(a) and (b), respectively. The switching

frequency dependent on load current makes the switching power loss proportional to the switching frequency.

At very light loads, the on-time of M_1 is further reduced to decrease the average inductor current. Therefore, the zero-current period increases significantly and occupies most of the switching periods. The slope of increasing in V_{comp} can be derived in (3)

$$m_{\text{EA}} = \frac{dV_{\text{comp}}}{dt} \approx \frac{g_{m(\text{EA})}}{C_{\text{COMP}}} \frac{I_{\text{load}}}{C_{\text{out}}} \frac{1}{f_{s(\text{DCM})}}. \tag{3}$$

In DCM operation, the switching frequency is determined by the hysteresis window, V_W. Thus, the value of m_{EA} can decide the switching frequency, as shown in (4)

$$f_{s(\text{DCM})} \geq \frac{m_{\text{EA}}}{V_W} = \sqrt{\frac{I_{\text{load}} g_{m(\text{EA})}}{V_W C_{\text{out}} C_{\text{COMP}}}} \tag{4}$$

where $g_{m(\text{EA})}$ is the transconductance of the error amplifier, C_{COMP} is the compensation capacitor in Fig. 3, I_{load} is the loading current, C_{out} is the output capacitor, and V_W is the hysteresis window. As shown in (4), the switching frequency decreases with the reduction of load current.

C. Smooth Transition Between CCM and DCM

In current-mode PWM control, the system enters into DCM operation with a constant switching frequency at light loads [23]. To obtain high efficiency, PFM can be included in the conventional current-mode control. Unfortunately, the transition between PWM and PFM will induce a large transient voltage variation [8], [24], [25]. In addition, optimum and smooth transition between PWM and PFM is hard to attain because of variations of loading or input/output condition. In contrast, the CSC technique can smoothly decrease the load-dependent switching frequency at light loads and achieve optimal mode transition.

Fig. 4(c) shows that the CSC technique can smoothly transit from DCM to CCM when the load current changes from light to heavy. As load current increase at point A, the lack of energy at V_{out} causes V_{comp} to increase, thereby raising the hysteresis window. The increase in V_{comp} results in the decrease in zero inductor current periods and forces the operation mode entering into the CCM at point A. The advance of V_{clk} pulse at point B increases the switching frequency from f_s to f_s'. On the contrary, the mode transition from CCM to DCM can be achieved spontaneously. Therefore, a smooth transition between DCM to CCM ensures smaller output ripples comparing with the prior arts with PWM/PFM hybrid mode control.

D. Compact Design Between Output Ripple and Switching Frequency

The voltage ripple can be reduced with higher switching frequency. Thus, a converter with low frequency suffers from worse ripple performance and larger output voltage drop. In addition, an annoying sound is produced when switching frequency is near or below the audio frequency. Therefore, the modified DCM operation is shown in Fig. 6. After a zero current is detected by ZCD, V_{ramp} slowly ramps down with

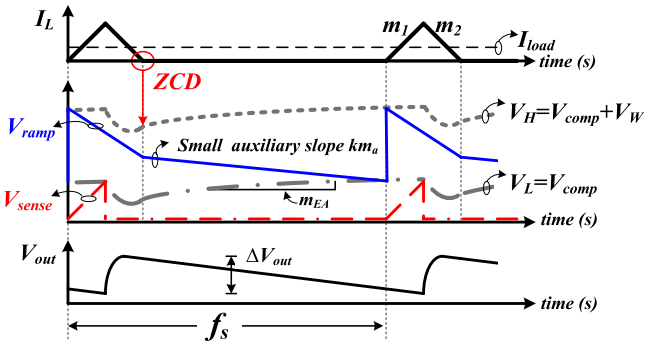

Fig. 6. Modified DCM operation in CSC technique, which introduces the small auxiliary slope m_{a} after the zero current is detected.

the small auxiliary slope km_a rather than keeping constant in Fig. 4(b) to prevent the converter operating at a very low switching frequency. At very light-load condition, the switching frequency can be derived by modifying (4) and expressed in (5)

$$f_{s(\text{DCM,aux})} \geq \frac{\text{km}_a}{2V_W} + \sqrt{\left(\frac{\text{km}_a}{2V_W}\right)^2 + \frac{I_{\text{load}} g_{m(\text{EA})}}{V_W C_{\text{out}} C_{\text{COMP}}}} \tag{5}$$

where $g_{m(\text{EA})}$ is the transconductance of the error amplifier, C_{COMP} is the compensation capacitor in Fig. 3, I_{load} is the loading current, C_{out} is the output capacitor, V_W is the hysteresis window, and km_a is the small auxiliary discharge slope. As shown in (5), the auxiliary slope helps to suppress the reduction of switching frequency effectively. Furthermore, even if the load current is equal to zero, the switching frequency is able to be kept beyond audio frequency band (20 Hz–2 kHz). As shown in (6), the minimum switching frequency can be properly designed considering the maximum allowable output ripple, ΔV_{OUT}

$$f_{s(\text{DCM,aux})}\big|_{I_{\text{load}}=0} = \frac{\text{km}_{\text{a}}}{V_W} > 20\ \text{kHz} > f_{s(\text{DCM})}. \tag{6}$$

III. Circuit Implementation

A. Synthetic Clock Generator

As shown in Fig. 7(a), the SCG circuit, which ensures nearly constant switching frequency in CCM operation, includes two parts—high linearity in–out subtractor in Fig. 7(b) and hysteresis clock generator in Fig. 7(c). To emulate the decreasing inductor current, discharging current I_{diff} is generated by the difference of V_{in} and V_{out}. Hysteresis clock generator limits V_{ramp} between V_H and V_L for current-mode hysteresis control. The switching frequency and V_{clk} are determined by hysteresis clock generator with the dependence on the operation mode, which is represented by zero-current detection signal, Z_C.

In Fig. 7(b), V_{inFF} (a scaled-down V_{in}) and V_{fb} (a scaled-down V_{out}) are level shifted by folded flipped voltage followers (FFVFs) to V_{inFF}' and V_{fb}', respectively, as shown in (7) [22], [26]

$$V_{\text{fb}} - V_{\text{inFF}} = V_{\text{fb}}^{'} - V_{\text{inFF}}. \tag{7}$$

FFVFs can ensure wide input range and high linearity. The voltage difference crossing on the resistor, R_{gm}, generates the

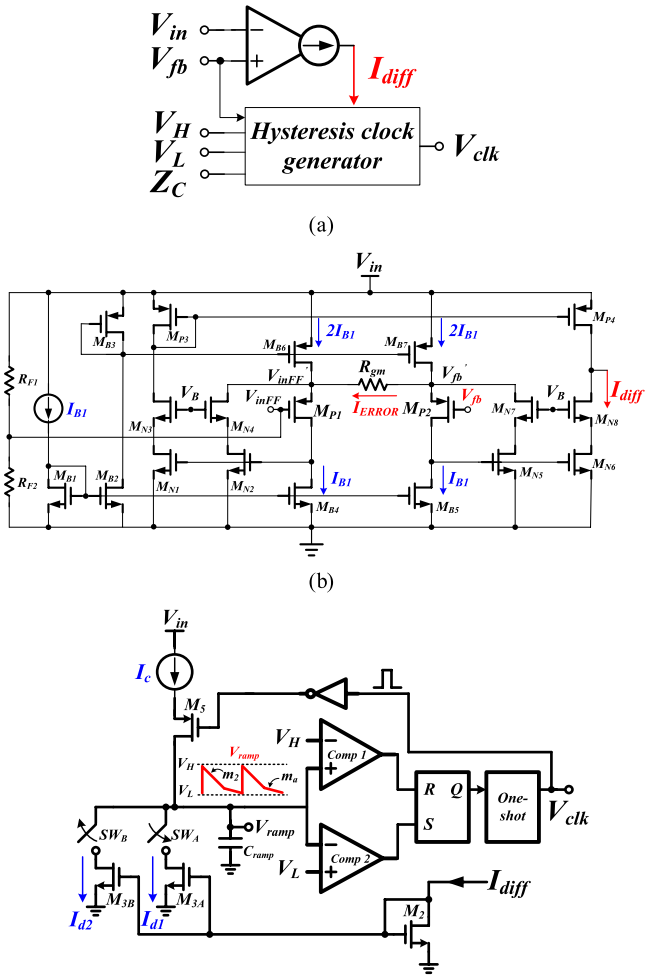

Fig. 7. (a) Proposed SCG circuit in the CSC technique. (b) In–out subtractor. (c) Hysteresis clock generator.

error signal, I_{ERROR}, and is mirrored to the output of in–out subtractor. Finally, I_{diff}, which is proportional to the difference between V_{in} and V_{out}, is obtained and expressed as (8)

$$\begin{aligned} I_{\text{diff}} &= 2I_{\text{ERROR}} \\ &= 2\frac{V_{\text{fb}} - V_{\text{inFF}}}{R_{\text{gm}}} \\ &= 2\beta\frac{V_{\text{out}} - V_{\text{in}}}{R_{\text{gm}}} \propto V_{\text{out}} - V_{\text{in}} \end{aligned}$$

where

$$\beta = \frac{R_{F2}}{R_{F1} + R_{F2}} \qquad V_{\text{inFF}} = \beta V_{\text{in}} \qquad V_{\text{out}} = \beta V_{\text{fb}}. \quad (8)$$

Fig. 7(c) shows that I_{diff} is mirrored by transistors $M_{3\text{A}}$ and $M_{3\text{B}}$ to constitute discharging currents I_{d1} and I_{d2}, which form the slopes of m_2 and m_{a}, respectively. The upper bound voltage, V_H, defines the starting point of the emulation of the decreasing inductor current. At the start of the switching period, the transistor M_5 introduces charging current I_c, which is much higher than I_{d1} and I_{d2}, flowing into the ramp capacitor C_{ramp} to ramp up V_{ramp} rapidly to the V_H. On the other hand, the lower bound voltage, V_L, determines the end

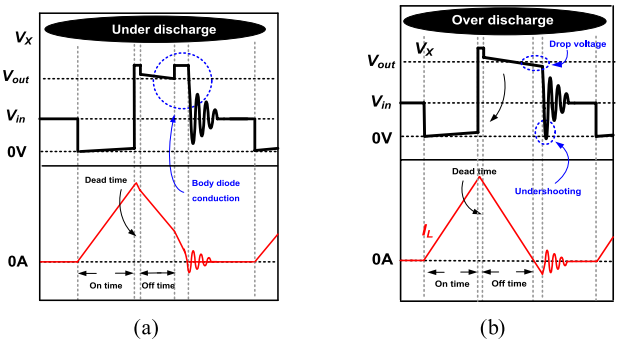

Fig. 8. ZCD operation. Off-time is too (a) long and (b) short.

time of the decreasing inductor current, that is, the next starting point of the switching period.

In the DCM operation at light loads, switch SW_A turns off and switch SW_B turns on when the ZCD circuit senses zero inductor current. Transistor I_{3B} discharges C_{ramp} with the auxiliary slope m_a. Thus, the switching frequency decreases to reduce the switching power loss and efficiency can be improved at light loads, as shown in (5).

B. Zero-Current Detector

The accuracy of ZCD affects the power conversion efficiency at light loads. Generally, implementation of zero-current detection involves the use of a simple comparator by directly comparing switching node V_X and V_{out} in Fig. 3 [22], [27]. The comparator offset voltage and the driver's propagation delay, however, postpone the turnoff timing of the high-side power switch (M_2 in Fig. 3), resulting in negative inductor current and the degradation of power conversion efficiency at light loads.

Fig. 8 shows examples of nonoptimal zero-current switching. If the zero-current switching is activated too early, the high-side power switch is disabled with a positive inductor current value. Therefore, the parasitic diode at the high-side power switch will be turned on automatically to conduct the inductor current, as shown in Fig. 8(a). V_X is stretched to a voltage value higher than V_{out} because of a conductive drop voltage of body diode, which is typically 0.7 V. On the other hand, a reverse inductor current occurs with the detection delay of zero inductor current, as shown in Fig. 8(b). Before the high-side power switch turns off, a deep undershoot of V_X occurs, and V_X is lower than V_{out} until the ringing phenomenon happens. This reverse current phenomenon causes energy loss and low power efficiency.

Thus, the ZCD circuit, which calibrates the zero crossing point according to the comparator offset and propagation delay, is proposed, as shown in Fig. 9. The offset and delay are measured first at the wafer level; then, a seven-bit calibrator is used to calibrate the offset voltage or delay. Three test pads are placed in V_X, V_{out}, and ZCD. A ramped-down test voltage at V_X with an initial value higher than V_{out} is applied to monitor the ZCD signal. Ideally, the ZCD signal is triggered from low to high when V_X is equal to V_{out}. The input offset voltage of comparator X_2 can be obtained according to the delay or

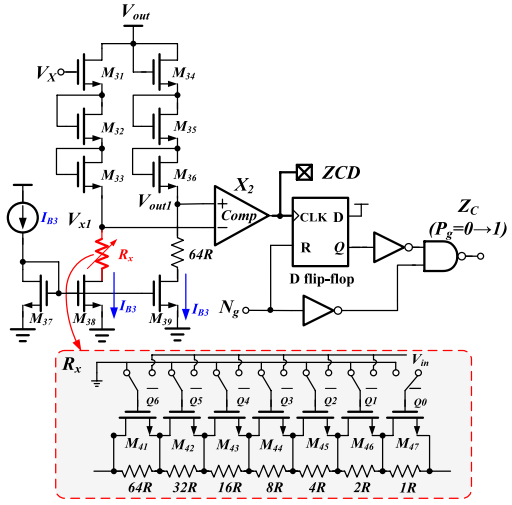

Fig. 9. Proposed ZCD circuit with self-calibration.

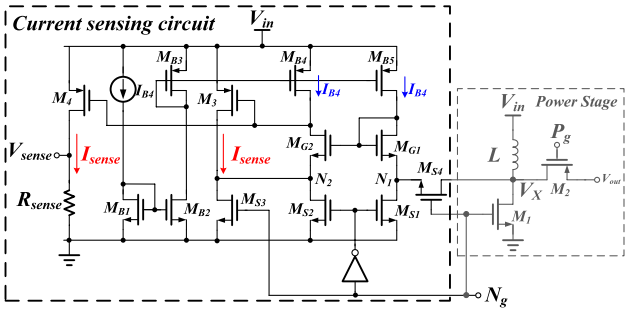

Fig. 10. Proposed current sensing circuit.

postponement level of ZCD signal. The resistor string, R_x, is then adjusted by the trimming method to find the optimal zero-current switching point. This test method also can be used to calibrate the delay between ZCD and P_g (gate driver of M_2 in Fig. 3) by measuring the delay time. The same process is applied while the triggered signal is changed at P_g.

C. Current Sensing Circuit

Fig. 10 shows the proposed current sensing circuit. Transistors M_{S1}, M_{S2}, and M_{S4} are the required switches for turning on/off during sensing procedure. Transistor M_{S3} is the sensing MOS with the scaled down ratio of N-type power MOSFET, M_1. During the inductor-charging period, N_g is equal to V_{in} to turn on M_1 and M_{S3} simultaneously. M_{S2} and M_{S1} are turned off, and M_{S4} is turned on to transmit the voltage of V_X to node, N_1. With the common-gate amplifier, which is composed of M_{G1} and M_{G2}, node N_2 can be tracked to the N_1. Therefore, the sensed current, I_{sense}, which is the scaled down of the inductor current by the aforementioned ratio, is generated automatically by M_{S3} and mirrored by M_3 and M_4 to flow through R_{esnes}. Finally, the current sensed signal, V_{sense}, is obtained.

D. Error Amplifier With On-Chip Compensator

Fig. 11 shows the proposed design of the error amplifier and the on-chip compensator. To reduce the die area and achieve

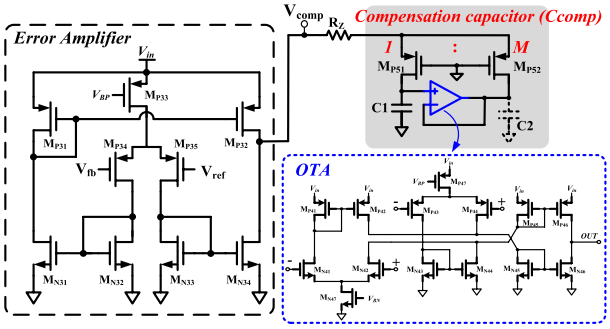

Fig. 11. Schematic view of the error amplifier with the on-chip compensator and the CM technique.

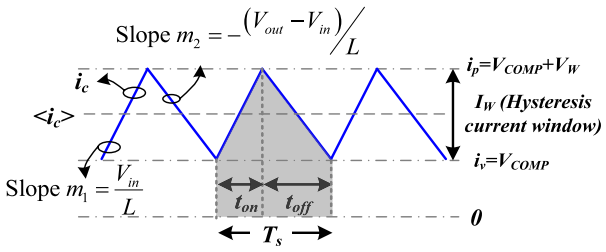

Fig. 12. Synthetic waveform is limited within the hysteresis window defined by the synthetic-ripple control.

the goal of system on a chip, an on-chip compensator using capacitance multiplier (CM) technique is adopted [19], [28]. Capacitor C_1, which is a pure capacitor with the value of 6 pF, is greatly amplified by CM technique. The effective capacitance is expressed in (9)

$$C_{\text{comp}} = C_1 \times (1 + M) \tag{9}$$

where M is the mirror ratio between transistors M_{P51} and transistor M_{P52}. In addition, a small capacitor C_2 is introduced to reduce the transient noise and adjust transient performance.

IV. System Stability Analysis

Small-signal modeling and system stability compensation for both conventional synthetic current-ripple regulator and the proposed CSC technique are analyzed and compared as follows.

A. Small-Signal Modeling of Conventional Synthetic Current Tipple Hysteresis Mode Modulator

Fig. 12 shows that the conventional synthetic current-ripple hysteresis mode modulator limits the inductor current ripple within the hysteresis current window (I_W) with upper and lower bound current, i_p and i_v, respectively.

The switching period, T_s, is equal to the summation of t_{on} and t_{off} in the CCM operation. Considering the small-signal analysis, the value of each variable can be written as the summation of the dc term and its perturbation. After linearization, (11)–(14) can be derived from (10)

$$\frac{I_W}{T_{\text{off}}(t)} = m_2(t) \quad T_s(t) = T_{\text{on}}(t) + T_{\text{off}}(t) \tag{10}$$

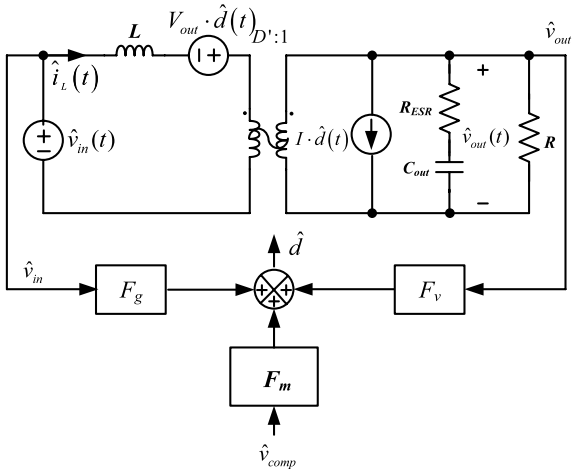

Fig. 13. Small-signal model of the conventional current-ripple hysteresis mode modulator.

where

$$V_W = kI_W$$

$$\hat{t}_{\text{off}} = -\frac{I_W \cdot L \cdot (\hat{v}_{\text{out}} - \hat{v}_{\text{in}})}{(V_{\text{out}} - V_{\text{in}})^2} \tag{11}$$

$$\hat{t}_s = \hat{t}_{\text{on}} - \frac{I_W \cdot L \cdot (\hat{v}_{\text{out}} - \hat{v}_{\text{in}})}{(V_{\text{out}} - V_{\text{in}})^2} \tag{12}$$

$$\hat{i}_p = \hat{i}_c + \frac{\left(V_{\text{in}}\hat{t}_{\text{on}} + T_{\text{on}}\hat{v}_{\text{in}}\right)}{2L} \tag{13}$$

$$\hat{t}_{\text{on}} = \frac{2L}{V_{\text{in}}}(\hat{i}_P - \hat{i}_c) - \frac{T_{\text{on}}}{V_{\text{in}}}\hat{v}_{\text{in}}. \tag{14}$$

Therefore, the $\hat{d}$ can be derived as (15)

$$\begin{aligned}\hat{d} &= \frac{D'\hat{t}_{\text{on}} - D\hat{t}_{\text{off}}}{T_s} \\ &= \left(D'\left(\frac{2L}{V_{\text{in}}}\left(\hat{i}_p - \hat{i}_c\right) - \frac{T_{\text{on}}}{V_{\text{in}}}\hat{v}_{\text{in}}\right)\right. \\ &\quad \left. + \frac{L \cdot I_W \cdot D}{(V_{\text{out}} - V_{\text{in}})^2}\left(\hat{v}_{\text{out}} - \hat{v}_{\text{in}}\right)\right) \cdot (T_s)^{-1}.\end{aligned} \tag{15}$$

Simplifying (15), can be shown as (16)

$$\hat{d} = F_m \cdot \left[\left(\widehat{i_p} - \widehat{i_c}\right) + F_g\hat{v}_{\text{in}} + F_v\hat{v}_{\text{out}}\right]$$

where

$$F_m = \frac{2D \cdot D'}{V_W},\ F_g = -\frac{1}{V_{\text{out}}} \cdot \frac{I_W}{2DD'},\ F_v = \frac{D'}{V_{\text{out}}} \cdot \frac{I_W}{2DD'}. \tag{16}$$

With synthetic current-ripple operation, the inductor current can be expressed as (17)

$$i_c(t) = \frac{g_m}{C_r}V_{\text{in}}(t) \cdot T_{\text{on}}(t). \tag{17}$$

Then, the $(\hat{i}_P - \hat{i}_c)$ term can be expressed as (18)

$$(\hat{i}_P - \hat{i}_c) = \widehat{i_p}\left(\frac{C_r + g_m \cdot (2L)}{C_r}\right). \tag{18}$$

Thus, (15) can be expressed as (19)

$$\hat{d} = F_m \cdot \left[\left(1 + \frac{g_m \cdot (2L)}{C_r}\right)\left(\widehat{i_p}\right) - F_g \cdot\hat{v}_{\text{in}} + F_v \cdot \hat{v}_{\text{out}}\right]. \tag{19}$$

TABLE I
PARAMETERS IN (21)

G_{vc0}	$\omega_{z(RHP)}$	$\omega_{z(ESR)}$	ω_{p1} and ω_{p2} (complex pole)
$F_m \cdot \frac{V_{out}}{D'}$	$\frac{(D')^2 R}{L}$	$\frac{1}{R_{ESR}C_{out}}$	$\frac{-\frac{2\zeta}{\omega_0} + \sqrt{\left(\frac{2\zeta}{\omega_0}\right)^2 - \frac{4}{\omega_0^2}}}{2\left(\frac{1}{\omega_0^2}\right)} \approx \omega_0$

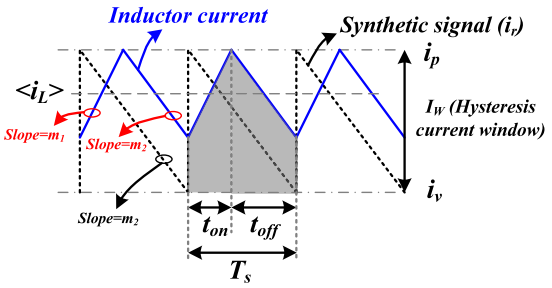

Fig. 14. Synthetic waveform is limited with the hysteresis window defined by the CSC technique.

Consequently, the conventional synthetic current-ripple hysteresis converter is similar to voltage-mode controlled converter [29] because the duty variation, $\hat{d}$, does not contain the dc inductor current information, which can be verified in (19).

The small-signal model of the conventional synthetic current-ripple hysteresis mode modulator is shown in Fig. 13, and the control-to-output transfer function is shown in (20). R is the output resistance, and R_{ESR} is the ESR of output capacitor C_{out}

$$G_{\text{vc}} = \frac{\hat{v}_{\text{out}}}{\hat{v}_{\text{comp}}} = \frac{F_m \cdot G_{\text{vd}}}{1 - F_v \cdot G_{\text{vd}}}$$

where

$$G_{\text{vd}} = \left.\frac{\hat{v}_{\text{out}}}{\hat{d}}\right|_{\hat{v}_{\text{in}}=0} = \frac{V_{\text{out}}}{D'} \cdot \frac{\left(1 - s\frac{L}{D'^2R}\right)(1 + sR_{\text{ESR}}C_{\text{out}})}{1 + s\frac{L}{\text{RD}'^2} + s^2\frac{LC_o}{D'^2}}. \tag{20}$$

Therefore, G_{vc} can be simplified as (21) with two poles and two zeros, including one right-half-plane (RHP) zero and one left-half-plane (LHP) zero [23], [30]–[32]. The parameters are shown in Table I

$$G_{\text{vc}} = G_{vc0} \cdot \frac{\left(1 - \frac{s}{\omega_{z(\text{RHP})}}\right)\left(1 + \frac{s}{\omega_{z(\text{ESR})}}\right)}{1 + \frac{2\zeta}{\omega_0}s + \frac{s^2}{\omega_0^2}}. \tag{21}$$

Obviously, the system contains a pair of complex pole and two zeros, including one RHP zero and one LHP zero. The frequency response of the conventional synthetic current-ripple hysteresis mode modulator is similar to that of the voltage-mode PWM technique [29]. Thus, PID compensation should be used for the system stability.

B. Small-Signal Modeling of the Proposed CSC Technique

Fig. 14 shows that the CSC technique limits the inductor current within the hysteresis current window, with the upper

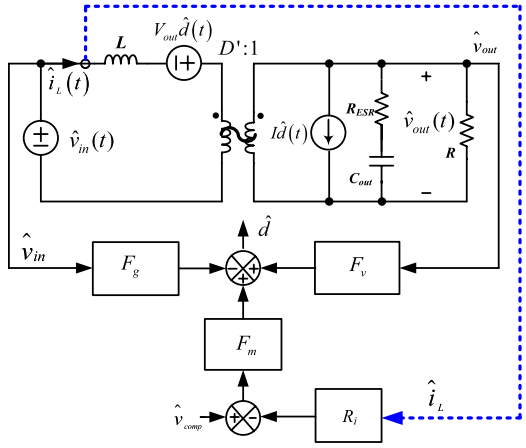

Fig. 15. Small-signal model of the proposed CSC technique.

TABLE II
PARAMETERS OF SMALL-SIGNAL MODEL IN THE PROPOSED CSC TECHNIQUE

G_{vc0}	$\omega_{z(RHP)}$	$\omega_{z(ESR)}$	ω_{p1} (single pole)
$\frac{D'R}{2R_i}$	$\frac{(D')^2R}{L}$	$\frac{1}{R_{ESR}C_{out}}$	$\frac{2}{RC_{out}}$

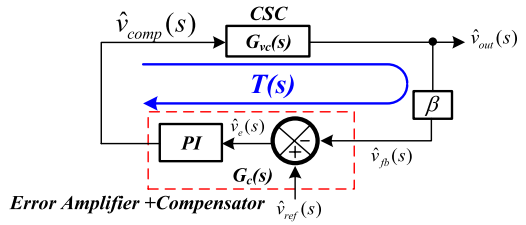

Fig. 16. Closed-loop diagram of the boost converter using the CSC technique.

and lower current bounds i_p and i_v, respectively. The current sensing circuit (R_i) senses the positive slope of the inductor current. Thus, the on-time value t_{on} is decided by comparing the inductor current with i_p. On the other hand, the negative slope of i_r, which is formed by the SCG circuit of the CSC technique, can determine the off-time t_{off} value once i_r is smaller than the i_v.

Similarly, the d can be obtained in (23) from (22)

$$\frac{I_W}{T_s(t)} = m_2(t)$$

and

$$\langle i_p \rangle = \langle i_L \rangle + m_1(t) \cdot dT_s \tag{22}$$
$$\hat{d} = F_m \cdot \left[(\hat{v}_{\text{comp}} - R_i \cdot \hat{i}_L) + F_v \hat{v}_{\text{out}} - F_g \hat{v}_{\text{in}} \right]$$

where

$$F_m = \frac{2 \cdot D}{I_W \cdot D' \cdot R_i},\ F_g = \frac{I_W \cdot R_i}{2 \cdot D \cdot V_{\text{out}}},\ F_v = \frac{D' \cdot I_W \cdot R_i}{2 \cdot D \cdot V_{\text{out}}}. \tag{23}$$

The small-signal model of the proposed CSC technique is shown in Fig. 15, and G_{vc} can be derived as (24)

$$G_{\text{vc}} = \frac{\hat{v}_{\text{out}}}{\hat{v}_{\text{comp}}} = \frac{F_m \cdot G_{\text{vd}}}{1 - F_v \cdot G_{\text{vd}} + F_m \cdot G_{\text{id}} \cdot R_i}. \tag{24}$$

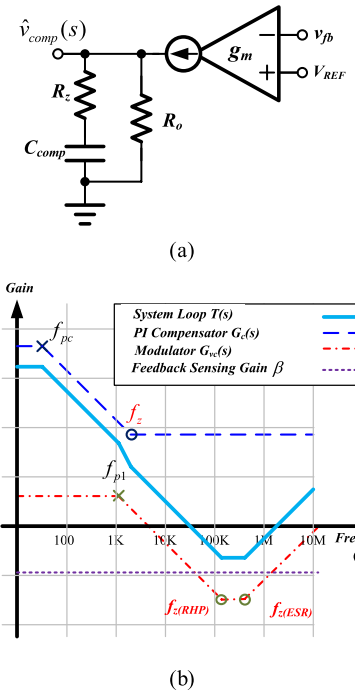

Fig. 17. Error amplifier with the PI compensator. (b) Bode plot of the closed-loop gain $T(s)$.

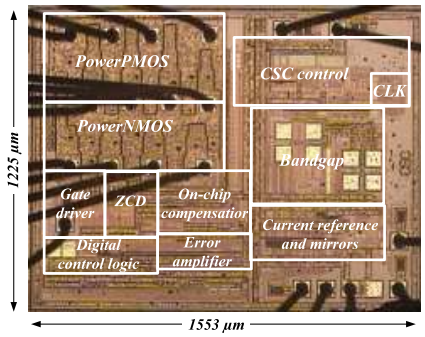

Fig. 18. Chip micrograph of the proposed converter.

TABLE III
DESIGN SPECIFICATIONS

PARAMETERS	VALUE	UNIT
Supply variation (V_{in})	2.5 - 4.2	V
Output voltage (V_{out})	5	V
Undershoot voltage recovery time @ I_{load} changes from 200 mA to 400 mA	60	μs
Overshoot voltage recovery time @ I_{load} changes from 400 mA to 200 mA	68	μs
Maximum load current	500	mA
Inductor (L)	1	μH
Capacitor (C_{out})	10	μF
Equivalent series resistor (R_{ESR})	20	mΩ
Switching frequency	2-5	MHz
Line regulation	0.3	%
Load regulation	5	%/A
efficiency	78-90	%

The designed value of $F_m \cdot G_{\text{id}} \cdot R_i$ is much larger than that of $1 - F_v \cdot G_{\text{vd}}$. Thus, the G_{vc} can be simplified as (25), and

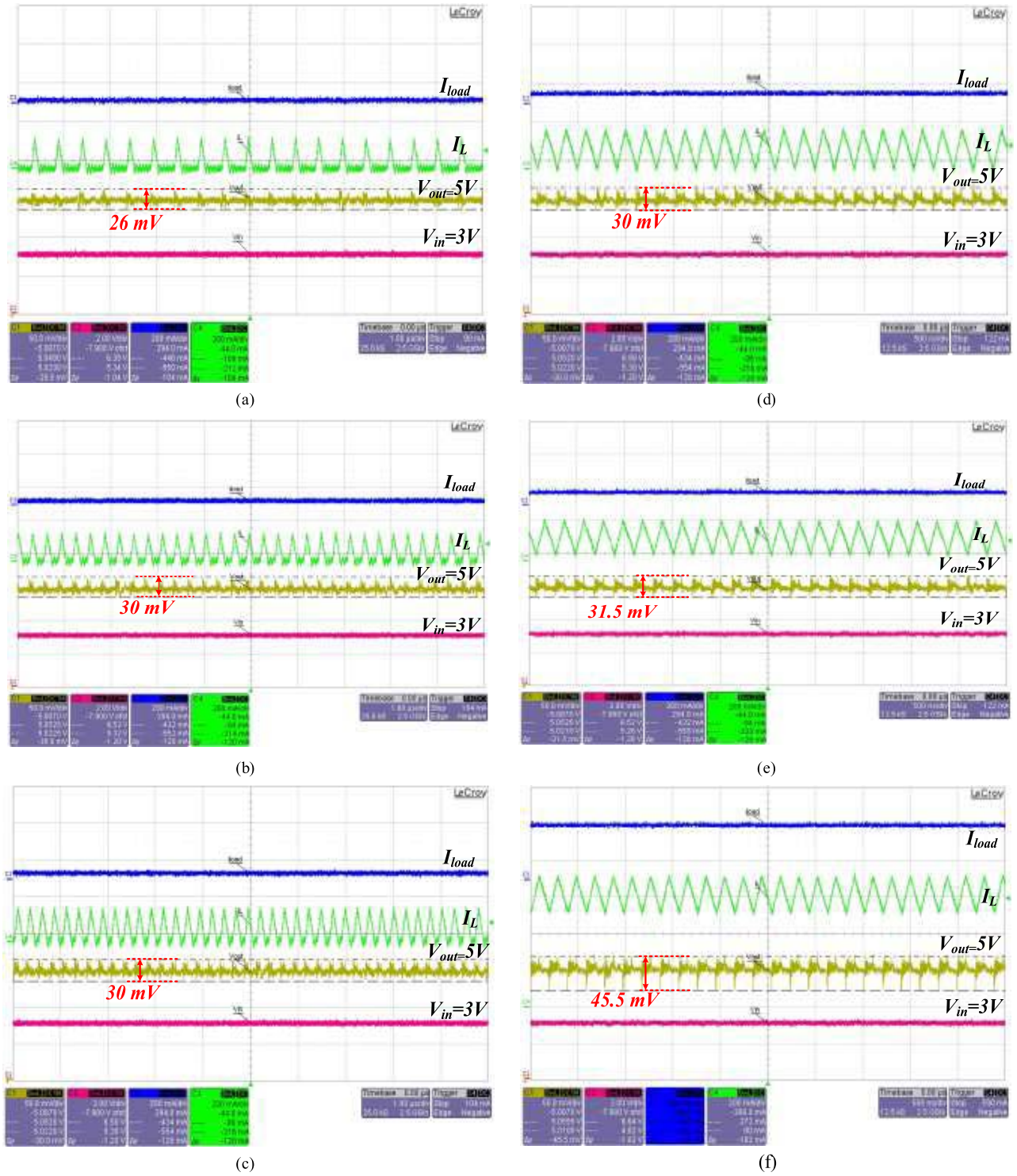

Fig. 19. Output ripple and switching frequency in DCM operation under different load current conditions. (a) $I_{\text{load}} = 10$ mA. (b) $I_{\text{load}} = 20$ mA. (c)$I_{\text{load}} = 30$ mA. (d) $I_{\text{load}} = 50$ mA. (e) $I_{\text{load}} = 70$ mA. (f) $I_{\text{load}} = 300$ mA.

the parameters are shown in Table II

$$G_{\text{vc}} = \frac{\hat{v}_{\text{out}}}{\hat{v}_{\text{comp}}} = \frac{F_m \cdot G_{\text{vd}}}{F_m \cdot G_{\text{id}} \cdot R_i} = G_{\text{vc0}} \cdot \frac{\left(1 - \frac{s}{\omega_{z(\text{RHP})}}\right)\left(1 + \frac{s}{\omega_{z(\text{ESR})}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)}. \quad (25)$$

Obviously, the system contains only one dominate pole and two zeros, which includes one RHP zero and one LHP zero. The frequency response of the CSC technique is similar to that of the current-mode PWM technique [33]–[40]. In other words, PI compensation is suitable and can be easily implemented on the chip [19], [28]. In addition, the advantage of the proposed CSC technique is verified by the removal of the slope compensation required in conventional

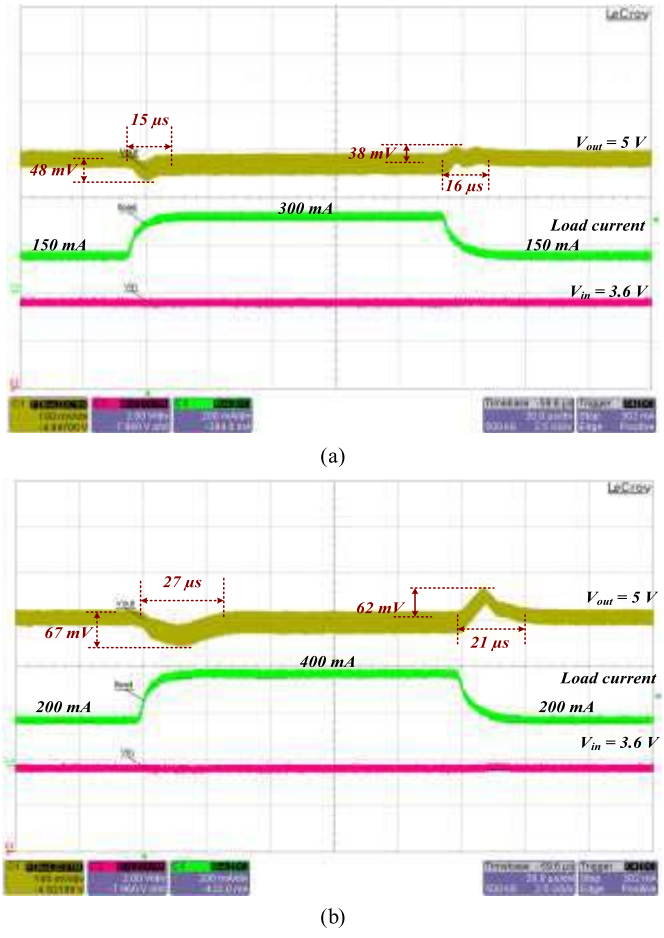

Fig. 20. Measurement results of the proposed converter with load transient ranges from (a) 150 to 300 mA and (b) 200 to 400 mA.

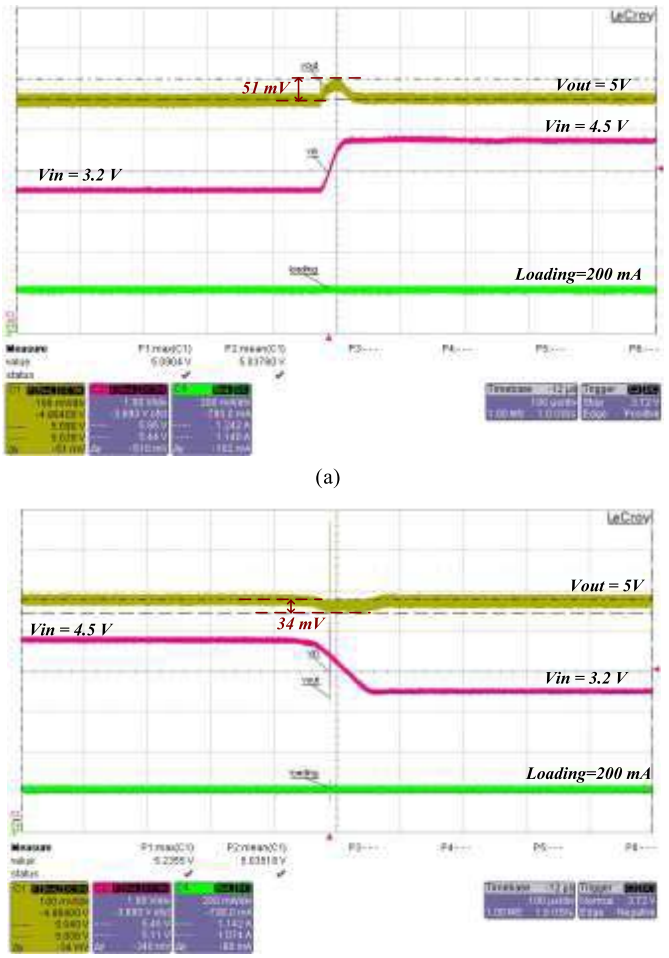

Fig. 21. Measurement results of the proposed converter with line transient changes from (a) 3.2 to 4.5 V and (b) 4.5 to 3.2 V.

current-mode PWM control. That is, the proposed CSC technique simplifies the compensation process and improves the power conversion efficiency at light loads because of the load-dependent switching frequency, which is more suitable for portable devices to extend the battery life.

C. Loop Gain Analysis With PI Compensator for the System Stability

Fig. 16 shows the closed-loop diagram of the boost converter using the CSC technique. The closed-loop gain $T(s)$ is expressed in (26). β is the sensor gain, which is equal to $R_{F2}/(R_{F1}+R_{F2})$. $G_c(s)$ is the compensation transfer function composed of an error amplifier and a PI compensator, as shown in Fig. 17(a). The PI compensator contributes one low-frequency pole-zero pair, ($\omega_{\rm pc}$ and ω_z)

$$T(s) = \beta \cdot G_{vc}(s) \cdot G_c(s). \tag{26}$$

ω_{pc} is the dominant pole and ω_z cancels the effect of the output pole ω_{p1}. As a result, the gain-bandwidth of the system expands. Simultaneously, the dc gain is enlarged to enhance load regulation of the system because of the high-gain error amplifier. The Bode plot of the proposed system with the compensator is shown in Fig. 18(b). $\omega_{\rm pc}$ and ω_z are expressed as (27). g_m and R_o are the transconductance and the output resistance of the error amplifier, respectively. R_z and $C_{\rm comp}$ are the compensation resistor and capacitor, respectively

$$\omega_{\rm pc} = 2\pi f_{\rm pc} = \frac{1}{R_o \cdot C_{\rm comp}}$$

and

$$\omega_z = 2\pi f_z = \frac{1}{R_z \cdot C_{\rm comp}}. \tag{27}$$

V. Experimental Results

The test chip was fabricated using the UMC 0.3-μm BCD process with a small inductor for compact printed-circuit board area. The chip micrograph is shown in Fig. 18. The chip area is 1553 μm $\times$ 1225 μm, and the specifications of this proposed design is listed in Table III.

Fig. 19 shows the output ripple and switching frequency in the DCM and CCM operations under different load current conditions. The variable switching frequency can ensure reduction of the switching power loss.

The output voltage and the inductor current waveforms during load transient response are shown in Fig. 20. The settling times when $V_{\rm in}$ = 3.6 V are $\sim$15 and 16 μs when the load

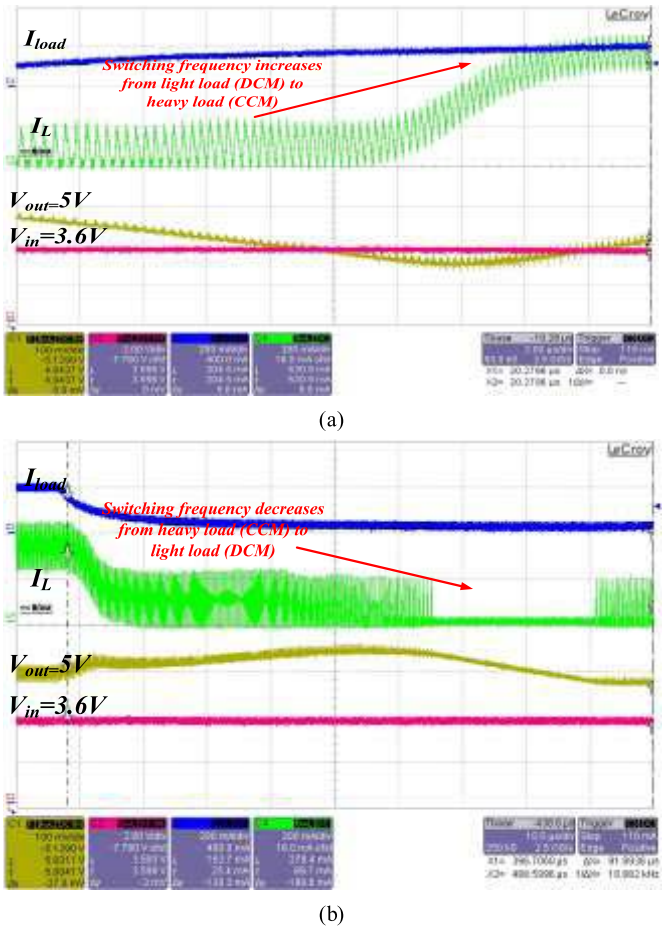

Fig. 22. Measurement results of the proposed converter with load transients (9) from (a) 25 to 200 mA and (b) 200 to 25 mA.

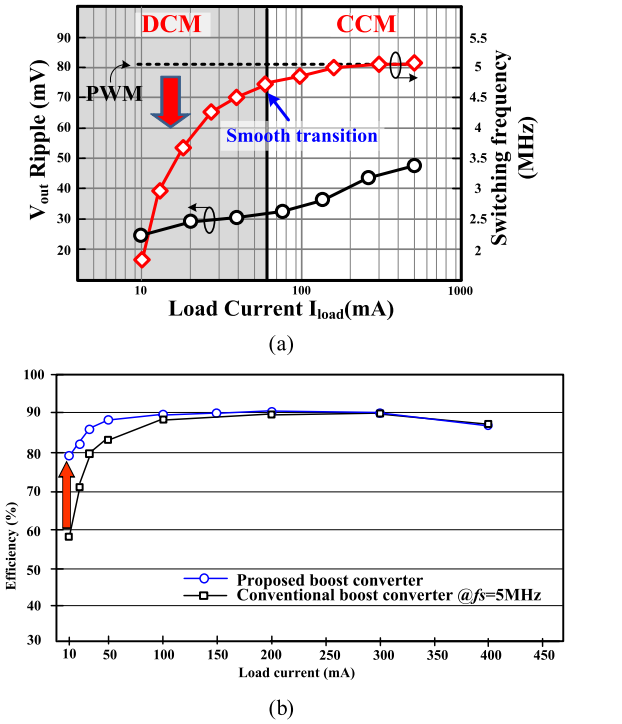

Fig. 23. Performance of (a) switching frequency and output ripple and (b) efficiency during the load range.

TABLE IV
COMPARISON TABLE

	[41]	[42]	[22]	This work
Control method	Adaptive-on-time	Adaptive Droop Resistance Technique	WTE technique	CSC technique
Process	0.35 μm	0.25 μm	0.4 μm	0.3 μm
V_{in}/V_{out} (V)	1.8-3.2/3.0-4.2	2.8-3.2/6	2.7-4.3/2.7-5	2.5-4.2/5
Load regulation (%/A)	N/A	10	N/A	5
Recovery time (μs/mA)	0.0139	0.125	0.3	0.135
Load transient droop (mV)	240 (Max.)	75 (Max.)	90 (Max.)	67 (Max.)
Efficiency (%)	68-94.5	80-92	65-90	78-90
Switching frequency (MHz)	1/N ($N=2^i$ and i=0 to 5)	1	2	2-5
Inductor (μH)	1	10	2.2	1
Capacitor (μF)	10	47	20	10
Maximum load current (mA)	800	550	400	500
Ripple (mV)	80	10	150	<50
FOM	0.283	0.125	0.0436	1.164

transient current is 150–300 mA, and ~27 and 21 μs when the load transient is 200–400 mA, respectively. Fig. 21 shows the line transient response when the input voltage changes from 3.2 to 4.5 V with the loading of 200 mA. The overshoot voltage and drop voltage at the output are 51 and 34 mV, respectively. Fig. 22 shows the transient waveforms from DCM to CCM and from CCM to DCM. The light load is 25 mA and the heavy load is 200 mA. The smooth transient corresponds to the proposed operation shown in Fig. 4(c). In Fig. 22(a), the boost converter is operating in DCM at light load. Once the load current increases, the inductor current starts to increase to depart from the DCM mode. By the CSC technique, the switching frequency increase smoothly. This can be verified by observing inductor current ripple. The gradual decrease of the inductor current ripple shows the increase of switching frequency. On the contrary, Fig. 22(b) shows smooth transition from CCM to DCM operation.

The relationship among load current, switching frequency, and output ripple is shown in Fig. 23(a). The conventional PWM controlled boost converter has constant switching frequency of 5 MHz at both light and heavy loads. With the proposed CSC technique, the switching frequencies at different loads are almost the same in the CCM operation. On the other hand, the switching frequency decreases with the decrease in load current in the DCM operation. The input and output voltages are 3 and 5 V, respectively. Fig. 23(b) shows the efficiency comparison between conventional boost converter with the PWM control, as shown in Fig. 23(a) and the proposed structure. When the CSC technique is disabled, the proposed boost converter acts as a conventional PWM controlled converter. The switching frequency of 5 MHz is generated by fixed-frequency CLK generator in Fig. 18. The power efficiency is deteriorated owing to the switching loss at light loads with a constant switching frequency. When activating the CSC technique, the fixed-frequency CLK generator

is disabled. The switching frequency of the proposed boost converter can be effectively reduced at light load. As a result, the efficiency can be maintained at 78% at load current of 10 mA, demonstrating that the efficiency can be kept high with the implementation of the CSC technique. Table IV shows the performance comparison with prior arts. To compare with prior arts, FOM is defined in (28)

$$\text{FOM} \equiv \frac{\eta_{\min} \cdot I_{\text{load}}}{\text{ripple} \cdot \text{droop} \cdot \text{L} \cdot \text{C}}. \tag{28}$$

With higher light-load efficiency, $\eta_{\min}$, and larger load range, I_{load}, larger FOM can be obtained. On the contrary, output ripple, load transient droop, inductor, and capacitor values should be kept small. As shown in Table IV, the proposed CSC technique has the largest FOM and the best performance compared with prior arts.

VI. Conclusion

The proposed CSC technique for boost converters overcomes the difficulty of implementing a current-ripple hysteresis control and improves efficiency over a wide load range. The CSC technique offers high accuracy similar to that of the current-mode control without the need for complex slope compensation. The load-dependent switching frequency at light loads results in high power conversion efficiency. The experimental results show that the output voltage ripple can be kept <50 mV over a wide load current range from 10 to 400 mA, where as power conversion efficiency is maintained at 78% at a load current of 10 mA.

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Yi-Ping Su was born in Taipei, Taiwan. She received the B.S. degree from the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan, in 2009. She is currently pursuing the Ph.D. degree with the Institute of Electrical Engineering, National Chiao-Tung, Hsinchu, Taiwan.

She is a member of the Mixed Signal and Power Management IC Laboratory, Institute of Electrical Engineering, National Chiao-Tung University. Her current research interests include power management and analog integrated circuits design.

Yean-Kuo Luo was born in Tainan, Taiwan. He received the B.S., M.S., and Ph.D. degrees from the Institute of Microelectronics, National Cheng-Kung University, Tainan, Taiwan, in 2001, 2003, and 2012, respectively.

He is a Faculty Member with the Mixed Signal and Power Management IC Laboratory, Institute of Electrical Control Engineering, National Chiao-Tung University, Hsinchu, Taiwan.

Yi-Chun Chen was born in Taoyuan, Taiwan. He received the B.S. degree in electrical and control engineering and the M.S. degree from the Department of Electrical Engineering and Institute of Electrical Control Engineering, National Chiao-Tung University, Hsinchu, Taiwan, in 2008 and 2010, respectively.

He is currently with Richtek Technology Corporation, Chupei City, Taiwan. He is a Member of the Mixed Signal and Power Management IC Laboratory, National Chiao-Tung University. His current research interests include power-management-integrated circuit design and analog-integrated circuits.

Ke-Horng Chen (M'04–SM'09) received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1994, 1996, and 2003, respectively.

He was a part-time IC Designer with Philips, Taipei, from 1996 to 1998. From 1998 to 2000, he was an Application Engineer with Avanti, Ltd., Taipei. From 2000 to 2003, he was a Project Manager with ACARD, Ltd., where he was engaged in designing power management ICs. He is currently the Director of the Institute of Electrical Control Engineering and a Professor with the Department of Electrical Engineering, National Chiao-Tung University, Hsinchu, Taiwan, where he organized a Mixed-Signal and Power Management IC Laboratory. He is the author or co-author of more than 100 papers published in journals and conferences and holds several patents. His current research interests include power management ICs, mixed-signal circuit designs, display algorithm and driver designs of liquid crystal display TV, and red, green, and blue (RGB) color sequential backlight designs.

Dr. Chen has served as an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS. He has been a member of the Editorial Board of Analog Integrated Circuits and Signal Processing since 2013. He is on the IEEE Circuits and Systems (CAS) VLSI Systems and Applications Technical Committee, and the IEEE CAS Power and Energy Circuits and Systems Technical Committee. He joins Society for Information Display and International Display Manufacturing Conference Technical Program Sub-Committees. He was the Tutorial Co-Chair of IEEE Asia Pacific Conference on Circuits and Systems in 2012. He is the Tack Chair of Integrated Power Electronics of IEEE International Conference on Power Electronics and Drive Systems for 2013. He is a Technical Program Co-Chair of IEEE International Future Energy Electronics Conference for 2013.