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Interfacial microstructure and electrical properties of $PT/Al_2O_3/Si$ annealed at high temperatures

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Abstract

$Pb_{1+x}TiO_3$ (PT) thin films were deposited on Al_2O_3(10 nm)/Si using lead acetate trihydrate and titanium isopropoxide with the addition of glycerol (GL) chelating agent as precursors. It was found that perovskite PT phase can be well crystallized at a lower temperature of 600 °C and excellent memory properties are obtained. However, with increasing annealing temperature above 700 °C, charge-injection mode instead of ferroelectric behavior was detected. Cross-sectional TEM results illustrate that with an increase of annealing temperature and Pb content in the PT films, diffusion envelops and even composition separations were detected in the interface of $PT/Al_2O_3/Si$. It was believed that the degradation in the ferroelectric memory properties is strongly related to the change of microstructure and composition in the interface of $PT/Al_2O_3/Si$.

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1. Introduction

Ferroelectric random access memories (FRAMs) have attracted much attention recently because of lower writing voltage and faster switching speed than those of flash memory [1]. To further improve the cell size and device performance, one-transistor (1T) ferroelectric metal–oxide–semiconductor field-effect transistor (FeMOSFET) type memory is desirable [2]. Unfortunately, the progress of 1T FeMOSFET memory is obstructed by the interface reaction between ferroelectric materials and Si that greatly degrades the device characteristics [3]. It is essential to develop low-temperature process to avoid the inter-diffusion between Si and ferroelectric films for one-transistor (1T) ferroelectric MOSFET memory structure. Therefore, in this research, our investigation will be focused on the effect of annealing temperature on the physical properties and the memory properties of $PT/Al_2O_3/Si$ capacitor. The interfacial microstructure in the interface of $PT/Al_2O_3/Si$ will be examined to investigate the annealing temperature on structure stability and phase change of $PT/Al_2O_3/Si$ FeMOS capacitor to elucidate the property degradation at high temperature.

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2. Experimental procedure

2.1. PT stock solution synthesis and thin film deposition

A ~10 nm thick Al_2O_3 gate dielectric was deposited on p-type (1 0 0) Si wafers [4]. Lead acetate trihydratem, titanium isopropoxide and glycerol (GL) chelating agent were used as PT precursors to deposit PT thin films on Al_2O_3/Si by spinning coating [5]. After multiple coatings, the wet multi-layer films were further annealed at 450–800 °C under oxygen ambient.

2.2. Film and capacitor characterization

The crystal phase of the PT films was determined by x-ray diffraction (XRD) method. The surface morphology and the thickness of PT were observed by transmission electron microscopy (TEM). For electrical measurement, Au was used as upper electrode with area of 5×10^{-4} cm^2 and Al bottom electrode was deposited at the back side of Si substrates. Capacitance–voltage (*C–V*) and current density–voltage (*J–V*) characteristics of PT capacitors were measured.

3. Results and discussion

3.1. Phase evolution and interfacial microstructure

The XRD patterns of Fig. 1 show that the perovskite phase can be developed below 500 °C and well crystallized above 550 °C for GL-added $Pb_{1.1}TiO_3$ (PT) film on Al_2O_3/Si. In contrast, without the addition of glycerol chelating agent, no apparent crystalline phase was detected from PT/Al_2O_3/Si annealed at 500 °C, but, above 600 °C, the perovskite phase starts to appear. The cross-sectional TEM images in Fig. 2(a) illustrate that a sharp interface was observed for GL-added $Pb_{1.1}TiO_3$/Al_2O_3/Si annealed at 700 °C and no trace of Si was detected in the PT film. As increasing the Pb content in the GL-added PT films, a diffusion envelop marked with arrow can be clearly discerned from Fig. 2(b) for the GL-added $Pb_{1.3}TiO_3$ films annealed at 700 °C and the GL-added PT film has been separated into two-layers. As increasing

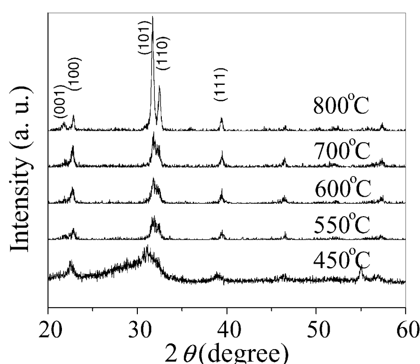

Fig. 1. XRD patterns of $Pb_{1.1}TiO_3$/Al_2O_3/Si annealed at 450–800 °C.

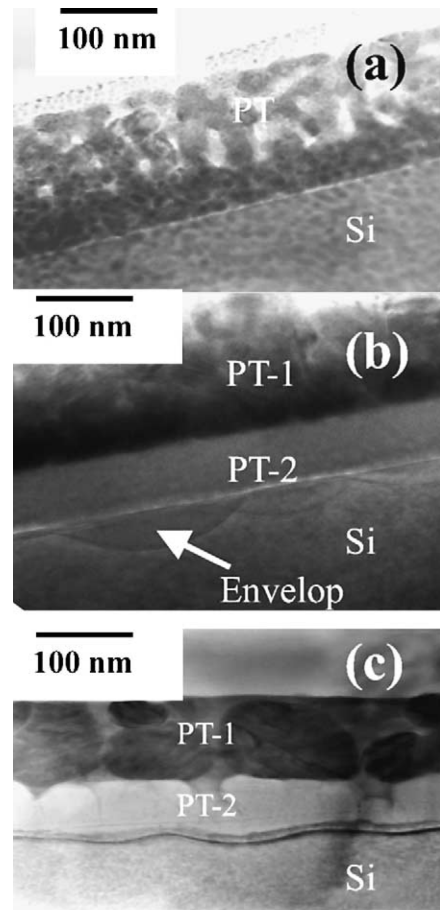

Fig. 2. Cross-sectional TEM images of (a) $Pb_{1.1}TiO_3$/Al_2O_3/Si annealed at 700 °C, and $Pb_{1.3}TiO_3$/Al_2O_3/Si annealed at (b) 700 and (c) 800 °C.

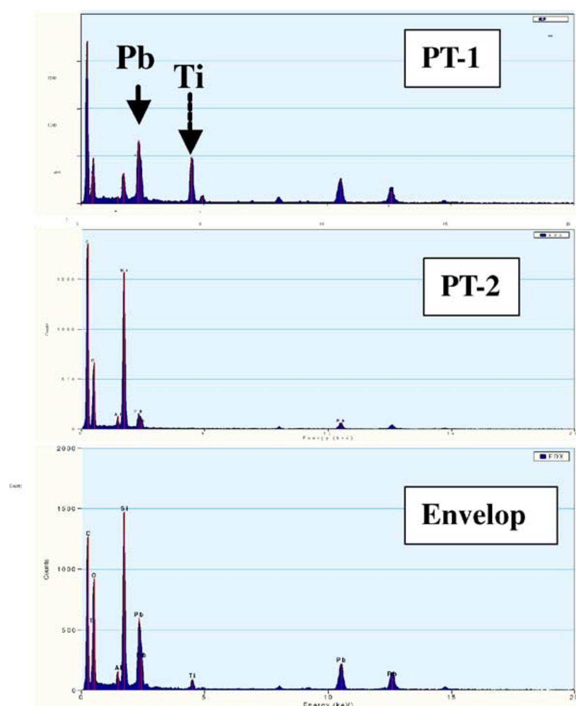

Fig. 3. Composition analysis of PT-1, PT-2 and diffusion envelop in Fig. 2(b).

annealing temperature up to 800 °C, a strong interaction and inter-diffusion has occurred in the interface and the diffusion envelop is further transformed into diffusion layer as shown in Fig. 2(c) where the Al_2O_3 insulator layer has been damaged. When the composition in each layer of Fig. 2(b) was further analyzed using EDS, as shown in Fig. 3, it was found that not only Ti but also Pb has been diffused into Si through Al_2O_3 insulator. The top PT-1 layer was composed of Pb, Ti, O and Si, indicating that the Si has been diffused into the PT film through Al_2O_3 barrier. In contrast, although Pb, Si, O and few Al can be detected from the PT-2 layer, the Ti peak almost disappears compared to that from PT-1 layer. In addition, it was observed that the diffusion envelop near to Al_2O_3 contains more Pb and some Ti. Therefore, the formation mechanism of the diffusion envelop in the GL-added PT/Al_2O_3/Si structure can be tentatively elucidated as follows. During annealing process, both elements of Pb and Ti tend to diffuse into Si and this results in the formation of (Pb, Ti)-deficient PT near to Al_2O_3. With increasing annealing temperature or Pb content, the driving force for Pb diffusion is increased. Therefore, the diffusion envelop will be enlarged and becomes flatten.

3.2. Memory properties

Fig. 4 shows the *C–V* characteristics of GL-added $Pb_{1.1}TiO_3$/Al_2O_3/Si stacked dielectrics. It was found that as the GL-added $Pb_{1.1}TiO_3$/Al_2O_3/Si stacked structure was annealed at 600–700 °C, well-behaved *C–V* curves without distortion were obtained. A memory window of 1.9 V is measured for GL-added $Pb_{1.1}TiO_3$/Al_2O_3/Si at ±5 V bias voltage. For the sample annealed at 700 °C, it is noticed that the memory window value of GL-added PT/Al_2O_3/Si capacitors would change from positive to negative as increasing bias voltage above 5 V, which may be due to the increased leakage current and charge trapping at high voltages. A clockwise hysteresis loop corresponds to ferroelectric mode [6] while the counter-clockwise hysteresis loop is caused by the charge-injection phenomenon. In sharp contrast, as the GL-added PT/Al_2O_3/Si was annealed above 800 °C, although the GL-added PT film shows good crystallite, no discerned *C–V* memory window can be detected.

Although the *C–V* curves can be obtained for the Pb-excess GL-added $Pb_{1.3}TiO_3$ films on Al_2O_3/Si

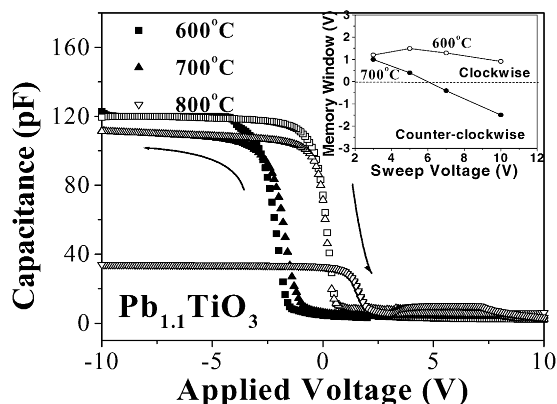

Fig. 4. *C–V* characteristics of $PbTi_{1.1}O_3$/Al_2O_3/Si capacitors annealed at 600–800 °C.

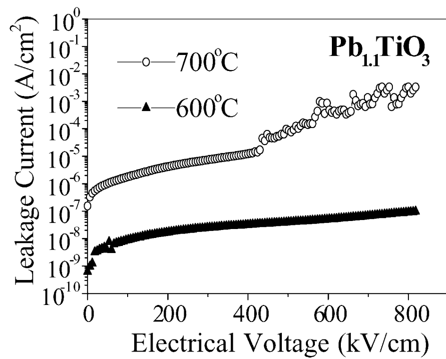

Fig. 5. *J–V* characteristics of $PbTi_{1.1}O_3/Al_2O_3/Si$ capacitors annealed at 600 and 700 °C.

annealed at 600 °C, a smaller memory window was obtained compared to that of GL-added $Pb_{1.1}TiO_3/Al_2O_3/Si$ because a charge-injection mode was generated, indicating a great number of defects or trap sites have been created. Furthermore, as the films were annealed at temperature above 650 °C, no apparent *C–V* memory window can be detected.

Fig. 5 illustrates that the leakage current density of GL-added $Pb_{1.1}TiO_3/Al_2O_3/Si$ annealed at 600 °C is 1.3×10^{-7} A/cm^2 at 100 kV/cm, much lower than that of the film annealed at 700 °C. This smaller leakage current and larger breakdown voltage may be related to the microstructure of GL-added PT films. Furthermore, with an increase of annealing temperature and Pb content in the GL-added PT films, the leakage current density was rapidly increased that is strongly correlated with the formation of the diffusion envelop in the interface of Al_2O_3/Si. However, the leakage current is still low enough for advanced deep sub-μm application.

4. Conclusions

The perovskite PT phase can be well crystallized at a lower temperature of 600 °C and excellent memory properties are obtained for GL-added $PT/Al_2O_3/Si$. However, with increasing annealing temperature above 700 °C, charge-injection mode instead of ferroelectric behavior was detected. Cross-sectional TEM results illustrate that diffusion envelops and even composition separations will be generated in the interface of GL-added $PT/Al_2O_3/Si$ at a higher annealing temperature and Pb-rich composition. It was believed that the degradation in the ferroelectric memory properties is strongly related to the change of microstructure and composition in GL-added $PT/Al_2O_3/Si$.

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