Alternative surface passivation on germanium for metal-oxide-semiconductor applications with high- k gate dielectric

Nan Wu, Qingchun Zhang, Chunxiang Zhu, D. S. H. Chan, M. F. Li, N. Balasubramanian, Albert Chin, and Dim-Lee Kwong

Citation: Applied Physics Letters **85**, 4127 (2004); doi: 10.1063/1.1812835
View online: http://dx.doi.org/10.1063/1.1812835
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/85/18?ver=pdfcov
Published by the AIP Publishing

Alternative surface passivation on germanium for metal-oxide-semiconductor applications with high-*k* gate dielectric

Nan Wu, Qingchun Zhang, Chunxiang Zhu,[a] D. S. H. Chan, and M. F. Li
Silicon Nano Device Lab, Department of Electrical and Computer Engineering, National University of Singapore, 10 Kent Ridge Crescent, Singapore, 119260

N. Balasubramanian
Institute of Microelectronics, 11 Science Park Road, Singapore Science Park II, Singapore, 117685

Albert Chin
Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, Republic of China

Dim-Lee Kwong
Department of Electrical and Computer Engineering, The University of Texas, Austin, Texas 78752

(Received 8 March 2004; accepted 1 September 2004)

An alternative surface passivation process for high-*k* Ge metal-oxide-semiconductor (MOS) device has been studied. The surface SiH_4 annealing was implemented prior to HfO_2 deposition. X-ray photoelectron spectroscopy analysis results show that the SiH_4 surface passivation can greatly prevent the formation of unstable germanium oxide at the surface and suppress the Ge out-diffusion after the HfO_2 deposition. The electrical measurement shows that an equivalent oxide thickness of 13.5 Å and a leakage current of 1.16×10^{-5} A/cm^2 at 1 V gate bias was achieved for $TaN/HfO_2/Ge$ MOS capacitors with the SiH_4 surface treatment. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1812835]

As the scaling of the modern complementary metal-oxide-semiconductor field effect transistor (MOSFET) continues, Si is approaching its fundamental limits. Various approaches are being investigated to overcome the limits. High permittivity (high-*k*) materials are being studied to replace the conventional silicon dioxide for gate oxide scaling.[1] At the same time, carrier mobility enhancement is another issue for performance improvement of the device. Germanium as channel is attractive because of its significant enhancement in bulk carrier mobility relative to silicon. In order to have the both merits of high-*k* and germanium, several successful demonstrations of MOS devices by using them together have been reported recently.[2–7] However, there is an intrinsic problem in the formation of the gate stack on Ge substrate: germanium oxide is thermally unstable, water solutable,[8] and of poor electrical properties. Thus, minimizing the unstable GeO_x at the surface during high-*k* deposition is a critical issue to form high quality gate stack on Ge substrate. Surface nitridation using NH_3 annealing prior to high-*k* deposition is a key step in recent demonstrations,[4–7] where nitrogen is introduced into the interface of germanium oxide to passivate the germanium. However, the nitrogen involvement has the potential for mobility degradation. In this letter, we demonstrate an alternative surface passivation for high-*k* gate stack formation on Ge using *in situ* SiH_4 annealing prior to HfO_2 deposition.

The starting wafers for the experiment were Sb-doped *n*-type wafers with a resistivity of 0.04–0.08 Ω cm. The native oxide (GeO_x) was removed by dipping the sample in a diluted HF solution (1:50) for 5 min, followed by rinsing in de-ionized water.[4] After that, the wafers were transferred to a constant-temperature (400 °C) process chamber with base pressure of 3 mTorr and annealed in SiH_4+N_2 ambient at 5 Torr for 60 s. Subsequently, the wafers were transferred to another chamber for the metal-organic chemical vapor deposition (MOCVD) of HfO_2. The deposition of HfO_2 was performed at 400 °C using Hf tert-butoxide as the metal organic precursor in an N_2+O_2 ambient (400 mTorr). Load lock was used for wafer loading, unloading, and transferring between the process chambers. Because the load lock is under a base pressure of $\sim5\times10^{-7}$ Torr, the SiH_4 surface passivation on the Ge substrate can be considered an *in situ* process prior to the HfO_2 MOCVD. Post-deposition anneal is performed in a rapid thermal processor at 500 °C. A 1500 Å TaN film is then sputtered and patterned as gate electrode. The final step was annealing in forming gas (H_2+N_2) ambient at 300 °C. High-resolution *ex situ* x-ray photoelectron spectroscopy (XPS) analysis was performed using a Physical Electronics quantum 2000 scanning ESCA microprobe with a monochromatic and standard Al x-ray source. Atomic force microscopy (AFM) was used to examine surface morphology. The electrical properties of MOS capacitors were characterized with an Agilent 4284A *LCR* meter and a Hewlett-Packard 4156A semiconductor parameter analyzer.

An effective SiH_4 surface passivation on germanium should meet the following criteria: (1) Si must completely cover the germanium surface and the germanium surface should be free of germanium oxide; (2) The silicon passivation layer should be thin enough and consumed during the subsequent high-*k* deposition so that the MOSFET channel is still kept in germanium.

Figure 1 shows the Ge 2*p*3 XPS spectra of the sample just after DHF cleaning and the sample after the SiH_4 surface passivation. The inset is the Si 2*p* XPS spectrum of the sample after the SiH_4 surface passivation. As can be seen, the

[a]Author to whom correspondence should be addressed; electronic mail: elezhucx@nus.edu.sg

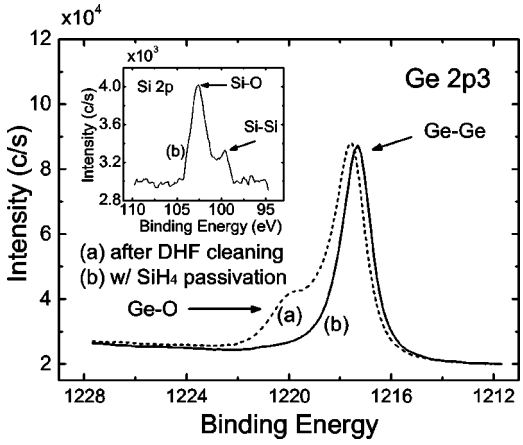

FIG. 1. The Ge 2*p*3 spectra of *ex-situ* XPS on the passivation process on Ge surface by SiH_4. The samples before and after passivation were compared. Inset: The Si 2*p* spectra of the samples after SiH_4 passivation.

Ge–O peak[9] observed on the DHF as-cleaned Ge surface disappeared after the SiH_4 passivation. Moreover, the Si-passivated Ge surface is stable even if the sample is exposed to the air. The existence of silicon is confirmed by the Si 2*p* spectrum of the same sample, as shown in the inset. This Si signal includes two types of bonds:[9] one is the elemental Si, and the other is SiO_x (which is likely introduced during sample transportation). Based on the above analysis, the germanium surface is completely covered by elemental Si and free of germanium oxide after the SiH_4 passivation. It is well known that Ge oxide is very unstable at moderately high temperatures ($\geqslant$400 °C) in vacuum. Therefore, it is possible that the germanium oxide is removed when the sample is loaded into the chamber and before gases are supplied to raise the chamber pressure. Further, the extreme deficiency of oxygen in the SiH_4 chemical vapor deposition chamber may also enhance the tendency for reduction reaction of the Ge among the surface germanium oxide.

It is also noticed in Fig. 1 that: (1) the intensity of the Si–O peak (~102.6 eV) is much lower (~65 times) than that of the Ge–Ge peak (~1217.4 eV) for the sample after passivation; (2) the Ge–Ge peak (~1217.4 eV) of the sample after passivation shows a negligible intensity reduction compared to the as-cleaned sample. Both imply that the amount of the top silicon is so little that the thickness is much less than the inelastic mean free path (IMFP) of Ge 2*p*3 electrons traveling in silicon. The small value of the IMFP (~8.7 Å)[10] indicates the silicon layer could be only a few monolayers. Such a result can be explained as the deposition of Si onto cleaned Ge surface is accelerated compared to the deposition of Si on Si surface because of the difference in surface energy.[11] Hence, after the Ge surface is fully covered by Si, the Si deposition will be much reduced or stopped especially at the temperature of ~400 °C.

In order to examine the surface roughness, AFM analysis was performed on the fresh sample, the as-cleaned sample, and the Si-passivated sample. Figure 2 shows the AFM results with a scanning area of 1 μm × 1 μm. As can be seen, the surface roughness is greatly reduced after the DHF cleaning (rms=0.157 nm) [Fig. 2(b)] compared to the fresh sample (rms=0.340 nm) [Fig. 2(a)]. Besides, comparable surface roughness between the DHF-cleaned sample [Fig. 2(b)] and the Si-passivated sample (rms=0.166 nm) [Fig. 2(c)] were observed.

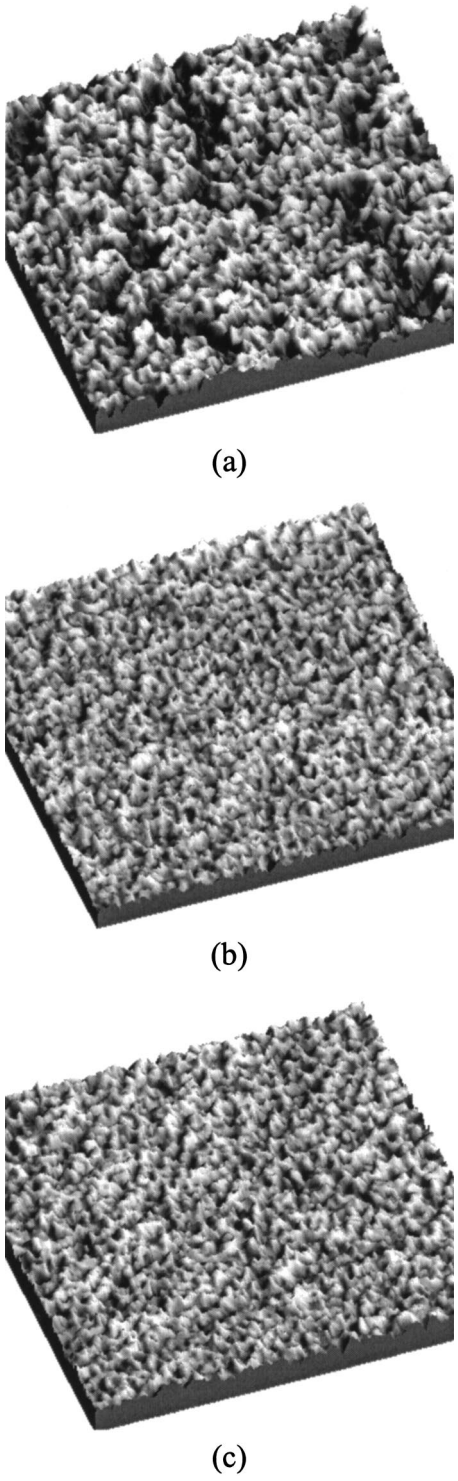

FIG. 2. AFM analysis of surface roughness on fresh sample (a), as-cleaned sample (b), and Si-passivated sample (c).

Early study shows that germanium out-diffuses into MOCVD HfO_2 during the deposition when there is no surface treatment.[7] Thus, the effect of the SiH_4 surface passivation on the subsequent HfO_2 deposition is studied by angle-resolved XPS analysis and shown in Fig. 3. The sample after HfO_2 deposition without Si passivation is included for comparison. Both samples are characterized at takeoff angles of 10° and 90°, respectively. In order to have fair comparison, since there is no difference in the binding energy between all

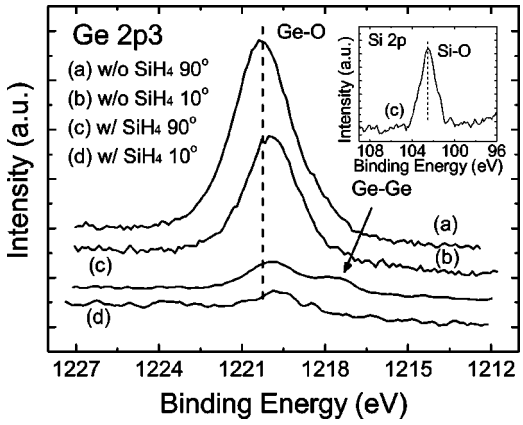

FIG. 3. The Ge 2*p*3 spectra of angle-resolved *ex-situ* XPS on the sample with and without passivation after HfO_2 MOCVD.

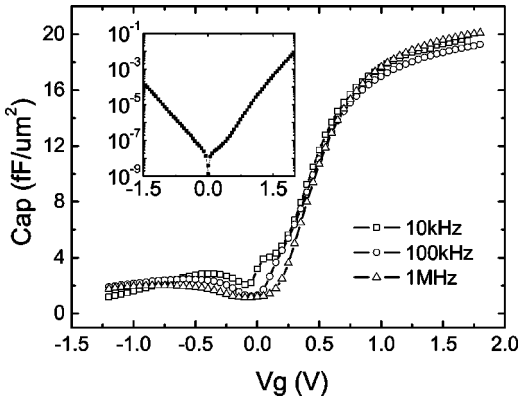

FIG. 4. Electrical characteristics of the $TaN/HfO_2/Ge$ MOS capacitor with SiH_4 surface passivation.

the Hf 4f spectra (not shown), the Hf 4f spectra are normalized to the same level, and then, all the correspondent Ge 2*p*3 signals are scaled, respectively, with the same factors as the Hf 4f (shown in Fig. 3). As can be seen, only the sample with Si passivation at the 90° takeoff angle shows a two-peak spectrum [curve (c)], representing the elemental germanium and the germanium at oxide states.[9] The detection of element Ge bonds indicates that the HfO_2 film on this sample is thinner than the sample without Si passivation [curve (a)]. Moreover, the Ge–O peak area of the Si passivated sample [curve (c)] is much smaller than that of the sample without passivation [curve (a)]. This means the passivation is very effective in suppressing formation of germanium oxide. The small takeoff angle (10°) in the analysis was then used to examine the dielectric film. Obviously, the amount of Ge in the sample with Si passivation at 10° takeoff angle is much less than that of the sample without Si passivation. Thus, the significant Ge out-diffusion during HfO_2 MOCVD is greatly suppressed by Si passivation. On the other hand, only Si at its oxide state is detected (the inset of Fig. 3), indicating that there is no Hf-silicide formation at the interface.

The characteristics of the $TaN/HfO_2/Ge$ MOS capacitor (area $=100\ \mu m \times 100\ \mu m$) with surface passivation are shown in Fig. 4. The capacitance was measured by sweeping the gate bias from inversion to accumulation. There is no substantial frequency dispersion across the entire measurement region.[12] However, a small kink can be observed when the measurement frequency is reduced to 10 kHz, indicating there are still some "slow" interface states near the valence band (E_V).[13] An equivalent oxide thickness (EOT) of $\sim$13.5 Å is obtained with taking account of quantum-mechanical effects. The leakage current as a function of gate bias is shown in the inset figure. A leakage current of $1.16 \times 10^{-5}\ A/cm^2$ is achieved at 1 V gate bias. The good performance of I_g-EOT shows the potential of SiH_4 surface passivation for HfO_2 scaling in forming future ultrascaled gate stack on germanium. For comparison, the MOS capacitor is of high leakage current even with relatively large EOT when there is no surface treatment prior to HfO_2 deposition.[7]

In summary, we proposed and demonstrated an alternative surface passivation to fabricate high-*k* Ge MOS devices by using *in situ* SiH_4 annealing. *Ex situ* XPS and AFM were used to study the passivation process. Silicon fully covers the germanium surface and is kept within monolayer range at the same time. Germanium remains un-oxidized after the Si passivation and the formation of germanium oxide was greatly suppressed during the HfO_2 MOCVD. The electrical results reveal the potential of the Ge MOS system with SiH_4 surface passivation for future ultrascaled very large scale integrated devices.

The authors thank the Department of Physics, National University of Singapore, for the AFM analysis. This work was supported by Singapore ASTAR R-263-000-267-305 grant.

[1]Internation Technology Roadmap for Semiconductors, 2003.
[2]C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, Tech. Dig. - Int. Electron Devices Meet. **2002**, 437 (2002).
[3]C. H. Huang, M. Y. Yang, A. Chin, W. J. Chen, C. X. Zhu, B. J. Cho, M. F. Li, and D. L. Kwong, VLSI Tech. Dig. **2003**, 119 (2003).
[4]W. P. Bai, N. Lu, J. Liu, A. Ramirez, D. L. Kwong, D. Wristers, A. Ritenour, L. Lee, and D. Antoniadis, VLSI Tech. Dig. **2003**, 121 (2003).
[5]A. Ritenour, S. Yu, M. L. Lee, N. Lu, W. Bai, A. Pitera, E. A. Fitzgerald, D. L. Kwong, and D. A. Antoniadis, Tech. Dig. - Int. Electron Devices Meet. **2003**, 433 (2003).
[6]C. O. Chui, H. Kim, P. C. McIntyre, and K. C. Saraswat, Tech. Dig. - Int. Electron Devices Meet. **2003**, 437 (2003).
[7]N. Wu, Q. Zhang, C. Zhu, C. C. Yeo, S. J. Whang, D. S. H. Chan, M. F. Li, B. J. Cho, A. Chin, D. L. Kwong, A. Y. Du, C. H. Tung, and N. Balasubramanian, Appl. Phys. Lett. **84**, 3741 (2004).
[8]K. Prabhakaran and T. Ogino, Surf. Sci. **325**, 263 (1995).
[9]NIST x-ray photoelectron spectroscopy database, NIST standard reference database 20, version 3.4 (web version), http://srdata.nist.gov/xps/
[10]P. J. Cumpson and M. P. Seah, Surf. Interface Anal. **25**, 430 (1997); web calculator: http://www.lasurface.com/IMFP/Ag_imfp_cal.htm
[11]D. J. Tweet, T. Tatsumi, H. Hirayama, K. Miyanaga, and K. Terashima, Appl. Phys. Lett. **65**, 2579 (1994).
[12]H. Kim, C. O. Chui, K. C. Saraswat, and P. C. McIntyre, Appl. Phys. Lett. **83**, 2647 (2003).
[13]C. O. Chui, S. Ramanathan, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, IEEE Electron Device Lett. **23**, 473 (2002).