

A 65 nm 0.165 fJ/Bit/Search 256×144 TCAM Macro Design for IPv6 Lookup Tables

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Abstract—Ternary content addressable memory (TCAM) is extensively adopted in network systems. As routing tables become larger, energy consumption and leakage current become increasingly important issues in the design of TCAM in nano-scale technologies. This work presents a novel 65 nm energy-efficient TCAM macro design for IPv6 applications. The proposed TCAM employs the concept of architecture and circuit co-design. To achieve an energy-efficient TCAM architecture, a butterfly match-line scheme and a hierarchy search-line scheme are developed to reduce significantly both the search time and power consumption. The match-lines are also implemented using noise-tolerant XOR-based conditional keepers to reduce not only the search time but also the power consumption. To reduce the increasing leakage power in advanced technologies, the proposed TCAM design utilizes two power gating techniques, namely super cut-off power gating and multi-mode data-retention power gating. An energy-efficient 256×144 TCAM macro is implemented using UMC 65 nm CMOS technology, and the experimental results demonstrate a leakage power reduction of 19.3% and an energy metric of the TCAM macro of 0.165 fJ/bit/search.

Index Terms—Butterfly match-line, hierarchy search-line, memory, power gating, TCAM, XOR conditional keeper.

I. INTRODUCTION

CONTENT-ADDRESSABLE memory (CAM), also called associative memory, executes the lookup-table function in a single clock cycle using dedicated comparison circuitry. CAM compares input search data against a table of stored information, and returns the matching data. Accordingly, CAM cells contain storage memories and comparison circuits. CAM cells are of two types – binary content addressable memory (BCAM) and ternary content addressable memory (TCAM) – depending on their comparison function as presented in Fig. 1. A BCAM cell has two states – the “one” state and the “zero” state. A BCAM cell contains 1-bit storage memory and a 1-bit comparison circuit. TCAM has three states – logic 0, logic 1, and don’t-care X. The third state, don’t-care X, which is used in masking, makes TCAM suitable for network router applications. Hence, the difference between BCAM and TCAM is that TCAM contains an extra SRAM to store the don’t-care state. If the datum in don’t-care cell is 1, then the match-line (ML) will bypass the

don’t-care cells and be discharged to ground. It will not perform any comparison operation. If the datum in don’t-care cell is 0, then the function of TCAM is the same as that of BCAM.

In past decades, CAM has been employed in numerous applications that depend on fast search. These applications are parametric curve extraction [1], Hough transformation [2], Lempel-Ziv compression [3], image coding [4], the human body communication controller [5], the periodic event generator [6], and the virus-detection processor [7]. At present, CAM is popular for use in network routers for packet forwarding, packet classification, asynchronous transfer mode (ATM) switching, and other functions. As the range of CAM applications grows, power consumption becomes one of the critical challenges. The trade-off among power, speed, and area is the most important issue in recent researches on large-capacity CAMs. The primary commercial application of CAMs today is the classification and forwarding of Internet protocol (IP) packets in network routers. Internet Protocol Version 6 (IPv6) is the next generation protocol, designed by the IETF, to replace the current version Internet Protocol, IP Version 4 (“IPv4”). IPv6 addresses are 128-bit or 144-bit identifiers for interfaces and sets of interfaces [8]–[12]. Each address must be stored in 128 or 144 TCAM cells, resulting in a long search delay path in network routers in packet forwarding applications. Accordingly, high speed and low power are the two major goals of TCAM design for IP-address forwarding applications, especially in nano-scale technologies.

As nano-scale technologies become more advanced, leakage currents increasingly dominate their overall power consumption. However, previous investigations of low-power TCAM have focused only on dynamic power consumption [13]–[22]. Our previous work has presented two power gating techniques to reduce leakage currents, called multi-mode data-retention power gating and super cut-off power gating [23]. We have also developed the noise-tolerant XOR-based conditional keeper, the butterfly match-line scheme and the hierarchy search-line scheme, to reduce not only the length of critical paths but also the power consumption [23]–[26]. Nevertheless, these papers presented simulation results obtained using 0.13 μm and 90 nm CMOS technologies, and did not analyze the energy-efficient schemes. In this work, however, a 65 nm TCAM macro is fabricated and measured, and details of power gating techniques and an energy analysis are also given.

II. ARCHITECTURE OF TCAM MACRO IN NETWORK ROUTERS

In recent years, TCAMs have been popularly used in network routers for packet forwarding and packet classification. Network routers forward data packets from an incoming port to

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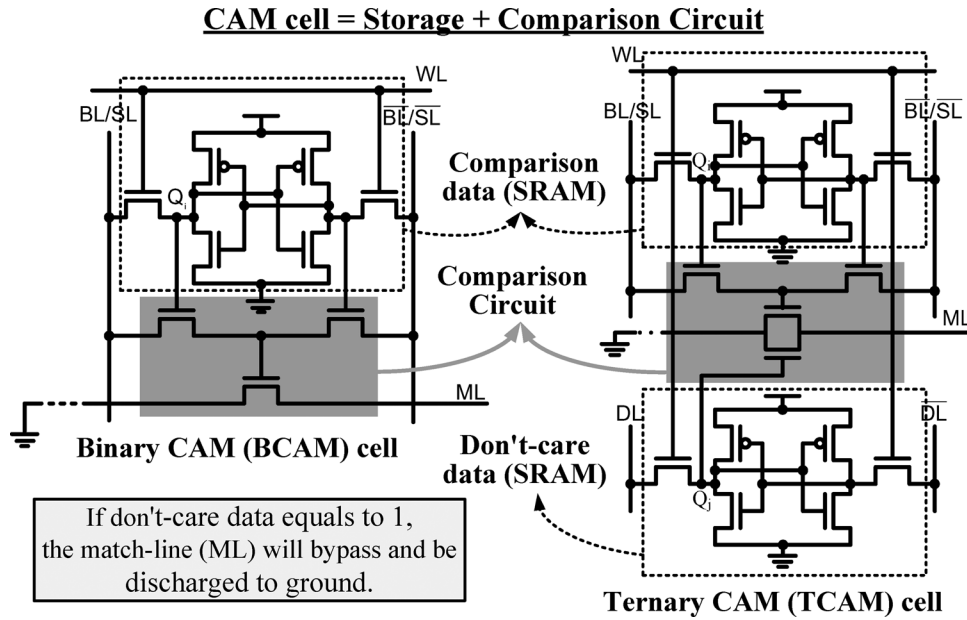


Fig. 1. Binary CAM (BCAM) cell and ternary CAM (TCAM) cell.

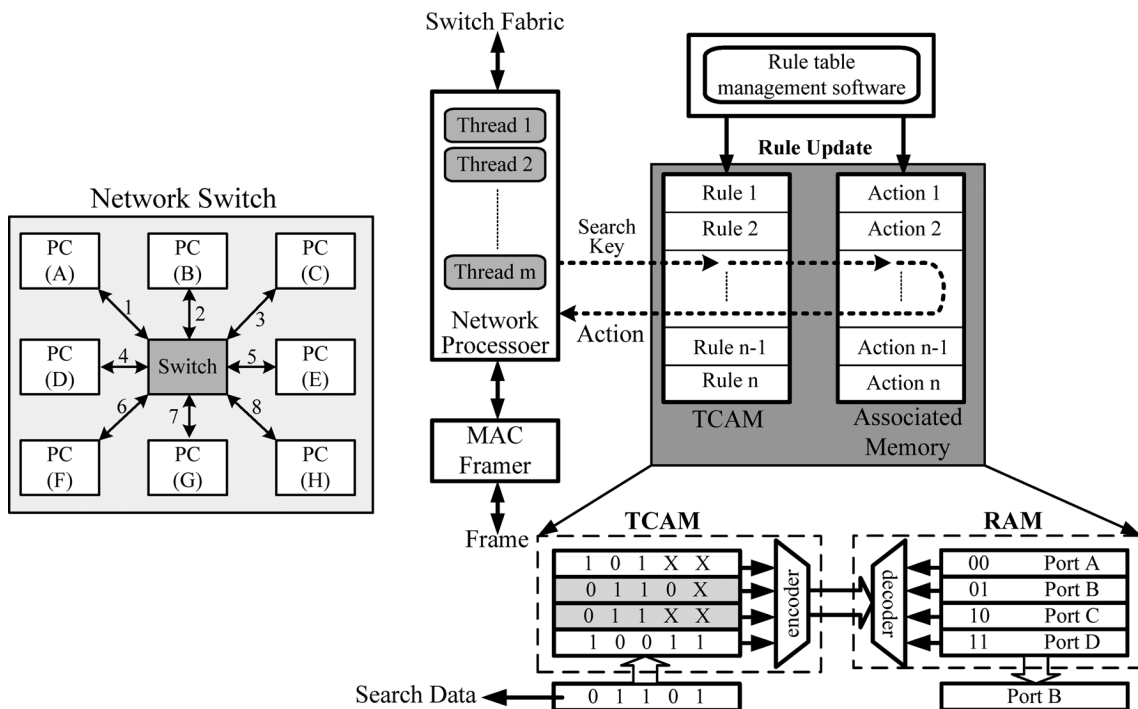


Fig. 2. A simplified block diagram of a TCAM macro and packet forwarding by an address-lookup table in network routers.

an outgoing port, using an address-lookup function [27]. Fig. 2 schematically depicts a simplified block diagram of a TCAM macro. The search data are broadcast onto the search-lines to the table of stored data. The address-lookup function determines the destination address of the packet and selects the output port that is associated with that address. For example, the packet destination address 01101 is input to the TCAM. As indicated by the table, two entries are matched, and the priority encoder chooses the upper entry and generates the matching location 01. This matching location is the address that is input to a RAM that contains a list of output ports, as shown in Fig. 2. A read oper-

ation of RAM outputs the port destination—port B, to which the incoming packet is forwarded. This TCAM/RAM system fully implements an address-lookup engine for packet forwarding.

The number of bits in a TCAM word is generally large, and existing implementations range from 36 to 144 bits. A typical TCAM utilizes a table size that has between a few hundred entries and 32 K entries, corresponding to an address space that ranges from 7 bits to 15 bits. Each stored word has a match-line that indicates whether the search word is identical to the stored word (matching) or not (mismatching, or “a miss”). The match-lines are fed to an encoder that generates a binary matching lo-

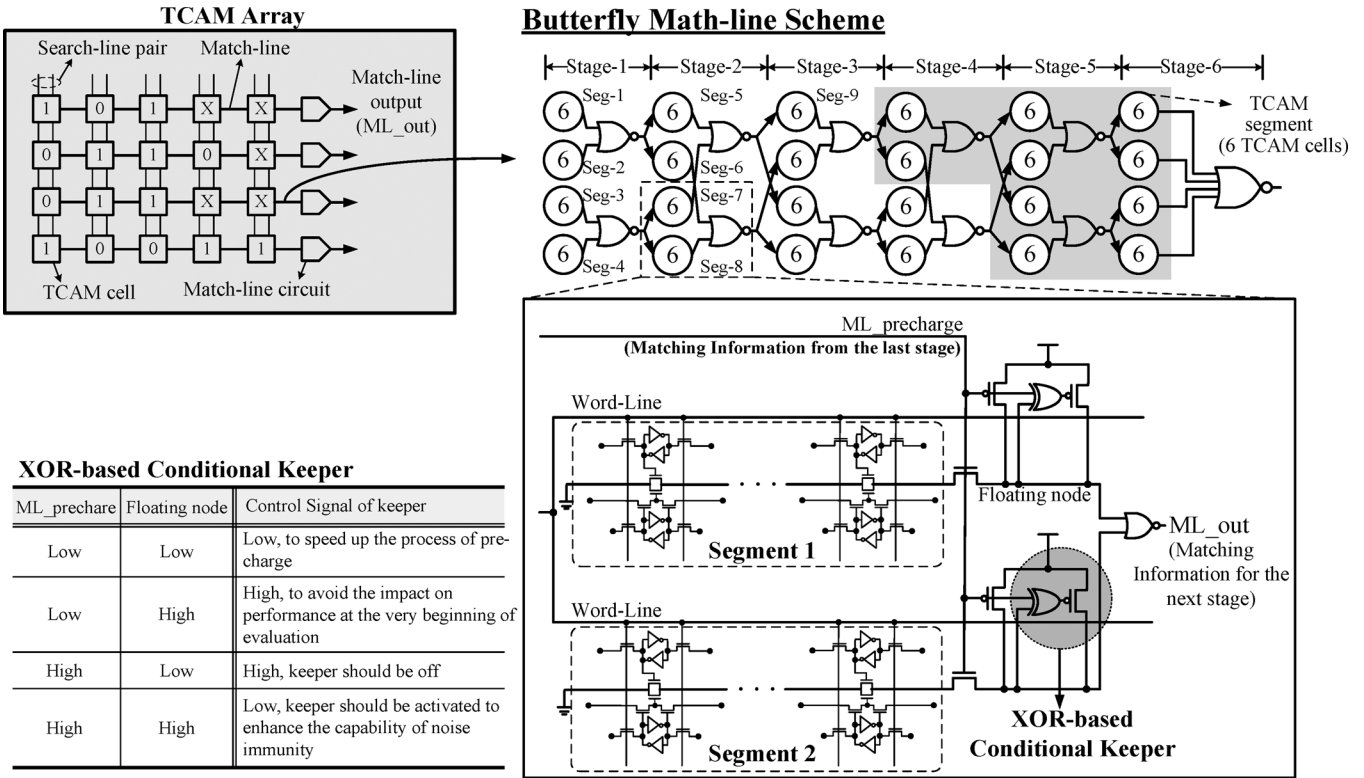


Fig. 3. Butterfly match-line schemes with XOR conditional keeper.

cation that corresponds to the most-direct routing. An encoder is adopted in systems in which only a single match is expected. In TCAM applications, where more than one word may match, a priority encoder is employed instead of a simple encoder. A priority encoder identifies the location that is matched with the highest priority to map the result of matching, such that words in lower address locations have higher priority. The overall function of TCAM is to take a search word and return the matching memory location.

Two match-line methods are applied with the TCAM architecture. When the stored data are not identical to the search data in every bit, the match-line is discharged to ground. This match-line is called the NOR-type match-line [19], [20], [22]. The other is the NAND-type (AND-type) match-line. The NAND-type match-line is discharged to ground only when all bits of stored data match all bits of search data. Generally, the NOR-type match-line has a shorter search time than the NAND-type match-line but consumes much more power in the search operation. The NAND-type consumes less search power but has a longer search time owing to the deep fan-in circuits. Numerous approaches have been presented to improve the search time of the NAND-type match-line. They include the pseudo-footless clock-data pre-charge dynamic (PF-CDPD) match-line scheme [15], the range matching scheme [16] and the tree-style AND-type match-line scheme [17], [21]. The evaluation operation of the conventional PF-CDPD match-line is enabled or disabled depending on the output of the preceding stages. Consequently, PF-CDPD circuits reduce not only search time but also power consumption.

III. ENERGY-EFFICIENT MATCH-LINE

As technology advances, leakage currents, coupling noise, charge sharing and power/ground fluctuation noises all increase the soft-error rate of dynamic circuits in the match-lines of the TCAM macro. The increasing noise not only worsens performance; it even destroys the functionality of the TCAM macro. Therefore, the proposed butterfly match-line scheme with the XOR-based conditional keeper supports a low-power, high-speed and noise-tolerant TCAM. The butterfly match-line scheme improves performance by increasing the parallelism of the search operation. It also reduces the power consumption in a manner that depends on the interlaced pipeline since the butterfly connections turn off more TCAM segments than PF-CDPD match-line scheme does. The XOR-based conditional keeper for the match-lines provides noise-tolerant circuitry to reduce both search time and power consumption. The XOR-based conditional keeper eliminates the performance overhead of the butterfly connections. Fig. 3 shows the butterfly match-line scheme with XOR-based conditional keepers. The butterfly match-line scheme and the XOR-based conditional keeper are described in detail below.

A. Butterfly Match-Line Scheme

Fig. 3 presents the butterfly match-line scheme, which is based on the PF-CDPD match-line scheme [15], for 144 TCAM cells. Each circle represents a TCAM segment, which contains six TCAM cells and a dynamic circuit. The degree of parallelism is double that of the conventional PF-CDPD match-line scheme. In 144-bit TCAM cells, the match-line is

folded into four sub match-lines in six stages. Accordingly, the number of segments of the critical path is reduced from 12 to six. Therefore, the critical delay of a match-line is reduced from $(12T_{\text{seg}} + T_{\text{AND2}})$ to $(6T_{\text{seg}} + 5T_{\text{NOR2}} + T_{\text{NOR4}})$ compared to the conventional PF-CDPD match-line scheme [15]. The T_{seg} represents the discharging time of a TCAM segment and is much larger than the delay of NOR gates. To reduce the power consumption, a butterfly connection is made among these four independent sub match-lines by intersecting the interlaced connections, as shown in Fig. 3. Therefore, the mismatching signal of one sub match-line can be propagated to other sub match-lines using the butterfly connection. When one of the TCAM segments is mismatched with search data, the proposed butterfly match-line scheme turns off more TCAM segments than does the conventional PF-CDPD match-line scheme. All the search operations behind this mismatched segment are terminated. The butterfly match-line scheme increases the dependence between the four parallel match-lines.

The butterfly match-line scheme not only achieves high performance with a high degree of parallelism but also reduces the power consumption by exploiting butterfly connections. Such a match-line can be implemented using full connections between two stages and thereby propagate all the mismatching information to the subsequent stages. However, it requires a NOR gate with four fan-ins to collect the information about the mismatching associated with the previous stage. Thus, this NOR-gate must provide the driving capacity to trigger the four segments in the subsequent stage. Although it can turn off two more segments than can the butterfly match-line scheme, the power and performance overheads of the NOR gates with four fan-ins and four fan-outs will dominate the critical path of the match-line. Accordingly, the butterfly connection can turn off the segments behind the mismatching segment most efficiently.

The power analysis of the butterfly match-line scheme is as follows. Before the power formulas of the butterfly match-line schemes can be derived, some assumptions are made for simplicity.

- The power consumption of the search operation is the same in all segments (P_{seg}) when all of the TCAM cells are matched with the search data in one TCAM segment.
- The matching probability of the TCAM cell [i] is represented as p_i ($i = 1$ to 144). The probability p_i is defined as one when $i < 1$.

Equation (1), at the bottom of the page, is the power formula for the butterfly match-line scheme with 144-bit TCAM cells. P_{seg} denotes the power consumption when the TCAM segment is discharged in the evaluation cycle. However, the power consumption of the charge sharing in the dynamic circuit is neglected when the TCAM segment is mismatched. The probability of segment- n , PS_n , represents the probability that the TCAM segment- n is matched to the search data. Each stage consists of four TCAM segments, and the segments in stage-1 are defined from Seg-1 to Seg-4. The terms, j and k , refer to the odd and even stages of the butterfly match-line scheme, respectively. Therefore, the butterfly match-line scheme can achieve a higher power saving because more TCAM segments are turned off, according to (1). For example, if Seg-9 as shown in Fig. 3 is turned off, all the segments in the gray background will not be activated.

B. XOR-Based Conditional Keeper for Match-Line

The AND-type match-line includes high fan-in circuits. However, conventional keepers perform more poorly in terms of propagation delay and power consumption. Accordingly, the authors previously proposed a novel keeper, called the XOR-based conditional keeper in [28]. The main idea of the proposed XOR-based conditional keeper is to ensure that the keeper does not turn on in the dynamic circuit at the beginning of the evaluation phase. Fig. 3 also presents the new control signals and their corresponding keeper states. When the match-line pre-charge signal and the floating node are both low, the TCAM circuit is at the beginning of the pre-charge period and the conditional keeper should be turned on to accelerate the pre-charge procedure. When the match-line pre-charge signal is low and the floating node is high, the pre-charge process is complete and the gate is ready to be evaluated. Therefore, the conditional keeper should be turned off to prevent any impact on the delay and any unnecessary power consumption. When the match-line pre-charge signal and floating node are both high, the match-line is either at the beginning of the evaluation process or stores state HIGH in the floating node at the end of the evaluation process. If it is at the beginning of the evaluation process, the floating node will eventually be at the appropriate voltage as long as the delay of the XOR gate exceeds the propagation delay of the dynamic circuits. Since the delay time of the dynamic circuits is shorter than that of the XOR gate, the conditional keeper is slightly turned on at the beginning of the evaluation process and is fully

$$P_{144\text{-bit}} = P_{\text{seg}} \left\{ \sum_{j=0}^2 \left[\prod_{i=0}^{4+8(j-1)} PS_i \times [PS_{8j-3}PS_{8j-1} (PS_{8j+1} + PS_{8j+2}) + PS_{8j-2}PS_{8j} (PS_{8j+3} + PS_{8j+4})] \right] \right. \\ \left. + \sum_{k=0}^2 \left[\prod_{i=0}^{8k} PS_i \times [PS_{8k+1}PS_{8k+2} (PS_{8k+5} + PS_{8k+6}) + PS_{8k+3}PS_{8k+4} (PS_{8k+7} + PS_{8k+8})] \right] \right\} \\ \text{where } PS_n = \begin{cases} \prod_{i=6n-5}^{6n} p_i, & n \geq 1 \\ 1, & n \leq 0 \end{cases} \quad (\text{probability product of segment } n). \quad (1)$$

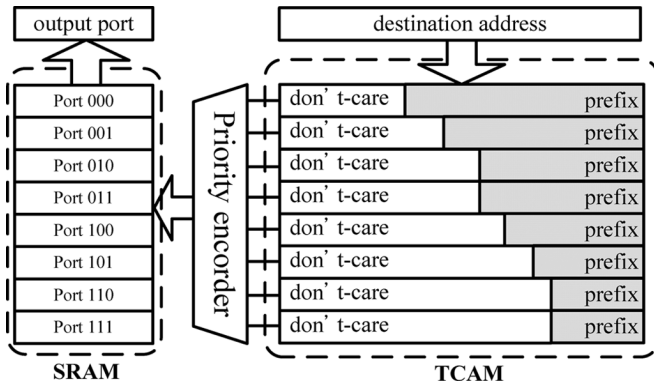


Fig. 4. Packet routing table based on longest prefix matching mechanism.

turned on or off as determined by the final value that is stored in the floating node. When the match-line pre-charge signal is high and the floating node is low, the evaluation mode has been completed and the final value stored in the floating node is low. Consequently, the conditional keeper should be fully turned off. An XOR gate is required to generate the desired control signals.

The noise-tolerant energy-efficient match-line employs the co-design of the architecture and the circuit. Based on the butterfly connection, the inverters behind the XOR-based conditional keepers and the AND gate can together be represented an NOR gate, as presented in Fig. 3. Therefore, to reduce the search time overhead caused by the butterfly connection, the XOR-based conditional keeper approach can be used to reduce the delay associated with the critical path of the match-line. Clearly, the increase in the propagation delay of a TCAM segment by the XOR-based conditional keeper is small. Furthermore, the gate delay of a NOR gate is shorter than that of an AND gate. Accordingly, the proposed butterfly match-line scheme with a XOR-based conditional keeper exhibits high performance, because of the high degree of parallelism. It also saves power by using an XOR-based conditional keeper and turning off the mismatched segments. This match-line also simultaneously reduces the search time and power consumption. Moreover, it is resilient against noise effectively.

IV. DON'T-CARE BASED HIERARCHY SEARCH-LINE SCHEME

In a manner determined by an address-lookup function, network routers forward data packets from an incoming port to an outgoing port. Additionally, a TCAM cell stores an “X” value as a mask. The “X” value represents a don’t-care state, referring both “0” and “1”, and allows a wildcard operation. The wildcard operation is a feature of packet forwarding in Internet routers and involves the storing of an “X” value in a cell to yield a match, regardless of the input bit. Furthermore, the list of routing tables can be rearranged and maintained using rule table management with continuous don’t-care X patterns, as presented in Fig. 4. Based on the continuous don’t-care X pattern and pre-fix pattern, a hierarchy search-line scheme, a super cut-off power gating technique and a multi-mode data-retention power gating technique, are proposed. This section presents the don’t-care-based hierarchy search-line scheme. The following sections will elucidate the other procedures.

The don’t-care-based hierarchical search-line scheme is utilized to decrease the switching capacitances and switching activities without adding any search time overhead. If the TCAM cell is don’t-care, then the matching signal is independent of the searching data and the search-lines can be disabled to reduce consumed power. Therefore, the hierarchy search-line scheme divides the search-lines into a two-level hierarchy of global search-lines (GSLs) and local search-lines (LSLs). The GSLs are active in every cycle, but whether the LSLs are active depends on don’t-care cells. Fig. 5(a) displays a simplified architecture of the don’t-care-based hierarchical search-line scheme. The entire TCAM is divided into n sub-blocks, each of which is composed of numerous match-lines and one global search-line to local search-line buffer (GSL-to-LSL buffer). In the IPv6 addressing lookup tables associated with TCAM, the prefixes are arranged in order by prefix lengths. The longest prefix is located at the top of the TCAM. Accordingly, the upper TCAM cells must be don’t-care terms. The GSL-to-LSL buffers are controlled by the data in the don’t-care cells which is stored in the bottom word of each block. Moreover, Fig. 5(b) presents the circuit implementation of the don’t-care-based hierarchical search-line. During a search operation, the search data are propagated to GSL first. And then, the search data would be propagated to the LSLs according to the don’t-care data. Therefore, the GSL-to-LSL buffer is used to determine whether search data on GSL will be broadcast to LSL. If the don’t-care state is true, the local search-line pair will always be discharged to ground without a voltage swing. However, if the don’t-care state is false, then the local search line will be active and perform the search operation after the search data are propagated from GSL. Accordingly, the hierarchy search-line scheme can reduce the power consumption by decreasing the switching capacitances and switching activities without adding any searching time overhead.

Unlike the conventional hierarchical search-line [17], the don’t-care-based hierarchical search-line does not increase the search delay of the search operation. Fig. 5(c) shows the timing diagram of the don’t-care-based hierarchical search-line during a search operation. The search-lines are activated when the clock is high, and the delay path is through the D flip-flops, GSL buffers and GSL-to-LSL buffers. For a 50% duty cycle clock, the GSL-to-LSL buffer delay is clearly shorter than half of a clock cycle, and the critical path depends on the match-lines. Before the negative edge of the clock, search data have been transferred to the LSL. Therefore, the search time, which depends on the buffer delay (ml_pre buf delay) and the search delay of the match-lines, dominates the clock period. By exploiting the critical delay, the proposed search-line scheme can save power without adding any timing overhead.

V. DON'T-CARE BASED POWER GATING TECHNIQUES

Two power gating techniques, multi-mode data-retention power gating and super cut-off power gating, are proposed based on the characteristic of continuous don’t-care X patterns. The super cut-off power gating and the data-retention power gating are applied in don’t-care cells and storage cells, respectively. They reduce the standby power by reducing leakage current. Fig. 6 schematically depicts super cut-off power gating

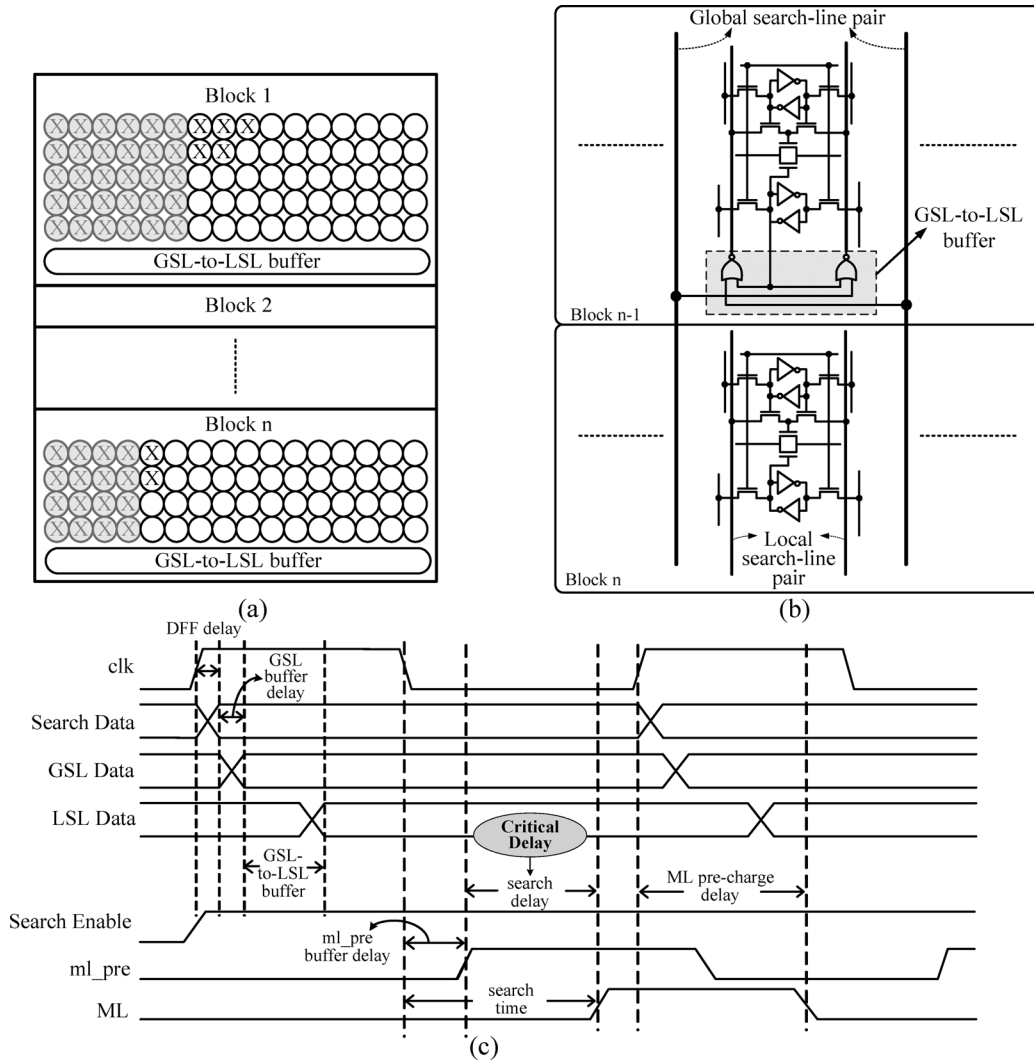


Fig. 5. (a) Architecture of don't-care based hierarchical search-line. (b) Circuit implementation of don't-care based hierarchical search-line. (c) Timing analysis of a search operation.

and multi-mode data-retention power gating in a TCAM segment. Additionally, Fig. 6 presents the tables associated with the corresponding control signals. The sleep signal indicates that the TCAM macro is in standby mode, and the most significant bit (MSB) and last significant bit (LSB) of a TCAM segment reveal the don't-care states in this segment. If both MSB and LSB are 1, then all TCAM cells in this segment are in the don't-care states. Therefore, the operations of the proposed power gating techniques depend on the above control signals. Power gating approaches are described and analyzed below.

A. Multi-Mode Data-Retention Power Gating

The multi-mode data-retention power gating is utilized in storage cells, and modified from the power gating devices that we proposed elsewhere [29]. Fig. 6 presents the circuitry associated with multi-mode data-retention power gating. The regular power gating nMOS (M1) and a diode-connected nMOS (M3), whose functions are similar to those in our earlier investigation [29], are adopted herein, but the pMOS diode is replaced by M1 to improve speed in the active mode. Additionally, an additional

nMOS (M2) is added to the stack to increase the virtual ground voltage. The diode-connected nMOS causes the virtual ground to saturate to a limited voltage which depends on the threshold voltage of M3.

The three modes of data-retention power gating control circuit are active, data-retention and cut-off modes, respectively. Fig. 6 also presents the truth table of the control signals in these three modes. When the storage cell is in the active mode, both control signals are set to high and the power gating transistors are turned on to support full-speed operation. When the circuit enters the data-retention mode, ctrl1 will be high and ctrl2 will be low. M3 just represents a diode, which causes the voltage of the virtual ground to saturate and provides a sufficient noise margin. If the virtual ground voltage established by the leakage current increases beyond the saturation value, then M3 will be turned on and the virtual ground voltage will discharge through it. Accordingly, the virtual ground declines back to the saturated value, guaranteeing the stability of the data storage cells. When all don't-care cells in a TCAM segment are set to the don't-care state, the data that are stored in storage cells are meaningless and can be eliminated. Therefore, the data-retention power gating

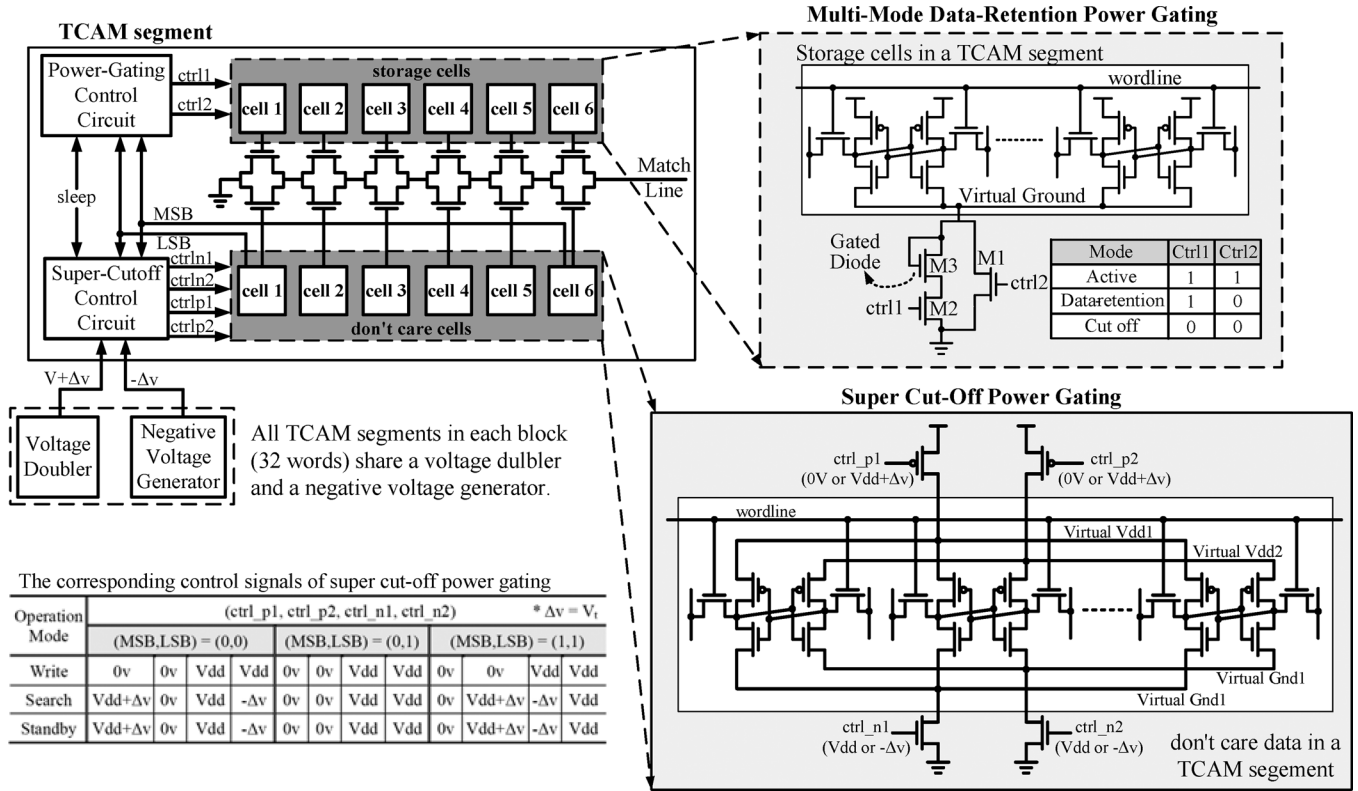


Fig. 6. Schematics of super cut-off power gating and multi-mode data-retention power gating techniques.

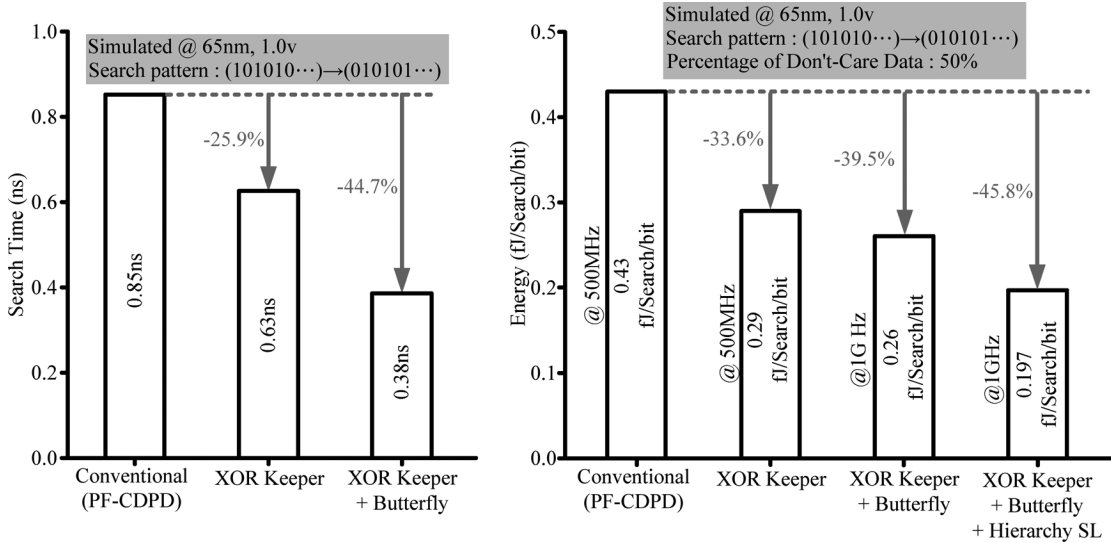


Fig. 7. Analysis of the search time and energy consumption under different energy-efficient schemes.

control circuit will be switched to the cut off mode while the most significant bit (MSB) of the don't-care cells is set to high.

B. Super Cut-Off Power Gating

Super cut-off power gating is a well-known power gating approach, and has been explored elsewhere [30]. However, the super cut-off technique is not favorable when applied to SRAMs, because in this approach the signals that are transmitted to the cell array must preserve the data even in stand-by mode. Furthermore, super cut-off power gating suffers from a

long wake-up time and a high current peak in the sleep-to-active transition. As determined by the continuous don't-care X patterns, don't-care cells in a segment are all set to 1 or 0, except in the segment that is located at the boundary of the don't-care X patterns. However, the super cut-off power gating technique is effective for don't-care cells without a long wake-up time and a high current peak.

Fig. 6 presents the circuit implementation of super cut-off don't-care cells. It also shows the corresponding control signals (P1, P2, N1, N2) under various operations. When all the

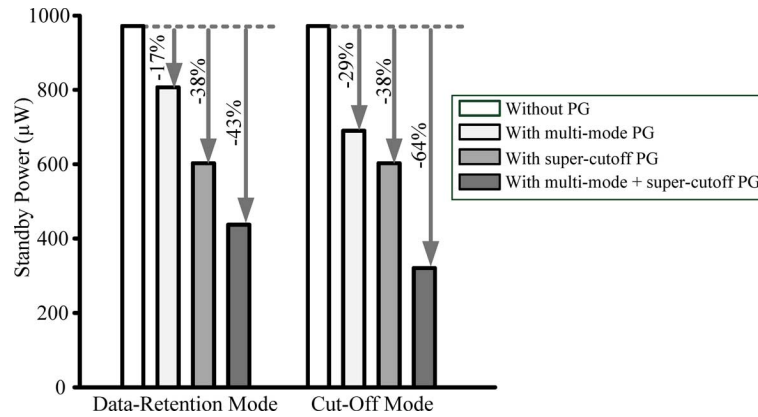


Fig. 8. Standby power analysis under different power gating techniques.

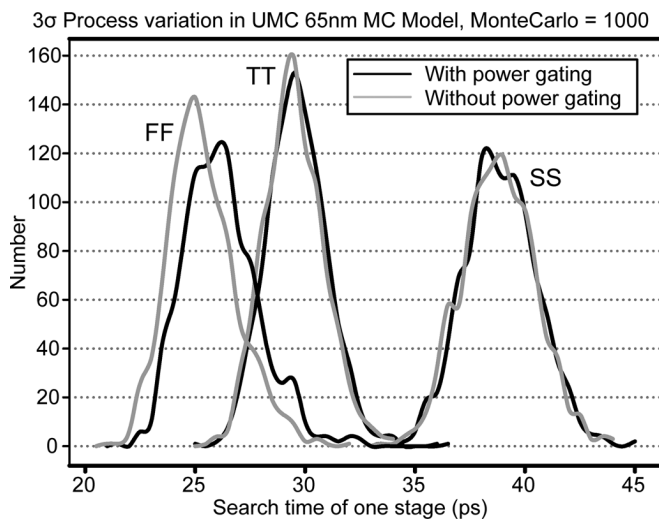


Fig. 9. Search time of one stage under 3σ process variations.

don't-care cells in the segment are set to 1, P1 and N2 are turned on to preserve the data in the don't-care cells. Additionally, P2 and N1 are turned off to reduce leakage currents. The situation is similar to that in which all the don't-care cells in the segment are set to 0, where P1 and N2 are turned off and P2 and N1 are turned on. Accordingly, each segment contains four cut-off switch transistors to reduce leakage power and preserve data in the don't-care cells. The cut-off voltages are $V_{dd} + \Delta v$ for pMOS and $-\Delta v$ for nMOS, which voltages are generated from a VBB generator and a voltage doubler [31], [32]. Since the subthreshold leakage depends exponentially on the gate-source voltage, the super cut-off technique considerably reduces the subthreshold leakage. Restated, when a larger overdrive voltage is applied to the cut-off transistor, the subthreshold leakage is lower. However, two design-limiting factors should be considered. First, the increase in the gate-drain voltage caused by the overdrive voltage at the gate may increase the gate leakage, which also depends strongly on the gate-source voltage. The second limiting factor is the over-stress voltage across the gate-source node, which may cause the gate oxide to break down. In UMC 65 nm CMOS technology, the oxide stress voltage will not exceed VDD when the gate overdrive voltage is less than 0.5 V. Additionally, since the subthreshold leakage

is exponentially related to the gate-source voltage in the weak inversion region, the subthreshold leakage may be significantly reduced by increasing the cut-off switch gate voltage. Hence, the overdrive voltage in this approach is set to 0.3 V, which is the threshold voltage of a normal V_t device in UMC 65 nm CMOS technology.

The super cut-off control circuit between the voltage generators and the don't-care cells must comprise level converters that prevent short currents. The control circuits that are associated with the pMOS super cut-off switch and the nMOS super cut-off switch were proposed in [23]. They are constructed from cross coupling level shifters to prevent short circuits. Furthermore, a voltage doubler [31] and a VBB generator [32] are realized to provide $V_{dd} + \Delta v$ and $-\Delta v$, respectively. To reduce the area overhead of the voltage generators, 32 match-lines are employed in the energy-efficient TCAM macro.

The power reduction of the super cut-off power gating technique is independent of the percentage of don't-care bits in the TCAM macro because the super cut-off power gating can be applied to all segments in a match-line, except for the segment at the boundary of continuous don't-care patterns. Moreover, the super cut-off power gating technique does not degrade the cell stability in standby mode. In fact, a charge path and a discharge path exist from the supply and the ground to node-1 and node-0, respectively. Accordingly, the super cut-off power gating technique has two main advantages. First, the cell stability is maintained and the data are not destroyed when the charge/discharge paths in don't-care cells are preserved. Second, nearly half of the SRAM cells in the TCAM macro, the don't-care cells, operate in super cut-off mode, reducing the leakage current.

VI. TCAM MACRO IMPLEMENTATION AND MEASUREMENTS

In this section, an energy-efficient 256×144 TCAM macro was implemented using UMC 65 nm CMOS technology. The energy-efficient 256×144 TCAM performs a high-speed and low-power search operation using PF-CDPD circuits, the butterfly match-line scheme, the XOR-based conditional keeper and the don't-care based hierarchy search-line scheme. Furthermore, the TCAM macro reduces the leakage current via multi-mode data-retention power gating and super cut-off power gating techniques. The TCAM array is 256-word \times 144-bit, and is divided into eight blocks. Each block is composed of

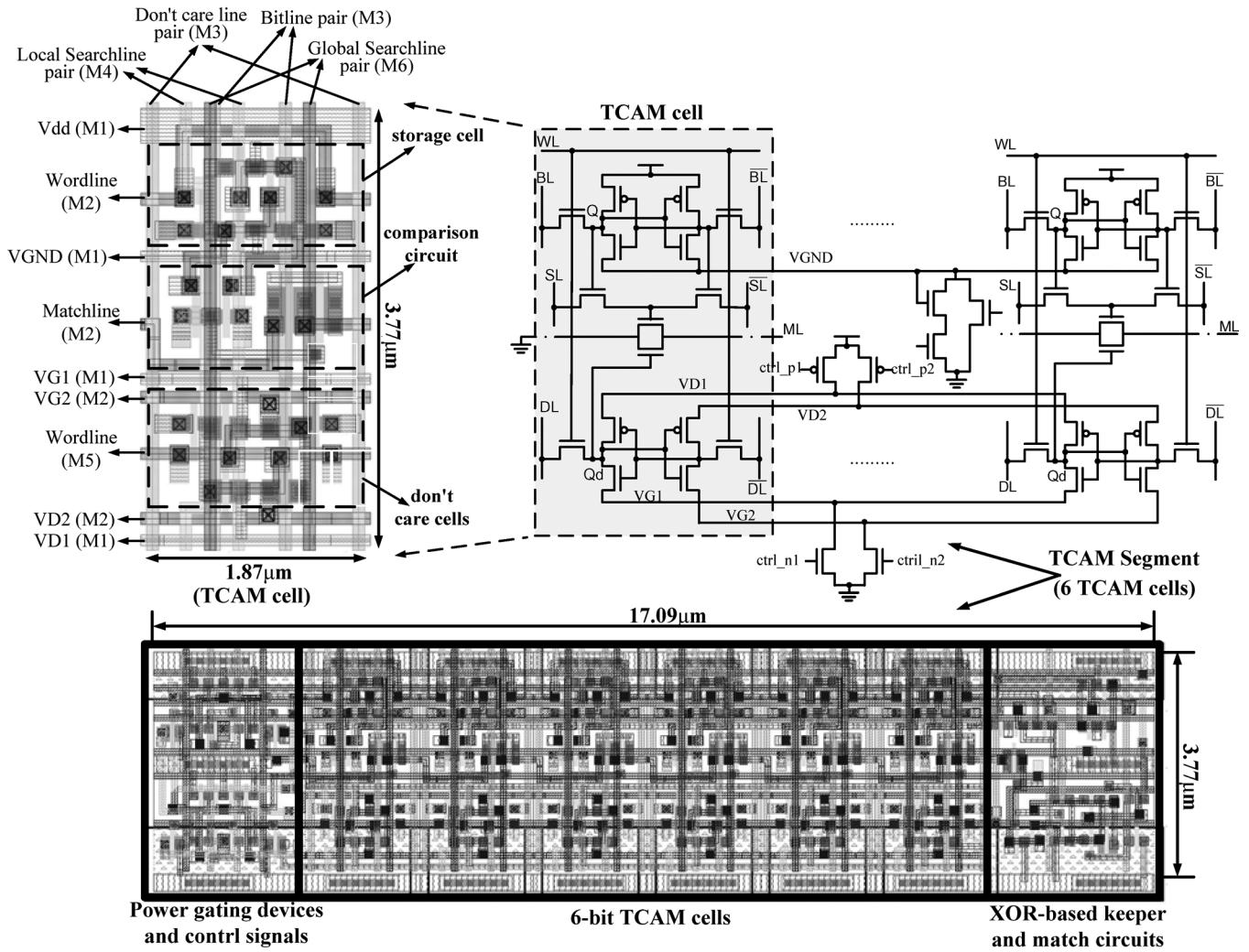


Fig. 10. Layout view of 1-bit TCAM cell and a TCAM segment with 6-bit TCAM cells.

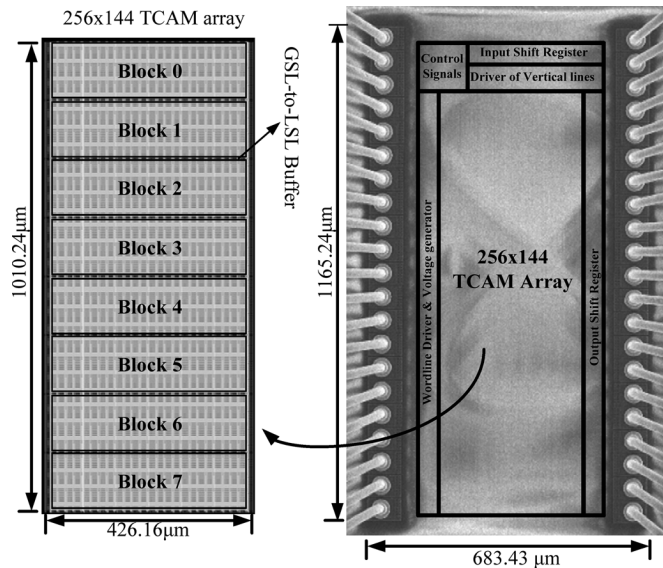


Fig. 11. Layout view of 256 × 144 TCAM array and test chip micrograph.

64 match-lines with a VBB generator, a voltage doubler and GSL-to-LSL buffers. In the VBB generator and the voltage

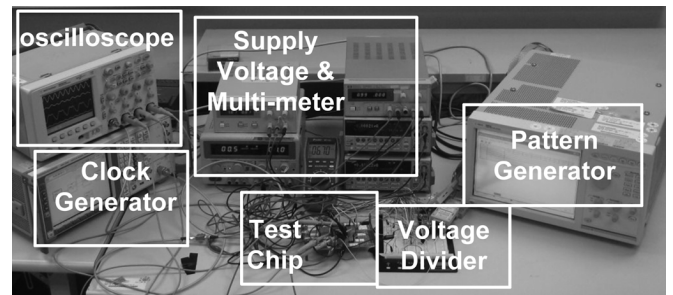


Fig. 12. Measurement setup.

doubler, the cut-off voltage is 1.3 v ($V_{dd} + V_t$) for the pMOS cut-off switch and -0.3 v ($-V_t$) for the nMOS cut-off switch. Each block, in addition, has its own VBB generator and voltage doubler, which is associated with the 32×24 six-bit TCAM segments. The clock rate of the charge-pump circuits equals the system clock rate.

The butterfly match-line with XOR-based conditional keepers can reduce search time based on PF-CDPD circuits. Fig. 7 shows the reduction in the search time achieved using the butterfly match-line and the XOR-based conditional keeper.

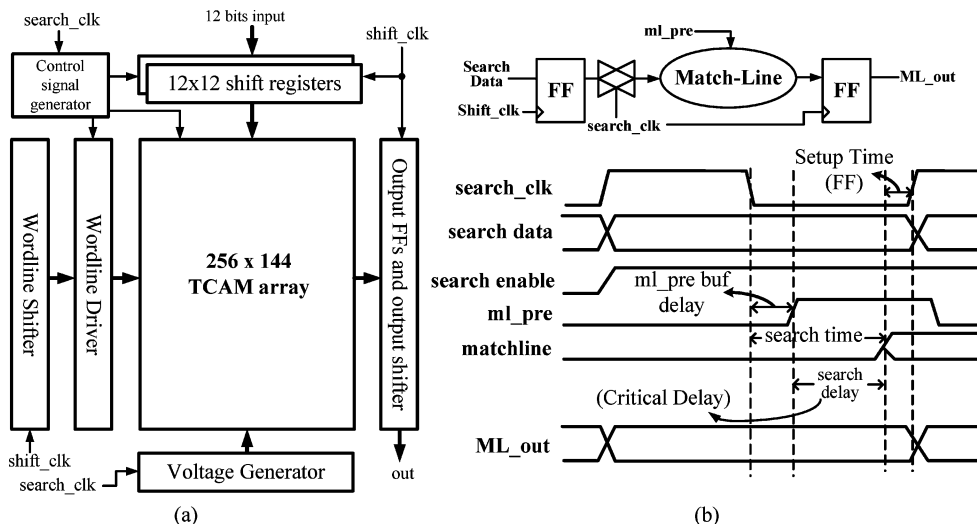


Fig. 13. (a) Block diagram of the test chip. (b) Test strategy.

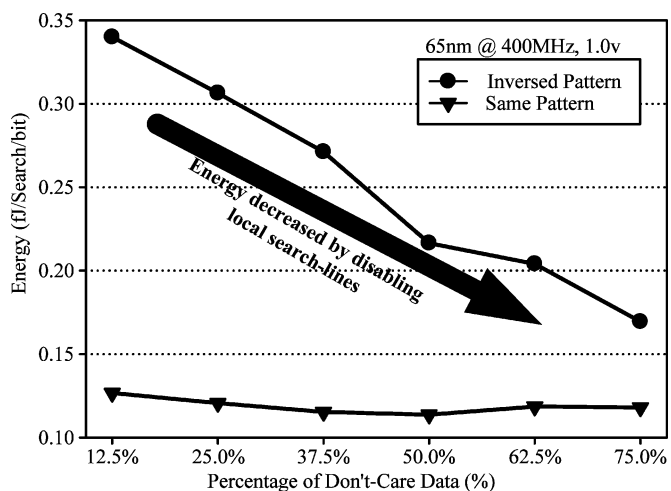


Fig. 14. Energy consumption under different don't-care patterns.

The search time is defined in Fig. 5(c), and the simulation is based on the worst-case patterns from (101010...) to (010101...). The butterfly match-line with XOR-based conditional keepers reduces the search time by 44.7% below that achieved using the conventional PF-CDPD match-line scheme. Fig. 7 also presents the analysis of the energy consumption under different energy-efficient schemes. The simulation is conducted using the worst-case patterns, 50% don't care data, 1.0 v supply voltage and the highest possible frequencies, which are listed at the side of the bars. The XOR-conditional keeper reduces the energy consumption to 33.6% below that of the PF-CDPD match-line with the conventional keeper, and exhibits enhanced immunity to noise. Additionally, the butterfly match-line scheme with XOR conditional keepers reduces the energy consumption by 39.5%. The don't-care based-hierarchy search-line schemes further reduce the energy by approximately 45.8%, reducing the power consumption of the search-lines.

The standby power with and without power gating is analyzed. Fig. 8 presents the standby power under the different power gating approaches. Super cut-off power gating reduces

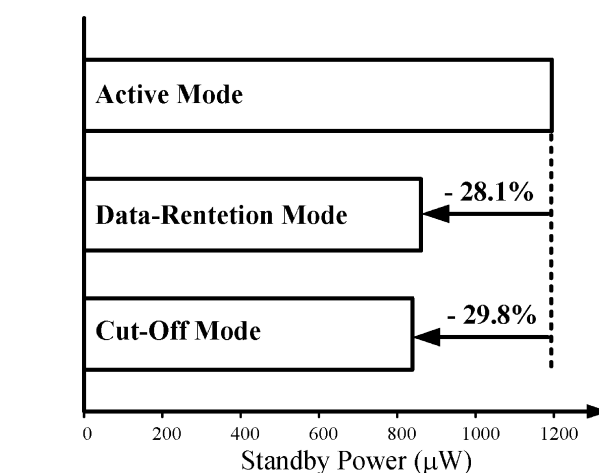


Fig. 15. Average standby power with different power gating modes.

the leakage current by 38% by increasing the gate-drain voltage. Additionally, the multi-mode data-retention power gating reduces the leakage power by 17% and 29% in the data-retention and cut-off modes, respectively. If both power gating techniques are applied, the leakage power is further reduced. However, the process variation has become one of the critical design challenges in shrinking to nano-scale technologies [33]. Fig. 9 presents the search delay of one TCAM stage with/without the power gating techniques under 3σ process variations in UMC 65 nm MC (Monte-Carlo) model with three corners (TT, SS and FF). The search delay with power gating is similar to that without power gating since the discharging paths are determined by NMOSs, which are controlled by the comparisons of stored data and search data. Fortunately, the comparisons were finished before pre-charging the floating node via the PF-CDPD circuitry [15]. Therefore, the variation in search time in the TCAM stage, ranging from 20–45 ps, is tolerant.

Based on the power gating techniques and hierarchy search-line schemes, each TCAM cell needs extra metal layers to route extra virtual ground, virtual Vdd and global search-lines. Fig. 10

TABLE I
FEATURES SUMMARY AND COMPARISONS

	Hybrid [19] (JSSC 2005)	PF-CDPD [15] (JSSC 2006)	Range Match [16] (ISSCC 2006)	Tree-style [17, 21] (JSSC 2008)	Charge Recycling [22] (ASSCC 2008)	This Work	
						Simulation	Test Chip Measurement
configuration	1024x144	256x128	512x144	256x128	1024x144	256x144	
Technology	100 nm	0.18 μm	0.13 μm	0.18 μm	0.18 μm	65 nm	
Area (mm ²)	2.8x4.2 (chip)	1.21x0.56 (core)	1.5x1.7 (core)	0.84x0.92 (core)	3.67x0.98 (core)	1.01x0.43 (core)	
Supply voltage (V)	1.2 V	1.8 V	1.2 V	1.8 V	1.8V	1.0 V	
Search time (ns)	2.20 ns	2.10 ns	4.80 ns	1.56 ns	100MHz	0.38ns	400MHz
Energy metric (fJ/bit/search)	0.700	2.330	0.590	1.420	6.300	0.113	0.165
Normalized Search time T* (ns)	1.716	1.365	2.880	1.014	N.A.	0.380	N.A.
Normalized Energy metric E* (fJ/bit/search)	0.316	0.260	0.205	0.158	0.702	0.113	0.165

shows the layout view of a 1-bit TCAM cell and a TCAM segment with 6-bit TCAM cells. A TCAM cell is composed two SRAM cells and a comparison circuit. The size of a TCAM cell is $3.77 \times 1.87 \mu\text{m}^2$. To reduce the loading capacitance, the search-line pair and the bit-line pair are separated to reduce both the search-time and the power consumption. However, two more vertical lines must then be added. Therefore, the bit line pair (M4), the don't-care line pair (M3), the LSL pair (M4) and the GSL (M6) pair are routed along the vertical axis. Two horizontal metal lines, M1 and M2, are preserved as power lines, virtual ground and virtual Vdd. Furthermore, the upper word-lines and match-line are along the horizontal axis using M2. The lower word-line is routed through M5. M5 is also utilized to realize the butterfly connection. Nevertheless, the area of the proposed TCAM cell is 3 times as large as a 65 nm TCAM cell proposed in [34]. The addition of metal tracks further increase the bit-cell area which is a wire-limited design based on butterfly match-line, hierarchy search-line and power gating. Therefore, a trade-off exists between the area efficiency and energy efficiency while adopting energy-efficient schemes. Fig. 10 also presents the layout of a TCAM segment that consists of 6-bit TCAM cells, a XOR-based conditional keeper, a match-line circuit, power gating devices and power gating control circuits. The keeper and match-line circuit are placed at the right-hand side of a TCAM segment. The left-hand side contains the power-gating devices and the corresponding control signals. The size of one TCAM segment is $3.77 \times 17.09 \mu\text{m}^2$. Fig. 11 displays the layout of the 256×144 TCAM array. Fig. 11 also presents the floorplan and the test-chip micrograph. The 256×144 TCAM array is divided into eight blocks, each with 32 match-lines. The GSL-to-LSL buffers are placed between pairs of adjacent blocks. The total sizes of the TCAM array and the test chip are 426×1010 and $683 \times 1165 \mu\text{m}^2$, respectively.

Fig. 12 displays the measurement setup. A pattern generator and voltage dividers are utilized to set up the TCAM array, and two clocks, the shift clock and the search clock, are generated by the pattern generator and clock generator, respectively. Fig. 13(a) shows the block diagram of this test chip. The test strategy is divided into two phases. The first phase is to input the data in the TCAM array, and the second phase is the search operation. In the first phase, 12×12 shift registers and a word-line

shifter are adopted to write data in the 256×144 TCAM array. After the storage data and the don't-care data are set, the search data are inputted into two 12×12 shifter registers. Then, the test enters the second phase. In the second phase, the shift clock is turned off, and the search clock is turned on to perform the search operation. The search data in these two 12×12 shifter registers are thereby transferred into the search-lines. To measure the worst-case patterns, the search data in these two shifter registers are set to be mutually complementary. After the search operation has been complete, the output shifter shifts the results of the match-lines and checks the functionality of the TCAM macro. Fig. 13(b) plots the corresponding waveform. However, this test chip cannot measure the search delay because the search frequency is limited by the pad.

The TCAM array is operated at 1 V and 400 MHz, which frequencies are limited by the pads. Fig. 14 shows the energy matrix for various percentages of don't-care data. Additionally, the applying search data are as one pattern in one of the two shift registers and the same pattern or the same one inverted in the other shifter register. As the proportion of don't-care data increases, the energy dissipation is reduced because the LSLs are disabled. When the same pattern is input repeatedly, the energy consumption is almost independent of the percentage of don't-care data. For achieving the accurate measurement results, the properties of routing tables in IPv6 should be considered.¹ From the prefix length distribution in the router of 6Bone, the distributions of the prefix length equal to 32, 48, 35, 24, and 28 are approximately 86.21%, 4.76%, 3.78%, 1.31% and 1.31%. According to these statistics, more than half of TCAM cells in a routing table are don't-care bits. Moreover, most TCAM segments would not be activated in search operations. Applying 50% don't-care data, Table I summarizes the performance of the proposed TCAM and other recently proposed TCAMs. The normalized factors are modified from another investigation [35], and (2) is derived:

$$\begin{cases} E^* = E \times \left(\frac{65}{\text{Technology}} \right) \times \left(\frac{1.0}{V_{DD}} \right)^2 \\ T^* = T \times \left(\frac{65}{\text{Technology}} \right) \times \left(\frac{V_{DD}}{1.0} \right) \end{cases} \quad (2)$$

¹<http://go6.net/ipv6-6bone>

where E and T represent the energy and the delay time, respectively, and E^* and T^* denote the normalized factors for 65 nm CMOS technology and a supply voltage of 1.0 V. The search time determined from the simulation result is 0.38 ns. Additionally, the energy metric of the test chip is 0.165 fJ/bit/search. According to Table I, the comparisons of the proposed energy-efficient TCAM and other TCAM approaches reveal that the proposed TCAM has very competitive search speed and energy efficiency.

Although the normalized energy of a tree-style match-line is a little smaller than that of the proposed approach, the tree-style match-line suffers from leakage problems when the technology is shrunk to the nano-scale. Fig. 15 presents the standby power with different power gating modes. The measured standby power differs from the simulated results. The simulation results reveal that the leakage saving in the cut-off mode exceeds that in the in data-retention mode when the multi-mode data-retention power gating is used. The measurements demonstrate that the standby power in the cut-off mode is almost the same as that in the data-retention mode, perhaps because of the floating node of the virtual ground in the multi-mode data-retention power gating.

VII. CONCLUSION

This work has presented an energy-efficient TCAM design approach, which exploits the co-design of the architecture and circuit. To achieve low-power and high-performance TCAM architecture, a don't-care-based hierarchy search-line scheme and a butterfly match-line scheme have been presented. The hierarchy search-line reduces power consumption by reducing not only the switching activity but also the capacitance of the search-lines. The butterfly match-line scheme reduces not only the search time but also the power consumption by exploiting a high degree of parallelism and dependence of sub match-lines. The proposed TCAM match-line was also implemented using a noise-tolerant XOR-based conditional keeper to perform energy-efficient search operations for match-lines. As technologies advance, leakage currents increasingly dominate the overall power consumption of nanoscale technologies. Accordingly, the super cut-off technique and the multi-mode data-retention power gating technique were utilized to reduce leakage currents significantly in standby mode. Furthermore, the super cut-off power gating technique also reduces the leakage current in the search operations without reducing the search time or destroying the noise margin. Based on UMC 65 nm CMOS technology, an energy-efficient 256-word \times 144-bit TCAM array was implemented. The experimental results demonstrate that the leakage power is reduced by 19.3% and the energy metric of the TCAM is 0.165 fJ/bit/search. The proposed TCAM will be very useful in further nanoscale CMOS technology.

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