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Memory properties of metal/ferroelectric/semiconductor and metal/ferroelectric/insulator/semiconductor structures using rf sputtered ferroelectric $Sr_{0.8}Bi_{2.5}Ta_{1.2}Nb_{0.8}O_9$ thin films

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Abstract

Off-axis rf magnetron sputtering has been employed to grow $Sr_{0.8}Bi_{2.5}Ta_{1.2}Nb_{0.8}O_9$ (SBTN) ferroelectric thin films with (115) preferred orientation on SiO_2/Si and Si substrates. The lower temperature and the higher oxygen mixing ratios [OMR, O_2/($Ar+O_2$)] used in film processing lead to reduction in the leakage current densities and widening the memory window of the resultant metal–ferroelectric–insulator–semiconductor (MFIS) structures. The maximum memory windows of the MFIS structures based on 40% OMR SBTN films deposited at 500 °C on SiO_2/Si substrate are 2.87 and 2.27 V at the bias amplitudes of 10 and 8 V, respectively. With increasing applied voltage, the memory window also increases. The memory window decreases from 2.27 to 1.59 V after the 10^{11} switching cycles at a bias amplitude of 8 V. The capacitance difference, ΔC, between the two states decreases by 48% after retention time of 7000 s.
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Keywords: Fatigue; Ferroelectric properties; Films; Lifetime; SBTN; Sputtering; (Sr,Bi)(Ta,Nb)O_3

1. Introduction

Ferroelectric thin films are promising for nonvolatile memory applications. At present, the capacitor-type ferroelectric random access memory (FRAM) is used in a destructive readout[1,2] operation. In principle, it is much more desirable to develop nonvolatile memory device based on the metal–ferroelectric–semiconductor field–effect transistor (MFSFET) to serve both as the storage element and the sensing device with a non-destructive readout operation.[3,4] However, it is extremely difficult to prepare the ferroelectric/Si structure with good interface because of the chemical reaction and the interdiffusion of Si and ferroelectric materials. Therefore, an insulating buffer layer is usually inserted between the ferroelectric material and Si, resulting in a metal–ferro-electric–insulator–semiconductor (MFIS) structure.[5–9] The $Sr_{0.8}Bi_{2.5}Ta_{1.2}Nb_{0.8}O_9$ film is used as ferroelectric film because the film exhibited no fatigue up to 10^{10} cycles, and had excellent retention characteristics and a low leakage current in comparison with other related compounds.[10,11] The material SiO_2 is selected as an insulator in MFIS structures because the combination of SiO_2–Si is believed to be the most stable and promising structure to control the gate potential precisely through FET channel due to its excellent interface characteristics and also to achieve reliability with regard to fatigue or retention characteristics in the operation of MFISFET.[5,8,9] Nevertheless, SiO_2 has a rather small dielectric constant that reduces the electric field and the polarization in SBT. Therefore, an effective way to increase the electric field in SBT is to decrease the SiO_2 film thickness. However, as the thickness of the SiO_2 layer is reduced, preventing a mutual diffusion between SBT and Si substrate and hence the degradation of the SiO_2–Si interfaces is a challenging task. Therefore, the thickness of this buffer layer must be chosen properly. In this paper, the 27 nm thick SiO_2 film is employed for maintaining excellent MFIS characteristics.

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2. Experimental

The MFIS and MFS structures based on SBTN films were fabricated by the following procedure: First, the silicon wafer was cleaned by a standard RCA cleaning process. Subsequently, 27 nm thick SiO_2 layer was thermally grown at 1050 °C in a dry oxidation furnace. Then the 400 nm thick SBTN thin films were deposited on bare Si(*n*-type) and SiO_2/*n*-Si(100) substrates at various temperatures and OMR by off-axis rf magnetron sputtering, using a 2 inch diameter $Sr_{0.8}Bi_{2.5}Ta_{1.2}Nb_{0.8}O_9$ (SBTN) targets synthesized by a standard solid-state reaction process. The thicknesses of the SiO_2 and the SBTN thin films were determined using ellipsometry and scanning electron microscopy (SEM). The surface roughness and morphology of the SBTN thin film deposited at 500 °C in various OMR were observed with atomic force microscopy (AFM). The Pt top electrodes with diameters of 150, 250 and 350 μm were deposited by rf magnetron sputtering using a shadow mask followed by annealing at 400 °C. The MFIS and MFS structures with the SBTN crystallized films sputtered on the SiO_2/*n*-Si and bare *n*-Si substrates at 500° in various OMR were characterized by a Rigaku X-ray diffractometer to detect crystalline structure and preferred orientation of SBTN films. For the electrical measurements, back electrode Al was vacuum evaporated to form Pt/SBTN/SiO_2/*n*-Si/Al(MFISM) and Pt/SBTN/*n*-Si/Al(MFSM) structures. The leakage current density was performed using HP 4156B semiconductor parameter analyzer with 1 s delay time. The capacitance–voltage (C–V) characteristics were measured using HP4284 LCR meter. To measure the C–V characteristics, the voltage was applied from the accumulation to the inversion with a sweep rate of 0.1 V/s at 100 kHz.

3. Results and discussion

Fig. 1 shows X-ray diffraction (XRD) patterns of Pt/SBTN/Si and Pt/SBTN/SiO_2/Si deposited at 500 °C in various OMR and all SBTN films are polycrystalline structure. The preferred (115) peak intensity increases with decreasing OMR for SBTN films on SiO_2/Si. The grain size can be calculated from the Scherrer's formula which is inversely proportional to full width half-maximum (FWHM) of XRD peak. The average grain size values for SBTN films deposited at 500 °C for MFS structure in 40% OMR and deposited at 500 °C for MFIS structure in 10, 25, and 40% OMR are 12.8, 24.1, 22.8, and 21.6 nm, respectively. Fig. 2(a), (b) and (c) show the AFM surface images of various OMR SBTN films deposited at 500 °C. The root-mean-square (rms) surface roughnesses of SBTN films are decreased with increasing OMR during sputtering, which are 52, 46, and 43 nm for 10, 25, and 40% OMR SBTN films. The

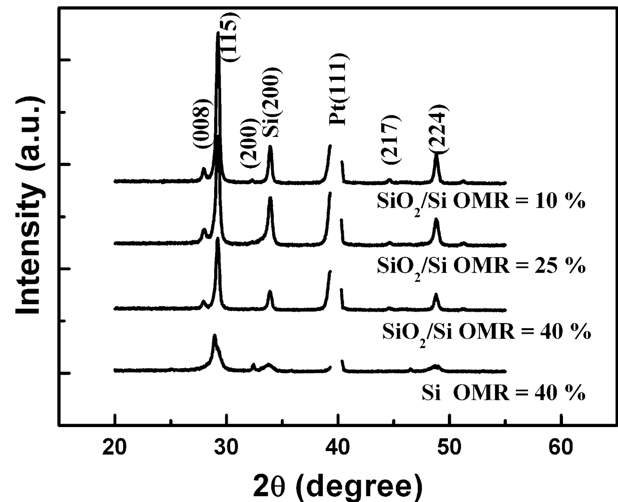

Fig. 1. XRD patterns of the Pt/SBTN/Si and Pt/SBTN/SiO_2/Si structures using SBTN films deposited at 500 °C in various OMR.

higher OMR in the sputtering gas decreases the deposition rate of the film. Smaller grain size and a lower film deposition rate at higher OMR may result in a smoother surface. Fig. 3 indicates the normalized C–V curves for Pt/SBTN/Si and Pt/SBTN/SiO_2/Si structures based SBTN films deposited at 500, 525, and 550 °C in 40% OMR. The sweeping voltage is changed in either direction from −10 to + 10 V, and the frequency of the measuring signal is 1 MHz. The memory windows are about 2.87, 2.4, and 0.6 V in MFIS structures with SBTN films deposited at 500, 525, and 550 °C, respectively and that is 0.9 V in MFS structure. Fig. 4 shows the comparison of the leakage current density vs electric field for the MFS and MFIS structures with SBTN films deposited at various temperatures in 40% OMR. It indicates that leakage current density of the MFS structure is about 1×10^{-5} A/cm^2 at 200 kV/cm while the MFIS structures with 500, 525, and 550 °C SBTN films have lower leakage current densities of about 1×10^{-9}, 3×10^{-9}, and 1×10^{-8}A/cm^2 at 200 kV/cm, respectively. The inset in Fig. 4 depicts that the leakage current increases and memory window decreases with increasing substrate temperature. The correlation of the leakage current with memory window implies that higher leakage current seriously deteriorates the width of memory windows. On the basis of the comparison of the C–V and J–E curves, it is indicated that the interdiffusion at the interface of SBTN/Si is worse than that of SBTN/SiO_2 and the higher deposition temperature favors the interfacial diffusion occurred. The interdiffusion occurs at the interface of SBTN/Si during fabrication, leading to increase interface trap density, which also implies a change in Si surface conductivity. This could be detrimental to the ferroelectric switching property. The failure of controlling the surface conductivity is supposed to be caused by the ferroelectric border traps,[12,13] which are the near-interface oxide traps in ferroelectric films

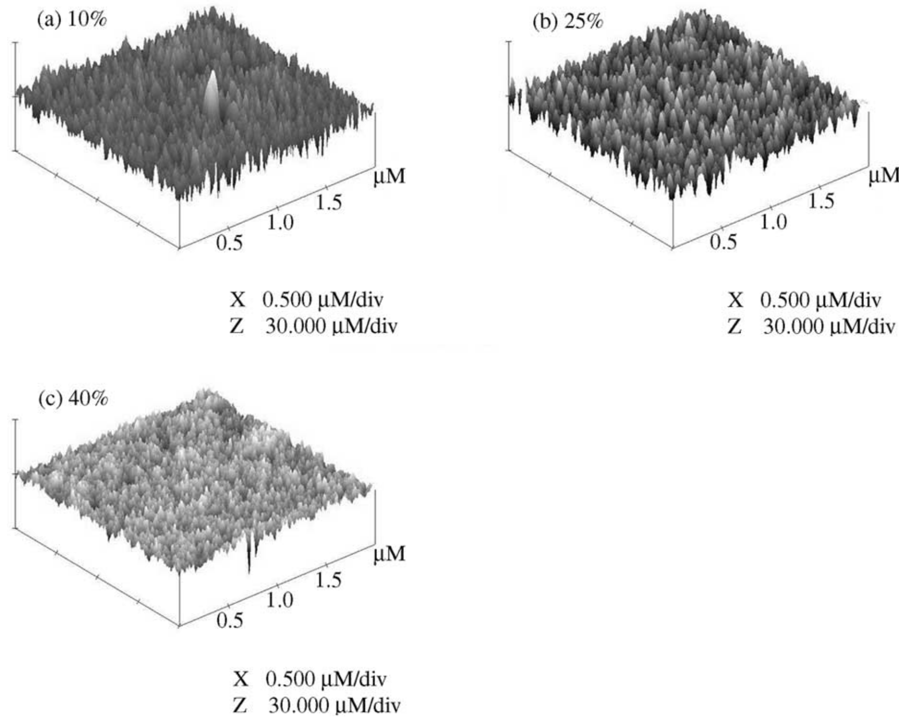

Fig. 2. The AFM surface images of SBTN films deposited at 500 °C in various OMR.

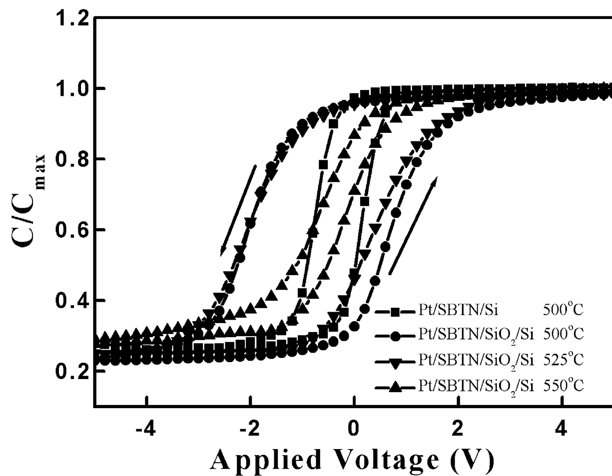

Fig. 3. The normalized C–V of Pt/SBTN/Si and Pt/SBTN/SiO_2/Si diodes based on the 40% OMR SBTN films deposited at 500, 525, and 550 °C.

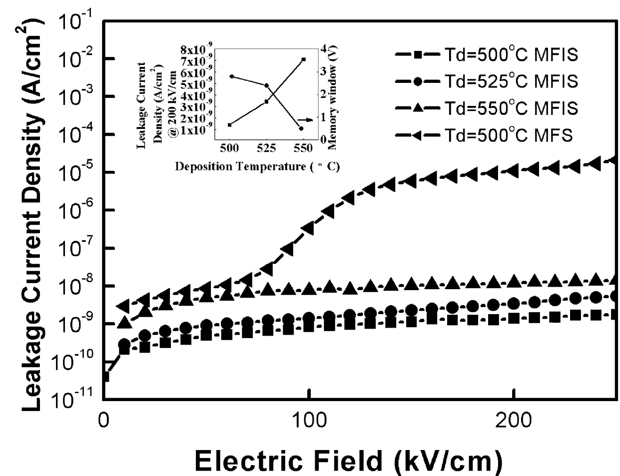

Fig. 4. Plots of leakage current density vs electric field of the MFIS structures with SBTN films deposited at various substrate temperatures indicated and that of the MFS structure at 500 °C. The inset shows relations between the leakage current density at 200 kV/cm and the memory window at various deposition temperatures of SBTN films on SiO_2/Si substrates.

communicating with the underlying Si. Therefore, the buffer layer is necessary for obtaining a better interface. The native oxide might be formed during film deposition process. The charge injection from the semiconductor to the film possibly dominates across the native oxide when high concentration traps exist in the native oxide. The memory windows also narrow down as the charge injection and leakage current increase. Hence, the silicon dioxide is very important as a barrier layer in order to lower the leakage current of the device.

The OMR used in the sputtering process is an important factor that affects the crystallinity of SBTN films deposited at 500 °C, which was confirmed in Fig. 1. The (115) peak intensity shown in Fig. 1 decreases with increasing OMR. The 10% OMR SBTN film exhibits the strongest (115) peak intensity, indicating that this film has better crystallinity. Fig. 5 depicts the curves of normalized C–V of the Pt/SBTN/SiO_2/n-Si(100) MFIS structure using 500 °C, various OMR deposited SBTN films. According to previous investigations,[14–16] the ferroelectric property of SBTN can cause the

counterclockwise hysteresis C–V loop for MFIS capacitors with *n*-type Si and the clockwise direction for MFIS capacitors with p-type Si. It shows counterclockwise dielectric hysteresis loops in Fig. 5, which are clearly observed as traced by arrows. We use *n*-type Si as the substrates in the present study, therefore, the memory effects in Fig. 5 are due to the ferroelectric domain reversal but not due to the charge injection. It is obvious from the Fig. 5 that the memory window tends to decrease as the OMR is lowered. Fig. 6 shows that the leakage current density increases with decreasing OMR in MFIS structure, while MFS structure has larger leakage current density than MFIS structure because the high resistively SiO_2 insulator (band gap, 9 eV) layer blocks current flow efficiently. The higher OMR in MFIS structure has lower leakage current density because oxygen vacancies diminish with higher OMR leading to the decrease in the electron concentration.

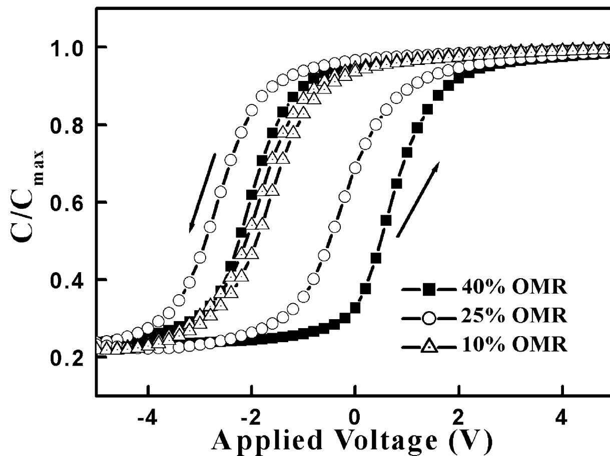

Fig. 5. The normalized C–V of the MFIS structure based on SBTN films deposited at 500 °C for various OMR.

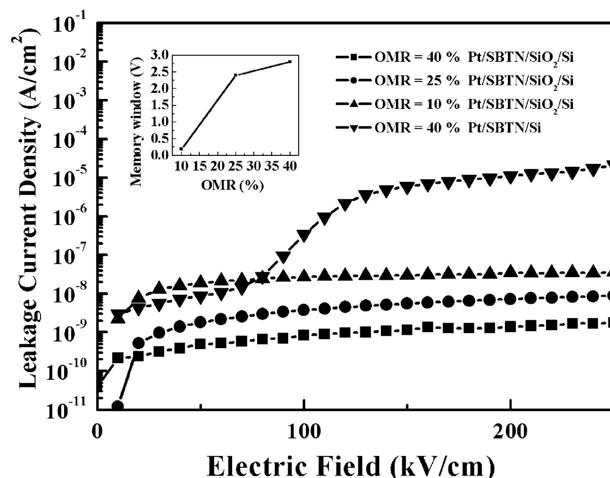

Fig. 6. Plots of leakage current density vs. electric field of the MFS and MFIS structures with SBTN films deposited in various OMR. The inset shows the performance of the memory window for the structures with various OMR SBTN films.

The smallest leakage current density is 1.38×10^{-9} A/cm^2 under applied electric filed of 200 kV/cm for the 500 °C and 40% OMR SBTN films. When the OMR increases during the sputtering process, the lower concentration of oxygen vacancies and roughness of the SBTN surface (Fig. 2) can be reduced so that the leakage current and local field of Pt/SBTN interface both decrease. The SBTN in the MFIS structures formed at lower OMR shows larger leakage current density, which leads to enhanced charge injection, and reduced counterclockwise C–V hysteresis and memory windows, which agrees with the previous results.[14,17]

Fig. 7 depicts the normalized C–V characteristics of the Pt/SBTN/SiO_2/Si structure incorporating SBTN film processed at 500 °C and 40% OMR. The memory window increases from 1.06 to 3.34 V when the applied voltage is changed from 4 to 12 V, and the widths of the memory windows are almost in proportion to the applied voltage, as shown in the inset of Fig. 7. This phenomenon is attributed to the non-saturation polarization of the SBTN thin films. Since the dielectric constant of SiO_2 is much lower than that of SBTN, the voltage drop in the SBTN is much lower than that in the oxide buffer layer. This insufficient electric field can not drive the SBTN thin film into a state of saturated polarization and therefore all the memory windows are operated in non-saturated sub-hysteresis loops. Therefore, increasing the applied voltage would promote the formation of more saturated hysteresis loop and wider memory window. The capacitance matching of the ferroelectric and insulator layers is important to increase the voltage drop in the ferroelectric layer, which can drive the ferroelectric into larger minor loop.[18]

Fig. 8 shows the curves of the C–V of the MFIS structure with the SBTN films deposited at 500 °C and 40% OMR films for various switching cycles as indicated in this plot. The fatigue test was performed using

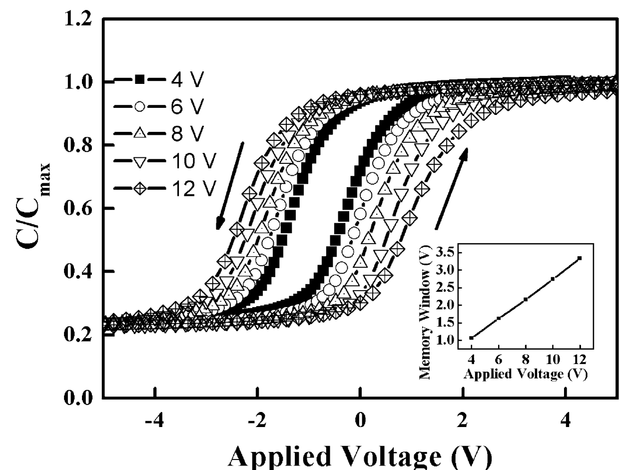

Fig. 7. The normalized C–V characteristics of the MFIS structure based on 500 °C, 40% OMR SBTN film. The inset shows the plot of the memory window vs. applied voltage.

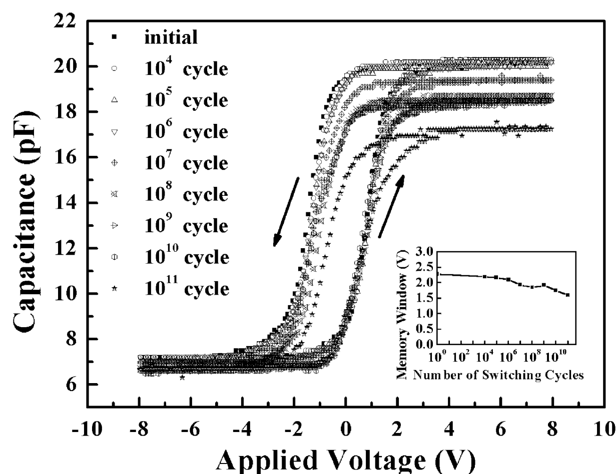

Fig. 8. Plots of the C–V of MFIS structure with the SBTN films deposited at 500 °C under 40% OMR for various switching cycles indicated.

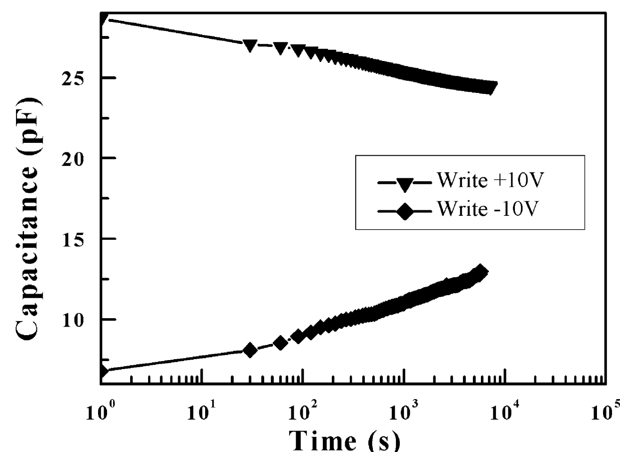

Fig. 9. Memory retention time of the $Pt/Sr_{0.8}Bi_{2.5}Ta_{1.2}Nb_{0.8}O_9/SiO_2/Si/Al$ capacitor, where 'on' and 'off' writing pulse voltages are +10 and −10 V, respectively.

a bipolar triangle wave of 8 V at 10 kHz below 10^6 cycles and 1 MHz over 10^6 cycles and the sweeping voltage change in either switching from +8 to −8 V. We survey the fatigue property using two different frequencies, 10 kHz and 1 MHz. It would have longer time to reverse the polarization of ferroelectric films at 10 kHz than at 1 MHz. Nevertheless, it could still have enough time to invert the polarization of ferroelectric films in accordance with former study.[10] It is shown in Fig. 8 that the accumulation capacitance reduced from its initial value after several cycles of switching duration. The reduced accumulation capacitance may be attributed to the decreased polarization of the SBTN film due to fatigue. Besides, the memory window decreases with increasing switching cycles. We find that the memory window degrades over 10^6 switching cycles due to fatigue. The memory window narrows from 2.27 to 1.59 V after 10^{11} switching cycles.

Memory retention time was measured for the $Pt/SBTN/SiO_2/Si/Al$ capacitor with the SBTN films deposited at 500 °C and 40% OMR, where 'on' and 'off' writing pulse voltages are +10 and −10 V. The measurement voltage was kept at 0 V. Fig. 9 shows the change in capacitance with time. The data storage and measurement are executed at room temperature. The memory capacitance decreases linearly as a function of the logarithm of the retention time. The capacitance difference, ΔC, between the two states decreased by 48% after retention time of 7000 s. Such poor retention may be attributed to small remanent polarization to saturation polarization ratio ferroelectric film, relatively high leakage current density of the MFIS structure and low dielectric constant of SiO_2 insulator layer.[14,18] As shown in Fig. 9, the writing at −10 V has a stronger degradation than the writing at +10 V. Such asymmetry is attributed to that the C–V curves (Fig. 3) shift left along voltage axis and do not show symmetrical with respect to zero voltage. This imprinted behavior may be resulted from some fixed charge in the insulating layer.

4. Conclusions

We have investigated the effects of substrate temperature and O_2/Ar ratio during rf magnetron sputtered SBTN films on the properties of MFS and MFIS structures based on SBTN films. Increasing the OMR increases the memory window and reduces the leakage current density. The SBTN films deposited at 500 °C and 40% OMR on SiO_2/Si substrate, which formed MFIS structures, have larger maximum memory window of 2.87 V at a sweeping voltage from +10 to −10 V. The buffer layer SiO_2 is necessary for avoiding the possible interdiffusion between SBTN and Si interface. The reliability of SBTN film has been examined through the fatigue and retention time tests. The width of memory window decreases from 2.27 to 1.59 V after 10^{11} switching cycles. The capacitance difference, ΔC, between the two states decreased by 48% after the retention time of 7000 s.

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