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LETTER TO THE EDITOR

High-speed (>10 Gbps) 850 nm oxide-confined vertical cavity surface emitting lasers (VCSELs) with a planar process and reduced parasitic capacitance

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Abstract

This study reports the high-speed performance of 850 nm oxide-confined vertical cavity surface emitting lasers (VCSELs) with a planar process and reduced parasitic capacitance. The parasitic capacitance of VCSELs was reduced using additional proton implantation. The small signal modulation bandwidth which was restricted by electric parasitic capacitance expanded from 2.3 GHz to 9 GHz after proton implantation. The reflection coefficient showed that the electric parasitic pole exceeded 20 GHz. An eye diagram of VCSEL with reduced parasitic capacitance operating at 10 Gps with 6 mA bias and 6 dB extinction ratio showed a very clean eye with a jitter of less than 20 ps.

1. Introduction

850 nm oxide-confined vertical cavity surface emitting lasers (VCSELs) have become a standard technology for applications in local area networks (LANs) and storage area networks (SANs). The main advantages of VCSELs are low threshold current, low divergence angle and circular beam, leading to simpler packaging and low electrical power consumption. The surface emission property of VCSELs also simplifies the two-dimensional arrays and enables wafer level testing, and thus low fabrication cost [1]. However, the electrical resistance of VCSELs is higher than that of edge-emitting lasers owing to their small current injection area and highly resistive DBRs. The small top contact area also increases contact resistance. For 10 Gbps operation, the 3 dB bandwidth should exceed 7 GHz [2]. Since the typical electrical resistance of high-speed VCSELs is ∼100 Ω due to a smaller oxide-confined aperture (5–7 μm in diameter), the requirement for the RC time constant therefore depends on the parasitic capacitance of the device. Previously developed high-speed VCSELs adopted either an intra-cavity/co-planar metal contact [3] or the polyimide planarization [4] process to reduce parasitic capacitance. Unfortunately, these nonplanar approaches have numerous disadvantages and are inconvenient to mass production [5]. To avoid these unfavourable process techniques, a simple planar approach for high-speed oxide-confined VCSELs fabrication has already been demonstrated [5, 6]. The static operation characteristics and lifetime test of devices demonstrate the fabrication technology adequate to the requirement of mass production. To further improve VCSEL performance, an additional proton implantation procedure was introduced into the process to reduce parasitic capacitance, and an eye diagram

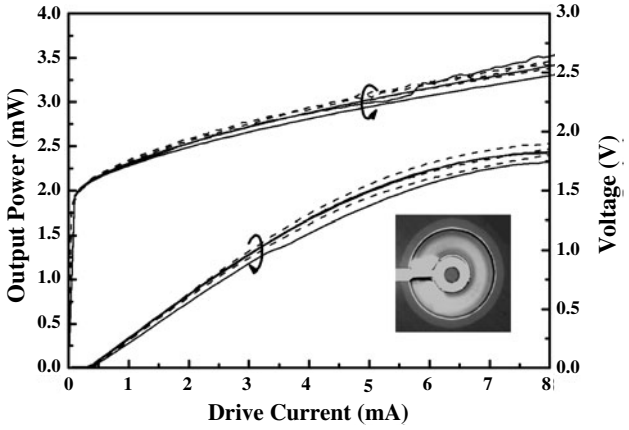

Figure 1. *L–I–V* curves of three oxide-implanted VCSELs (solid lines) and three oxide-only VCSELs (dashed lines).

widened to 10 Gbps was obtained [6]. This work details the proton implantation effect on high-speed VCSELs with planar geometry. A comprehensive small signal measurement and analysis was conducted based on the physical modelling of VCSELs. The analytical results confirm that proton implantation effectively reduces the parasitic capacitance of the oxide-confined VCSELs, improving the high-speed performance.

2. Experimental details

The VCSEL epi-wafers were grown by Aixtron 2400 G3 metal-organic chemical vapour-phase deposition (MOCVD) on n^+-GaAs substrate, the structure of which consists of a three quantum-well GaAs/AlGaAs active layer, sandwiched by fully doped n- and p-DBR mirrors. Both n- and p-DBR are composed of interlaced $1/4\lambda$-thick $Al_{0.15}Ga_{0.85}As$ and $Al_{0.9}Ga_{0.1}As$ layers, with periods of 39.5 and 22, respectively. The oxide-confined VCSEL process procedure has been described elsewhere [5, 6]. The mesa diameter of the fabricated device was 22 μm with a 5 μm oxide aperture, and the device surface was quasi-planar so that the annular p-contact metal and the bond pad were on the same level. The p-contact was created by directly depositing Ti/Pt/Au on the upper heavily doped p^+ GaAs contact layer, and Au/Ge/Ni/Au was deposited on the bottom side of the substrate following thinning down. Notably, the process did not use either the intra-cavity/co-planar metal contact or the polyimide resin planarization technique. Multiple proton implantations with a dose of 10^{15} cm^{-2} and four different proton energy ranges between 300 and 420 keV were adopted according to simulation results of the stopping and range of ions in matter (SRIM). The implantation region was kept away from the mesa to prevent damage to the active region and consequent voiding of triggering reliability issues.

3. Results and discussion

Figure 1 displays the *L–I–V* characteristics of the fabricated VCSELs with (solid lines) and without (dashed lines) proton implantation. The inset in the lower right corner of figure 1 is a top view microphotograph of the emitting area. Notably,

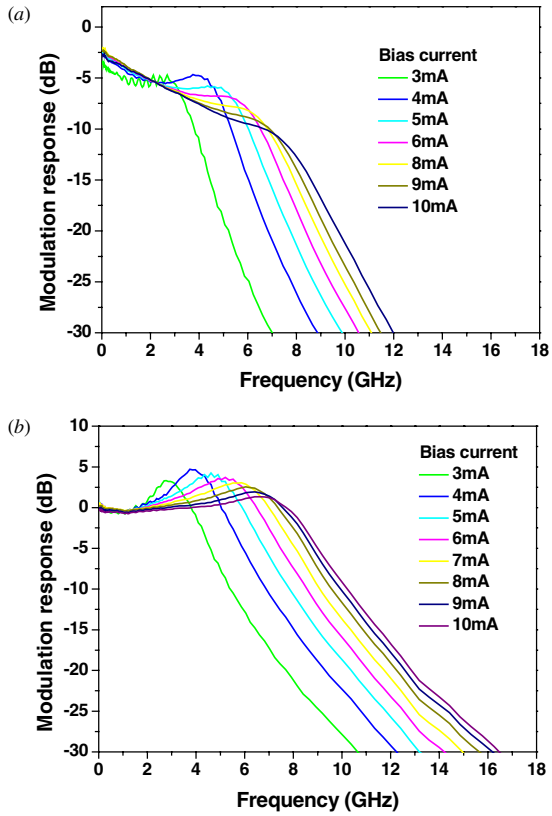

Figure 2. Small signal modulation response of (*a*) oxide-only VCSEL, (*b*) oxide-implanted VCSEL. Curves are listed in the key from left to right.

(This figure is in colour only in the electronic version)

the *L–I–V* curves before and after implantation are very similar. This result differs significantly from a previous investigation [7], because the mesas were entirely protected during implantation in this study and thus no damage was introduced into the active region. Consequently the threshold current can be maintained at the same value, and the dc characteristics are not influenced. The threshold currents of both samples are 0.5 mA and the resistance typically is 90 Ω.

The small signal response of VCSELs as a function of bias current was measured using a calibrated vector network analyser (Agilent 8720ES) with on-wafer probing and a 50 μm multimode optical fibre connected to a New Focus 25 GHz photodetector. The samples then were wire bonded to coplanar transmission lines with an impedance of 50 Ω.

The small signal modulation responses for both oxide-only VCSEL and oxide-implanted VCSEL are shown in figures 2(*a*) and (*b*), respectively. Figure 2(*a*) reveals that the resonance frequency increased with the biasing current as expected. The 3 dB frequency was restricted at ∼2.3 GHz owing to parasitic cut-off. After proton implantation, a parasitic-free modulation response was obtained as shown in figure 2(*b*). Figure 3 plots the resonant frequency and 3 dB frequency as a function of bias current for both oxide-only and oxide-implanted VCSEL. Figure 3 clearly indicates that the resonant frequencies are similar for both oxide-only and oxide-implanted VCSELs. However, although the resonant frequency increases with bias current, the 3 dB frequency is restricted at ∼2.3 GHz for oxide-only VCSEL, while the

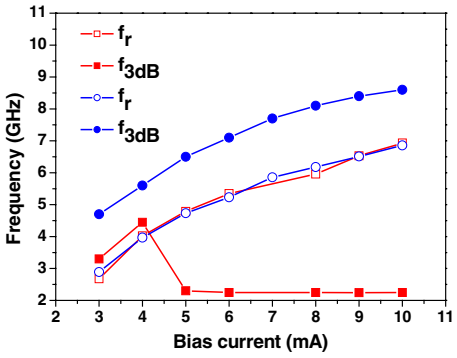

Figure 3. Resonant frequency and 3 dB frequency for oxide-only VCSELs (square symbols) and oxide-implanted VCSELs (circular symbols).

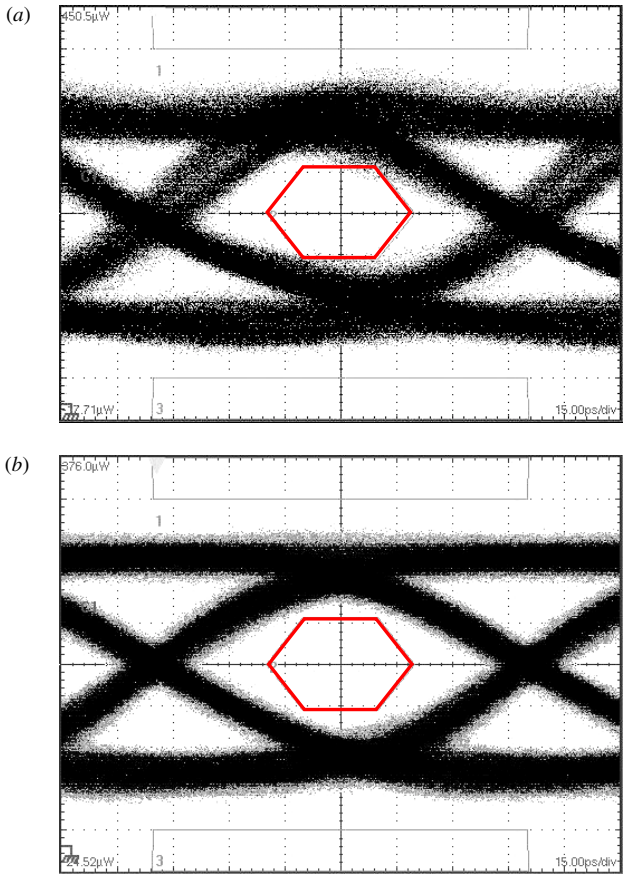

Figure 4. Eye diagram of (*a*) oxide-only VCSEL, (*b*) oxide-implanted VCSEL.

3 dB frequency of oxide-implanted VCSEL increases with bias current throughout the measurement range. These results clearly show that the parasitic components restricted the modulation bandwidth of oxide-only VCSEL, and moreover that the proton implantation successfully removed the parasitic effect. For large signal modulation, bias current and a nonreturn-to-zero (NRZ) pseudorandom bit sequence (PRBS) were combined in a bias-tee and fed to a top-emitting VCSEL which was wire-bonded to an SMA socket. Figure 4 shows eye diagrams modulated at 10 Gbps with 6 mA bias and 6 dB

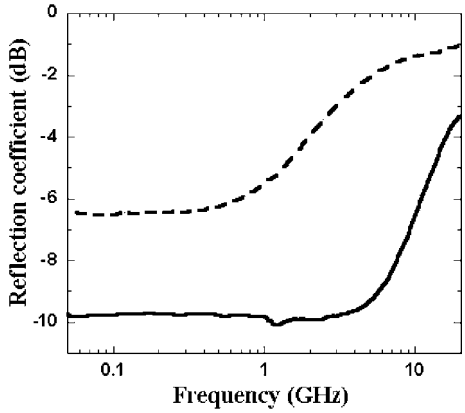

Figure 5. Reflection coefficient (S_{11}) for oxide-only device (dashed line) and oxide-implanted device (solid line) at 3 mA.

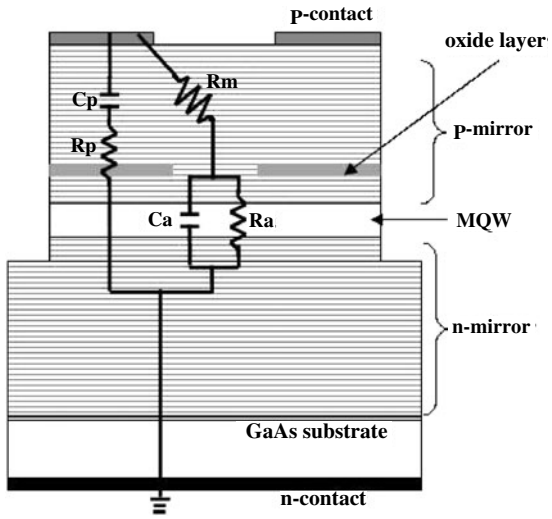

Figure 6. Equivalent circuit used for the oxide confined VCSEL impedance.

extinction ratio for both oxide-only and oxide-implanted VCSELs. For the oxide-only VCSEL, the turn on jitter was about 30 ps, and the fall time tail clearly hit the mask. In contrast, the eye improved significantly after ion implantation, and could pass the 10 Gb s^{-1} mask. The rise time, fall time and jitter of the oxide-implanted device were 44 ps, 54 ps and 20 ps, respectively. To further explore how the ion implantation influenced the electrical parasitic, figure 5 illustrates the reflection coefficient (S_{11}) of the oxide-only VCSEL and oxide-implanted VCSEL. The reflection coefficient curves reveal that more RF power is reflected back from the oxide-only VCSEL and therefore degrades the modulation bandwidth. The electrical bandwidth for oxide-only devices is ∼3 GHz, and exceeds 20 GHz for oxide-implanted devices. This finding again confirms that the proton implantation has successfully reduced the parasitic capacitance. An equivalent circuit model shown in figure 6 was used to extract the circuit components. The resistance R_m represents the mirror loss, while the R_a accounts for the active region resistance. C_a represents a combination of the capacitance of the active area and oxide layer. A shunt

resistance R_p is also included to account for pad loss, and the pad capacitance is represented by C_p. This equivalent circuit can also be applied to examine the extrinsic limitations on the modulation speed and to determine the influence of parasitic capacitance and mirror resistance on the modulation bandwidth. The values of the circuit components were extracted using ADS (Advanced Design System, Agilent) by fitting both the magnitude and the phase of S_{11} over the measured frequency range. Based on a co-optimization at several bias conditions, R_m was around 42 Ω and R_a was found to be bias dependent, varying from 80 to 37 Ω in 1–6 mA. The major difference between oxide-only and oxide-implanted devices was the capacitance C_a and C_p. Moreover, the C_a and C_p of oxide-only devices were 1.8 and 0.4 pF, respectively, while the C_a and C_p of oxide-implanted devices were 0.5 and 0.28 pF, respectively. Therefore, proton implantation is shown to effectively reduce the bond pad capacitance and oxide capacitance.

4. Conclusion

This study describes the high-speed performance of 850 nm oxide-confined VCSELs with a planar process and reduced parasitic capacitance. The high-speed operating characteristics of VCSELs have been improved by performing additional proton implantation without altering the *L–I–V* characteristics. The small signal modulation bandwidth which was restricted by electrical parasitic capacitance expanded from 2.3 GHz to 9 GHz after proton implantation. The reflection coefficient showed that the electrical parasitic pole exceeded 20 GHz. Finally, the eye diagram demonstrated that the devices can be modulated up to 10 Gbps.

Acknowledgments

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References

[1] Aeby I, Collins D, Gibson B, Helms C J, Hou Hong Q, Luo W, Bossert D J and Wang C X 2003 *Proc. SPIE* **4994** 152–61
[2] Yokouchi N, Iwai N and Kasukawa A 2003 *Proc. SPIE* **4994** 189–96
[3] Strijbos R C *et al* 2000 *Proc. SPIE* **3946** 69–77
[4] Mederer F *et al* 2000 *Proc. 50th Electronic Components and Technology Conference* pp 1242–51
[5] Yu H C, Chang S J, Su Y K, Sung C P, Lin Y W, Yang H P, Huang C Y and Wang J M 2004 *Proc. 5th Pacific Rim Conf. Lasers Electro-optics (Taipei, 2003)* p 159
[6] Yu H C, Chang S J, Su Y K, Sung C P, Lin Y W, Yang H P, Huang C Y and Wang J M 2004 *Mater. Sci. Eng.* B **106** 101–4
[7] Choquette K D, Fischer A J, Geib K M, Hadley G R, Allerman A A and Hindi J J 2000 *Semiconductor Laser Conference, Conference Digest* pp 59–60