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Leakage behavior of the quasi-superlattice stack for multilevel charge storage

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The leakage behavior of the quasi-superlattice structure has been characterized by current–voltage measurements at room temperature and 50 K. A resonant tunnelinglike leakage characteristic is observed at low temperature. The resonant tunneling occurs at around 2, 5.2, and 7 V under a gate voltage swept from 0 to 10 V. A concise physical model is proposed to characterize the leakage mechanism of tunneling for the quasi-lattice structure and suggests that the considerations of the operating voltage for the two-bit per cell nonvolatile-memory device need to be taken into account.
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In the age of 1960's, due to the high cost, large volume, and high-power consumption of the magnetic-core memory, the electronic industries urgently needed another memory device to replace the magnetic-core memory. Kahng and Sze developed a floating-gate (FG) nonvolatile semiconductor memory at Bell Labs in 1967.[1] To date, the stacked-gate FG device structure continues to be the most prevailing nonvolatile-memory implementation, and is widely used in both stand alone and embedded memories. The invention of FG memory impacts more than the replacement of magnetic-core memory, and creates an era of portable electronic systems. The most widespread memory array organization is the so-called flash memory, which has a byte-selectable write operation combined with a sector ''flash'' erase.

Although a huge commercial success, conventional FG devices have their limitations. The most prominent one is the limited potential for continued scaling of the device structure. This scaling limitation stems from the extreme requirement put on the tunnel oxide layer. On the one hand, the tunnel oxide has to allow quick and efficient charge transfer to and from the FG. On the other hand, the tunnel oxide needs to provide superior isolation under retention and disturbed conditions in order to maintain information integrity over periods of up to a decade. There is, therefore, a tradeoff between speed and reliability and the thickness of the tunnel oxide is compromised to about 8–11 nm, which is barely reduced over more than five successive generations of the industry.[2] To overcome the scaling limits of the conventional FG structure, two candidates are mostly mentioned, SONOS[3–5] and nanocrystal nonvolatile memory devices.[6–8] As for SONOS, the silicon nitride layer is used as the charge-trapping insulator. The intrinsic distributed storage takes advantage of the SONOS device over the FG device, its improved endurance, since a single defect will not cause the discharge of the memory.[5] Tiwari *et al.*[6] demonstrated the Si nanocrystal FG memory device in the early 1990's. Also, the nanocrystal memory device can maintain good retention characteristics when the tunnel oxide is thinner and the power consumption is lower.[6–8] In our current study, a quasi-superlattice structure has been demonstrated for the two-bit per cell nonvolatile-memory device.[9] Apparent and peculiar memory effects were also observed in our previous results. To achieve further study on the reliability issues, it is essential to understand the leakage mechanism that operates in the quasi-superlattice structure. In the present work, the leakage behavior of the quasi-superlattice stack for multilevel charge storage has been demonstrated. Also, a concise model is proposed to deduce and explain the leakage behavior of the quasi-superlattice stack.

Single-crystal, 6 in. in diameter, (100)-oriented *p* type silicon wafers were used in the present study. The wafers were chemically cleaned by a standard Radio Corporation of America cleaning, followed by a dry oxidation in an atmospheric pressure chemical vapor deposition furnace at 925 °C

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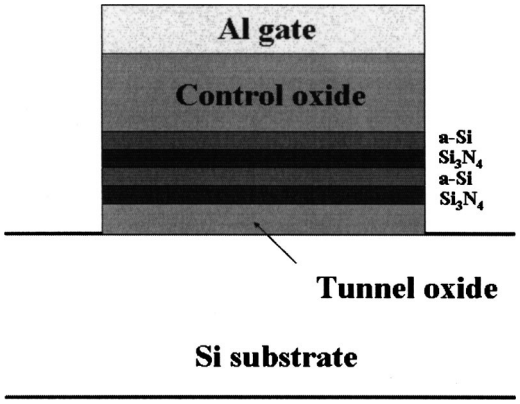

FIG. 1. The cross-sectional image of the quasi-superlattice structure.

to form a 3 nm tunnel oxide. Subsequently, silicon nitride (Si_3N_4) and amorphous Si (a-Si) quasi-superlattice of two periods were deposited by low-pressure chemical vapor deposition (LPCVD) at 780 °C and 550 °C, respectively. Each of the four LPCVD layers was controlled to be about 2 nm. A 10 nm thick tetraethyl orthosilicate (TEOS) oxide was deposited on the quasi-superlattice as the control oxide layer. To densify the control oxide layer, a steam densification was performed at 982 °C.[10] Via the TEOS oxide deposition and steam densification, the two a-Si layers will be crystallized into microcrystal or polycrystal, which depends on the grain size of the Si layers. After the Al electrodes were patterned and sintered, current–voltage ($I-V$) measurements were performed at room temperature and the low temperature of 50 K to investigate the leakage behavior of the quasi-superlattice memory device. The electrical measurements were performed using a semiconductor parameter analyzer, model HP4156, and a low-temperature integrated probing station.

Figure 1 shows the device structure in this work. The quasi-superlattice of Si_3N_4 and a-Si, sandwiched between tunnel oxide and control oxide, is utilized as a charge storage element for a memory device instead of poly-Si FG or Si_3N_4 single layer. To investigate the leakage behavior of the quasi-superlattice stack structure, $I-V$ electrical measurements are performed. Figure 2 exhibits the current density–voltage

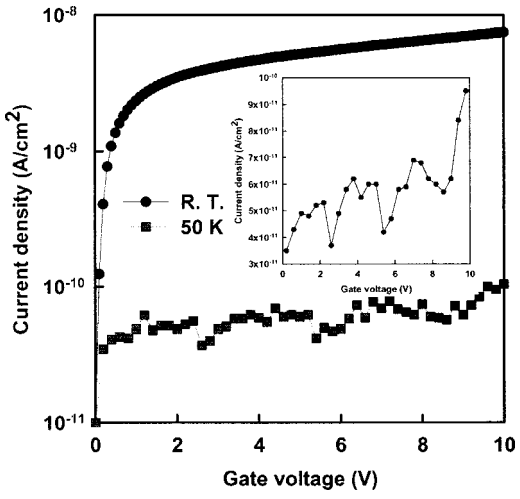

FIG. 2. The $J-V$ characteristics for both room temperature and 50 K. The inset shows the local amplification of the $J-V$ curve at 50 K.

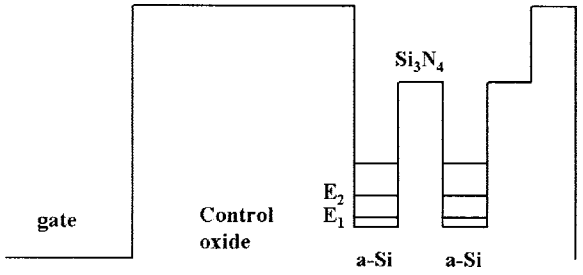

FIG. 3. The ideal energy band diagram of the quasi-superlattice stack under zero bias.

($J-V$) characteristics for both room temperature and 50 K. It is clearly shown the leakage current at 50 K is lower than that at room temperature as a factor of 2 orders due to the alleviation of thermionic emission.[11] The leakage current at room temperature, dominated by thermionic emission and trap-assisted tunneling, remains low when a 10 V gate voltage is applied. Additionally, there is a negative differential resistance observed at different gate biases for the measurements of 50 K. The inset shows the local amplification of the $J-V$ curve at 50 K. The negative differential resistance occurs at around 2, 5.2, and 7 V. It is inferred that the $I-V$ characteristics behave like that of the resonant tunneling diode (RTD) at low temperature.[12–14] To clarify the similarity between RTD and our quasi-superlattice stack of insulators, a model is proposed based on the energy band diagrams of tunneling. Figure 3 shows the ideal energy band diagram of the quasi-superlattice stack under zero bias. The quasi-superlattice of Si_3N_4 and a-Si clearly shows the band offsets that can easily trap electrons as the memory elements. The undoped a-Si layers are with a wider band gap than that of the Si substrate. In the a-Si quantum wells, discrete energy levels, E_1, E_2,..., and E_n, are formed due to quantum confinement effect.[15,16] Consider the resonant tunneling between the two a-Si layers under applied biases. As can be seen in Fig. 4(a), after the electrons tunnel from the channel, it is not easy for the electrons to surmount the energy barriers of

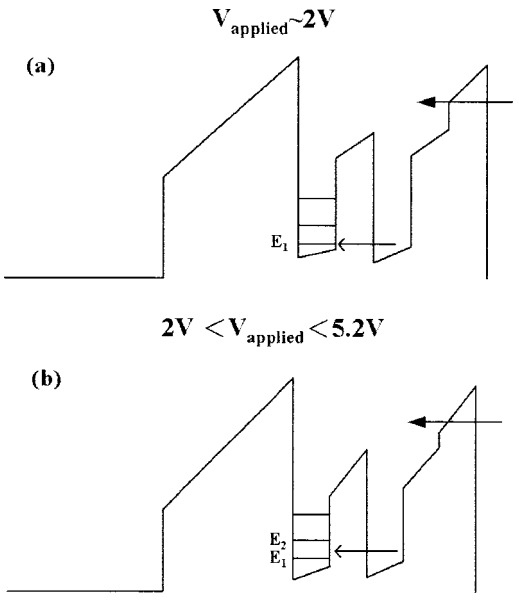

FIG. 4. (a) The energy band diagram of resonant tunneling at around 2 V between the two a-Si layers (b) the band diagram for 2 V < applied gate voltage <5.2 V.

nitride and control oxide at 50 K. Therefore, tunneling effects dominate the leakage mechanism. As the applied voltage is around 2 V, a resonant tunneling of E_1 occurs between the two a-Si quantum wells. The first resonant tunneling contributes the peak current density at 2 V as shown in the inset of Fig. 2. As the voltage is applied between 2 and 5.2 V, there is no energy level in the a-Si quantum well through which the electrons to resonantly tunnel. A sudden decrease of the leakage current occurs, followed by the gradual increase of the leakage current, and the second resonant tunneling of E_2 is reached at around 5.2 V. The peak current density at 7 V in Fig. 2 is inferred to be the resonant tunneling of E_3 between the two a-Si quantum wells. As shown in Fig. 4, the current conduction between the two a-Si quantum wells is dominated by the resonant-tunneling model. For the conduction of the current through tunnel oxide, silicon nitride, and control oxide, the conduction mechanism is dominated by direct tunneling, Fowler–Nordheim (F–N) tunneling, or trap-assisted tunneling.[17] Due to the thinness of the tunnel oxide and nitride layers, the probability of the occurrence of direct tunneling and trap-assisted tunneling is larger than that of F–N tunneling. As for the current conduction of the control oxide, F–N tunneling and trap-assisted tunneling are the main mechanisms dominated. The investigation of the leakage mechanism of the quasi-superlattice stack will help the multilevel charge storage develop the considerations of operating voltage for the two-bit per cell nonvolatile-memory device.

In summary, the study on the leakage behavior of the quasi-superlattice stack has been demonstrated for room temperature and 50 K. The $I-V$ characteristics of the quasi-superlattice structure behave like that of the RTD at a low temperature. The negative differential resistance occurs at around 2, 5.2, and 7 V. Also, a concise model is proposed to understand the leakage behavior of the quasi-superlattice stack.

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