An Endurance Evaluation Method for Flash EEPROM

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***Abstract*—Trap generation is hard to estimate in a Flash cell due to a dynamic stress field during program and erase. In this paper, a linear correlation is found between the erase state V_T rollup and cycling V_T window. With the knowledge of the time dependence of erase stress field based on Fowler–Nordheim (FN) tunneling, the V_T rollup during cycling is evaluated by incorporating field dependent oxide trap generation. The extracted ΔV_T degradation slope during constant FN stress can be applied quantitatively to predict the V_T window closure during Flash cell cycling.**

***Index Terms*—Dynamic stress, evaluation method, Flash EEPROM, tunnel oxide.**

I. Introduction

HIGH-FIELD stressing during program/erase (P/E) cycling in Flash EEPROM operation can lead to a significant increase of trap generation in tunnel oxide. Such trap generation has important impacts on endurance and data retention of a Flash memory cell. For example, these traps can serve as an intermediate state during tunneling and cause stress-induced leakage current [1]. To realize highly reliable Flash EEPROMs, comprehensive understanding of cell characteristics degradation during P/E cycling is essential. Trap generation during stress has been widely studied in MOSFETs and many trap generation models were proposed [2], [3]. However, these models, which are based on constant current stress or constant voltage stress conditions, cannot be directly applied to a Flash device, where both oxide field and gate current change with program or erase time. In addition, the modeling of degradation during P/E cycling is complicated [4]. By utilizing a steady-state stress-induced leakage current (SILC) model and an empirical formula to describe the relationship between stress current and neutral trap density, a quantitative model is developed that allows a prediction of the SILC-related disturb behavior of tunnel-oxide devices after P/E cycling [5]. In this work, we will focus on the modeling of the V_T window degradation due to cycling-caused trap creation. Both Flash device and dummy cell are characterized to investigate V_T window degradation under various stress conditions. The dummy cell is fabricated by the same process as a Flash cell except for connected floating gate and control gate.

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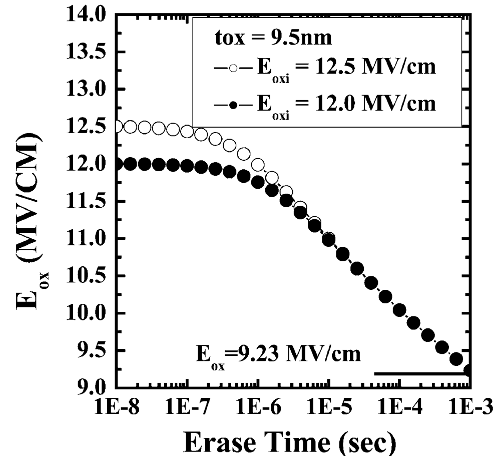

Fig. 1. Time evolution of erase E_{ox} is plotted with $E_{\mathrm{oxi}} = 12.5$ and 12.0 MV/cm for $t_{\mathrm{ox}} = 9.5$ nm. The convergence behavior is clearly observed as $t > 5 \times 10^{-6}$ s. The erase field at the end of erase operation is similar in the two cases, which is about 9.233 MV/cm.

By using a Fowler–Nordheim (FN) tunneling equation and a universal field dependent trap creation model, the evolution of oxide degradation during P/E cycling as a function of erase condition is established. Finally, this method has been verified with respect to cycling number dependence, cycling window dependence, and process dependence.

II. Modeling of Erase V_T Rollup

A. Analytical Expression for Erase Characteristic

A channel hot electron (CHE) program and FN erase scheme is adopted in this study. As reported by Suhail *et al.*, the CHE stress will cause less damage than FN tunneling stress [6]. Therefore, in calculation, we only consider the damage induced by FN erase. During erase, the electric field in tunnel oxide will change with time, and an expression for the $E_{\mathrm{ox}}(\mathrm{t})$ with initial erase field E_{oxi} can be expressed as [7]

$$E_{\mathrm{ox}}(t) = \frac{B}{\ln\left[\frac{kBtA_{\mathrm{ox}}}{C_{\mathrm{total}}t_{\mathrm{ox}}} + \exp\left(\frac{B}{E_{\mathrm{oxi}}}\right)\right]} \tag{1}$$

where $k = 2.0 \times 10^{-6}$ Amp/V^2, $B = 238.5$ MV/cm [8], C_{total} is the sum of the capacitances of the cell, t_{ox} is the thickness of tunnel dielectric, E_{oxi} stands for an initial electric field, and A_{ox} represents the tunnel area. In Fig. 1, the time evolution of erase E_{ox} is plotted for $t_{\mathrm{ox}} = 9.5$ nm. Two curves start to converge after $t = 5 \times 10^{-6}$ s , and reach about the same final $E_{\mathrm{ox}} = 9.23$ MV/cm at $t = 1$ ms. From (1), we know that this convergence behavior holds for $(kBtA_{\mathrm{ox}}/C_{\mathrm{total}}t_{\mathrm{ox}}) \gg \exp(B/E_{\mathrm{oxi}})$.

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B. Charge Generation During ac Stress

This simulated result shows that the $E_{\rm ox}$ is still high at the end of the erase operation. In such a high field region, both E and 1/E oxide breakdown models suggest a field-dependent trap generation rate [9]. According to published data, the degradation is 10^{γ} times worse for each 1 MV/cm increment of $E_{\rm ox}$ and the field acceleration factor γ is usually in the range of 0.7–1.1 [9], [10]. By applying a constant current stress with CHE filling in dummy cells, γ can be extracted, as shown in Fig. 2. Before the trap generation saturates, a linear correlation is observed in Fig. 2 in a $\log(\Delta V_T) - E_{\rm ox}$ plot. The extracted γ value (0.96) is in agreement with those reported in [9] and [10]. The CHE filling conditions are $V_D = 3.5$ V and $V_G = 6$ V for 100 s. As illustrated in Fig. 3, after subsequent CHE filling, no noticeable difference is observed for a fresh cell, but the threshold voltage is greatly increased for a stressed device. In other words, the CHE filling can increase the trapped electron density after stress [11] but will not damage the oxide. Since the erase time is 1 ms, the ΔV_T for 1–M cycling under constant $E_{\rm ox} = 9.23$ MV/cm is then estimated to be ΔV_T (9.23 MV/cm)$/\alpha = 0.243/0.65 = 0.374$ V from Fig. 2. Typically, the increased rate of ΔV_T under a constant stress field E_0 should follow a power law dependence on stress time and can be described as [12]

$$\Delta V_t(E_o) = A(E_o)t^n \tag{2}$$

where $A(E_o)$ is the degradation factor, and *t* represents a cumulative stress time under the same field. For a different $E_{\rm ox}$, since the relationship between $A(E_o)$ and $A(E_{\rm ox})$ is known, the damage induced by a different stress field $E_{\rm ox}$ at time *t* can be transformed to that induced by a same field E_0 via the following expression:

$$\begin{aligned}\Delta V_t(E_{\rm ox}) &= A(E_{\rm ox})\cdot t^n = 10^{\gamma(E_{\rm ox}-E_0)}A(E_0)t^n\\ &= A(E_0)\left[10^{\frac{\gamma(E_{\rm ox}-E_0)}{n}}t\right]^n.\end{aligned} \tag{3}$$

Similarly, if $E_{\rm ox}$ is time varying, $\Delta V_T(E_{\rm ox}(\mathrm{t}))$ can be approximated by a summation of numerous ΔV_Ts of small time interval, $\Delta\mathrm{t}$, within which $E_{\rm ox}$ can be assumed to be constant

$$\begin{aligned}\Delta V_t(AC)|_0^{t_{\rm erase}} &= A(E_0)\left[\sum_{i=1}^{\infty}10^{\frac{\gamma(E_i-E_0)}{n}}\Delta t\right]^n\\ &= A(E_0)\left[\int_0^{t_{\rm erase}}10^{\frac{\gamma(E_{\rm ox}(t)-E_0)}{n}}dt\right]^n.\end{aligned} \tag{4}$$

As a demonstration of the above time transformation, an experiment of ΔV_T under a staircase stress field is carried out. In Fig. 4, the ΔV_T under stress is plotted against the step number. The solid circles denote the measurement data and the open ones are the calculated result with $n = 0.5$. The power factor *n* can be extracted from Fig. 2. The calculated result reasonably matches the measurement result, which shows the validity of (4).

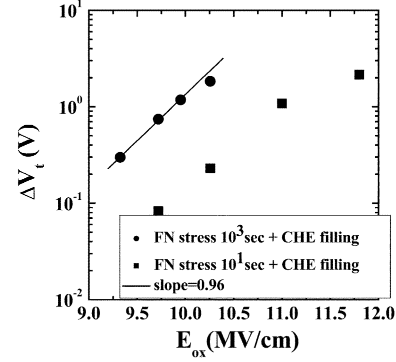

Fig. 2. ΔV_T under constant current stress is plotted against $E_{\rm ox}$ on a semilog scale. The CHE filling conditions are $V_D = 3.5$ V and $V_G = 6$ V for 100 s. The extracted γ value is about 0.96.

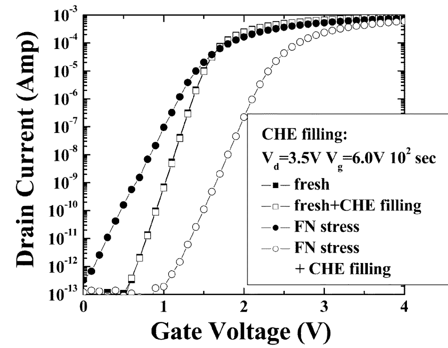

Fig. 3. With applying subsequent CHE filling, no noticeable difference is observed for a fresh cell, but the threshold voltage is greatly increased for a stressed device.

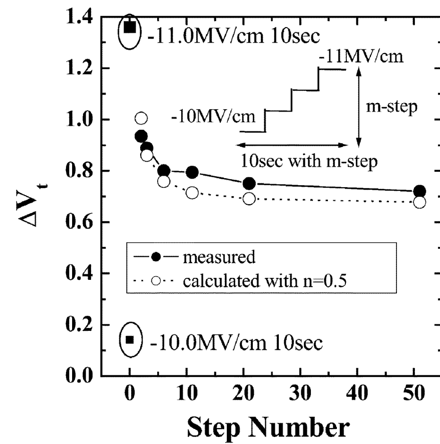

Fig. 4. ΔV_T under a staircase stress field is plotted against the step number. The total stress time is fixed at 10 s. The solid circles denote the measurement data, and the open ones are the calculated result with $n = 0.5$. The power factor n can be extracted from Fig. 2.

C. Erase V_T Rollup During P/E Cycling

Along with electron trapping in the tunnel oxide during cycling, the erase V_T rolls up and the maximum erase field $(E_{\max})$ will reduce. The $E_{\max}$ at each cycle can be expressed as

$$E_{\max} = E_{\rm oxi} - A(E_0)[\text{cumulative_stress_time@}E_0]^n/t_{\rm ox}. \tag{5}$$

Now, the endurance characteristic of a Flash cell can be evaluated by a self-consistent calculation of (1), (4), and (5). In the

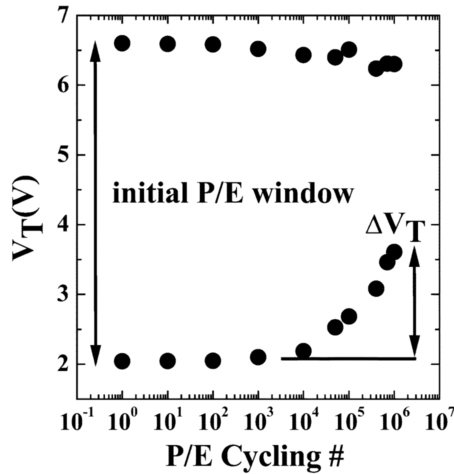

Fig. 5. Endurance characteristic of the Flash cell during P/E cycling is plotted. The device is programmed under $V_D = 5$ V and $V_G = 10$ V for 1 μs and is erased with $V_S = V_D = V_B = 8$ V and $V_G = -8$ V for 1 ms. The definition of initial P/E window and ΔV_T is also denoted.

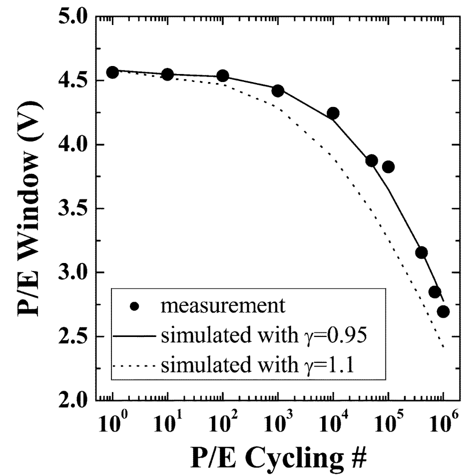

Fig. 6. Window closure effect is simulated with $\gamma = 0.95$ and $\gamma = 1.1$. The calculated result well fits the measurement data.

beginning, the $E_{\max}$ is equal to $E_{\rm oxi}$. After the $E_{\max}$ is obtained, the time evolution of oxide field can be simulated by utilizing (1), and then, the stress damage induced by $E_{\rm ox}(\rm t)$ can be calculated using an equivalent stress time at constant field E_o via (4). Finally, the $E_{\max}$ for next cycle can be determined. The above procedure is repeated until the prescribed cycle number is reached.

III. Experimental Results

The test device has a gate length of 0.3 μm and a gate area of 0.09 μm^2. The typical endurance characteristic of a Flash cell during P/E cycling is shown in Fig. 5. The Flash device is programmed by CHE injection at $V_{\rm ds} = 5$ V and $V_{\rm gs} = 10$ V for 1 μs and erased by FN injection at $V_D = V_S = V_B = 8$ V and $V_G = -8$ V for 1 ms. As shown in the figure, the dominant endurance characteristic of the cell is the collapse of the threshold window with increasing P/E cycles. Here, ΔV_T denotes the shift of erase V_T after 1 M cycling. We replot the cycling number evolution of the P/E window in Fig. 6 and the simulated results with $\gamma = 0.95$ and $\gamma = 1.1$ are shown for comparison. The calculated one fits well with the measurement data when $\gamma = 0.95$. In Fig. 7, the ΔV_T is plotted against its initial P/E window. Three erase gate biases of $V_G = -7, -8$, and -9 V are used to achieve a different range of cycling window. A linear correlation is observed in the figure. The slope is about 0.0926 on a semilog scale. For a given erase bias, the initial P/E window has a spread about 0.4 V. The explanation will be given later. As shown in the figure, regardless of erase bias, a similar trend of degradation is found under a same operation window. This implies that the rollup of ΔV_T is strongly related to the charge flow or $E_{\rm ox}$ but slightly depends on the oxide thickness. The calculated ΔV_T is also plotted against the initial P/E window on a semilog scale in Fig. 7 with $\gamma = 0.95$ cm/MV and $\gamma = 1.1$ cm/MV and the simulated degradation slope is consistent with the measurement result.

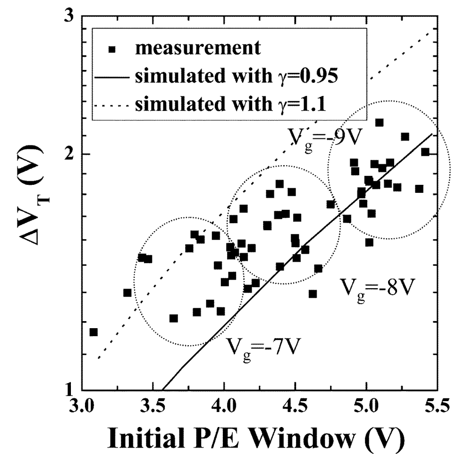

Fig. 7. ΔV_T is plotted against its initial P/E window. A linear correlation is observed. The simulated curves with two different field acceleration factors ($\gamma = 0.95$ and $\gamma = 1.1$) are also shown for comparison.

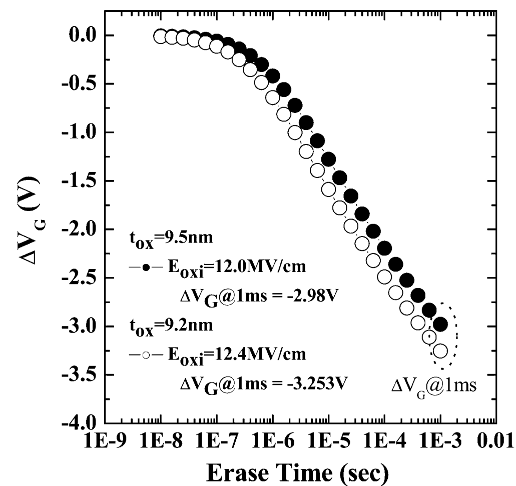

Fig. 8. Simulated erase characteristics for $t_{\rm ox} = 9.5$ nm with $E_{\rm oxi} = 12.0$ MV/cm and $t_{\rm ox} = 9.2$ nm with $E_{\rm oxi} = 12.4$ MV/cm. The changes of the threshold voltage on the tunnel oxide (ΔV_G) after 1-ms erase is also shown in the figure.

In Fig. 8, simulated erase characteristics for $t_{\rm ox} = 9.5$ nm with $E_{\rm oxi} = 12.0$ MV/cm and $t_{\rm ox} = 9.2$ nm with $E_{\rm oxi} =$ 12.4 MV/cm are shown. Note that the two curves have a same initial voltage at the floating gate although the tunnel oxide

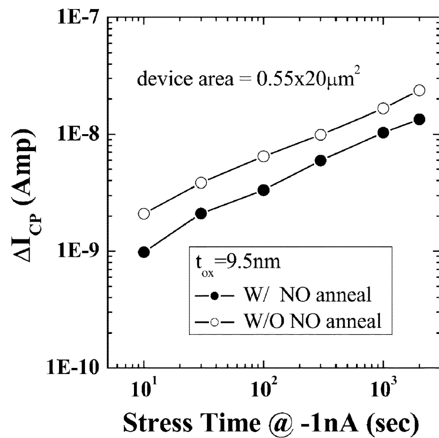

Fig. 9. Time evolution of the charge pumping current is recorded for the samples with and without NO anneal. Although the degradation rate is the same, the $\Delta I_{\rm cp}$ of a NO annealed sample is about half of that without NO anneal.

thickness is different. The change of the threshold voltage on the tunnel oxide (ΔV_G) after 1 ms erase is also denoted in the figure. It should be noted that a 0.3-nm variation on oxide thickness is not unusual due to process variation and this thickness variation can be monitored via the change of gate current in FN tunneling region. From the simulation, we know that even this small variation will induce about a 0.3-V V_T difference in the floating gate if the same initial erase voltage is applied to the floating gate. Since the gate coupling ratio [$\alpha = C_{\rm ono}/C_{\rm total}$, typically 0.65 for an EPROM tunnel oxide (ETOX) structure] is nearly the same for this two cases, the thickness difference here thus represents a $0.3{\rm V}/0.65 = 0.46$ V variation of P/E window under a fixed operation bias. The $C_{\rm ono}$ is the total capacitance between the control gate and the floating gate. This explains why the ΔV_T degradation fluctuates under a constant erase bias, as shown in Fig. 7.

IV. Process-Dependence

The continuous shrinkage of Flash device dimensions requires highly reliable tunnel dielectric films. The nitrided oxide is a promising candidate for such films due to its excellent immunity to electric stress, such as suppression of SILC [13]. In our experiments, the nitrogen is incorporated into the oxide via NO anneal. In Fig. 9, the charge pumping current is measured on a MOSFET with $L/W = 0.55$ μm/20 μm and $t_{\rm ox} = 9.5$ nm. Constant current stress (CCS) at $I_G = -1 \times 10^{-9}$ A is chosen here to emulate the same cycling windows during operation. Although the degradation rate is the same, the $\Delta {\rm I}_{\rm cp}$ of a NO annealed sample is about half of that without NO anneal. Assuming other parameters are the same for the two cases, the calculated ΔV_T of a NO annealed sample is plotted against the initial P/E window in Fig. 10 with $\gamma = 0.95$ cm/MV and $\gamma = 1.1$ cm/MV. The measurement data is also shown for comparison. The calculated result reasonably reflects the measurement, which proves the validity of our methodology during process evaluation. In other words, the measurement data collected in the process development stage can be correlated to the cell data.

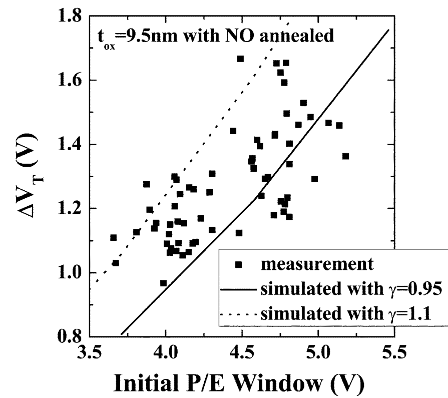

Fig. 10. According to the result of Fig. 9, the ΔV_T in a NO annealed sample is successfully emulated. This proves the predictability of our methodology.

V. Conclusion

A linear correlation has been found between the initial P/E window and the erase V_T rollup after cycling. A physical explanation has been given. In addition, the validity of this methodology during process evaluation has been proven. Since the oxide damage depends on the oxide field, a multiple erase bias scheme with a reduced maximum field may be a better choice. Our findings are important in evaluating the tunnel oxide quality and optimizing the erase waveform.

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From 1978 to 1983, he was an Associate Professor and was promoted to Full Professor at the National Chiao-Tung University, Hsinchu, Taiwan. In 1983, he was with North Carolina State University, Raleigh, as a Visiting Associate Professor and Adjunct Research Staff Member of the Microelectronic Center of North Carolina (MCNC), Research Triangle Park. In 1984, he joined AT&T Bell Laboratories, where he was engaged in very-high-voltage bipolar-CMOS-DMOS (BCDMOS) IC technology for telecommunication applications, CMOS DRAM technology, laser programmable redundancy, and submicron CMOS ULSI technology. He joined the Electronics Research and Service Organization, Industrial Technology Research Institute, Hsinchu, (ERSO/ITRI) in late 1989 as a Deputy General Director responsible for semiconductor and integrated circuit operation, especially the Grand Submicron Project. This project later successfully developed Taiwan's first 8-in CMOS submicron manufacturing technology with high-density DRAM/SRAM as technology vehicles. In late 1994, he was the cofounder of Vanguard International Semiconductor Corporation, Hsinchu, which is a spinoff memory IC Company from ITRIs Submicron Project. He was the Vice President of Operations, Vice President of Research and Development, and later President from 1994 to 1999. He brought Vanguard from a research and development laboratory to a U.S. $400 million sales company and went IPO in 1998. He is currently Chairman and CEO of Ardentec Corporation, Hsinchu, a VLSI testing service company, and also serves Macronix International Company (MXIC), Ltd., Hsinchu, as a Senior Vice President/CTO. He led MXIC's technology development team to successfully achieve the state-of-the-art nonvolatile memory technology and embedded SoC technology; now, MXIC is the top nonvolatile semiconductor company in Taiwan. He has published more than 100 technical papers and has been granted 123 international patents. He also authored more than 30 articles in science education and R&D policy in magazines and newspapers. He served as the President of *Science Monthly* from 1978 to 1983.

Dr. Lu was the Executive Secretary and Managing Director of the Board and Board Director since 1998 for the Physical Society of the R.O.C. from 1981 to 1984. He has been Vice-Chairman and then Chairman of IEEE Electron Devices Society, Taipei Chapter, from 1991 to 1996, and Board Director and Supervisor of IEEE Section since 1996. He is a member of many honor societies, including Sigma Pi Sigma, Phi Tau Phi, and Phi Lambda. He is a life member of the American Physical Society, the Physical Society of the R.O.C., the Chinese Institute of Engineers, and CIE-USA. He received the National Science and Technology Achievement Award from the Prime Minister of Taiwan, R.O.C., in 1994. In 1995, he was awarded the National Invention Award, and in 2002, he was awarded the most prestigious semiconductor award in Taiwan—the Pan Wen Yuan Award.