A CMOS 6-Bit 16-GS/s Time-Interleaved ADC with Digital Background Calibration

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Abstract

An 8-channel 6-bit 16-GS/s time-interleaved ADC was fabricated using a 65nm CMOS technology. Each A/D channel is a flash ADC using latch-type comparator with background offset calibration. Timing skews among the channels are also continuously calibrated in the background. The chip achieves 42.3dB SFDR and 30.8dB SNDR at 16 GS/s sampling rate.

Introduction

In high-speed time-interleaved ADC designs, power consumption and timing skew are two major concerns. We use digital calibration to mitigate the above issues. The reported ADC demonstrates our proposed calibration techniques, which are realized on the chip and continuously operate in the background.

The ADC block diagram is shown in Figure 1. It consists of 8 time-interleaved identical A/D channels, ADC_1 to ADC_8. The A/D channels are driven respectively by 8 different clocks with equally-spaced phases, ϕ_1 to ϕ_8. The clocks are generated from an on-chip delay-locked loop (DLL). The ADC analog input is s(t). It is sequentially sampled and digitized by each A/D channel to produce a 6-bit digital stream. The clock frequency is f_{ref}. The digital streams from the 8 A/D channels, $s_1[k]$ to $s_8[k]$, are then multiplexed to generate the final ADC digital output, s[l]. The ADC equivalent sampling rate is $8xf_{ref}$.

Circuit Description

For a time-interleaved ADC, it is imperative to minimize the mismatches among sampling intervals. In a high-speed design, the sampling intervals are sensitive to mismatches among clock drivers and clock routes. In Figure 1, the delays of the clock drivers, B_1 to B_8, can be independently adjusted by the digital control signals, $T_1[k]$ to $T_8[k]$. The resolution for the delay control is 0.4 psec. The control signals are generated from an on-chip timing-skew calibration processor (TSCP). An on-chip oscillator generates a testing signal x(t). It is sampled and quantized in each A/D channel to produce 8 1-bit digital streams, $c_1[k]$ to $c_8[k]$. From those digital streams, the TSCP continuously counts the zero-crossing (ZC) occurrences in every sampling interval [1]. Each ZC count is proportional to its corresponding sampling interval. The TSCP uses the ZC counts to detect the timing skews, and then automatically adjusts the delays of the clock drivers to ensure uniform sampling intervals.

In each A/D channel, the x(t) signal path consists of only a replica sampler and a comparator, and is separated from the s(t) signal path. Thus, the timing-skew calibration can continuously operate in the background. The proposed ZC detection technique is insensitive to comparator offsets, and does not require the x(t) signal having an accurate frequency or a specific waveform shape. The x(t) generator is a simple ring oscillator free running at 400MHz. To reduce power dissipation, the TSCP operates at 1/64 of the f_{ref} frequency.

Each A/D channel is a flash ADC consisting of 63 background-calibrated comparators (BCC) [2]. Preceding the comparators is a p-channel MOSFET that functions as a sample-and-hold for the ADC. Figure 2 shows the BCC block diagram. It consists of a random-chopping latch (RCL) and a digital calibration processor (CP). In the RCL, two choppers CHP1 and CHP2 are used to invert the polarity of the input-referred offset voltage $V_{OS}[k]$ according to a pseudo-random sequence q[k]. This random chopping introduces offset information into RCL output codes $D_c[k]$. $D_c[k]$ is the input of the thermometer-code edge detector and $D_e[k]$ is the corresponding output. CP then detects the offset polarity by accumulating the correlation of q[k] and $D_e[k]$. A digital control signal T[k], which is continuously updated according to the CP detection, is used to adjust $V_{OS}[k]$. Hence $V_{OS}[k]$ is automatically trimmed to a minimum in the background.

The comparator signal amplification is provided by a cascade of 3 pipelined latches. Figure 3 shows the schematic of the first latch. A coarse and a fine offset adjustment are achieved by varying the pulling strength and the capacitive load on nodes V_{a1} and V_{a2}[3]. Both the second and the third latches have a circuit structure similar to Figure 3 except that they have only one input port and no offset-adjusting circuits.

Measurement Results

The ADC chip was fabricated using 65 nm CMOS technology. Figure 4 shows its micrograph. The active area is $0.93x1.58mm^2$. The supply voltage is 1.5V. Operating at f_{ref}=2GHz, i.e., 16GS/s equivalent sampling rate, the ADC consumes 435mW of power, excluding I/O. Each A/D channel consumes 54mW. The ADC chip is mounted directly on a circuit board. The ADC input capacitance is 1.8pF. The original ADC digital outputs are down-sampled to 1/64.125 of f_{ref} frequency when delivered off-chip.

Figure 5 shows the measured DNL and INL for a single channel ADC. Before activating the calibration, the DNL is -1.0/+4.9 LSB and the INL is -4.3/+5.4 LSB. There are missing codes. After activating the offset calibration, the DNL becomes -0.5/+0.6 LSB and the INL is reduced to -0.4/+0.7 LSB.

Figure 6 shows the measure SNDR versus input frequency for the time-interleaved ADC. The sampling rate is 16GS/s. The effective resolution bandwidth (ERBW) is 3GHz, which is limited by the bandwidth of the sample-and-hold switches. At the frequency near ERBW, the SNDR is improved from 19.8dB to 28.0dB by the timing skew calibration. The figure-of-merit (FOM), defined as power/(2^{ENOB}*2*ERBW) for this ADC is 2.6pJ/conversion-step. If the sampling rate is reduced to 12GS/s, with ERBW=3GHz, the ADC FOM becomes 2.0pJ/conversion-step.

Acknowledgements

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References

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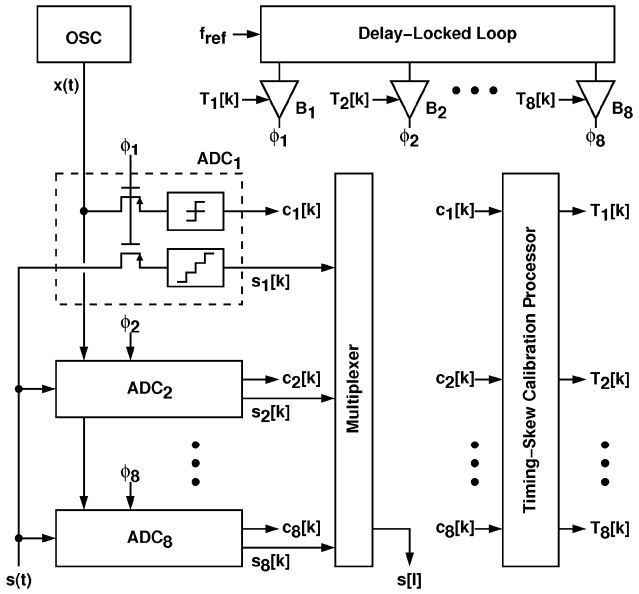

Figure 1: ADC block diagram

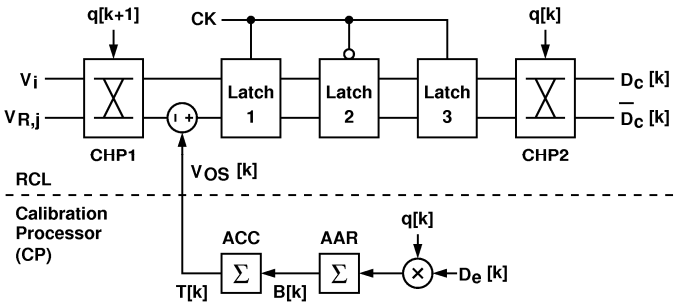

Figure 2: Background-calibrated comparator (BCC)

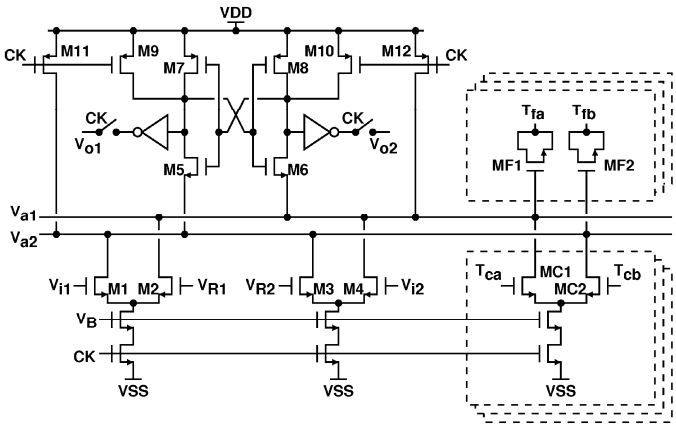

Figure 3: Latch schematic

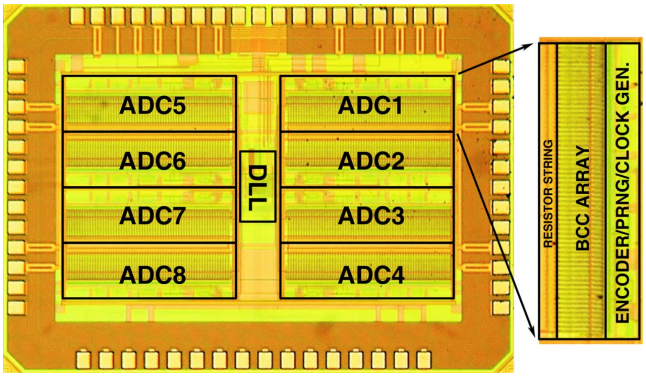

Figure 4: ADC micrograph

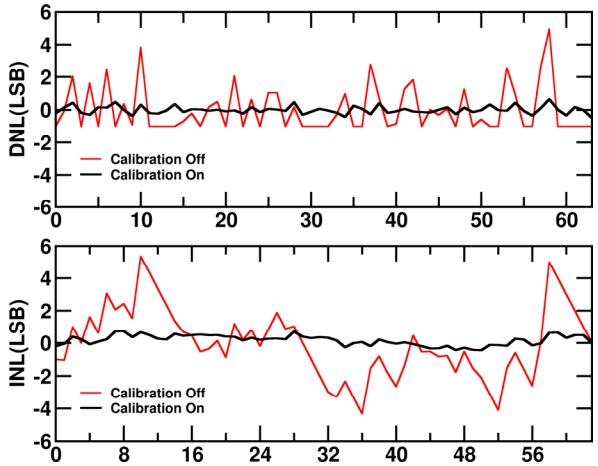

Figure 5: Measured DNL and INL of a single A/D channel.

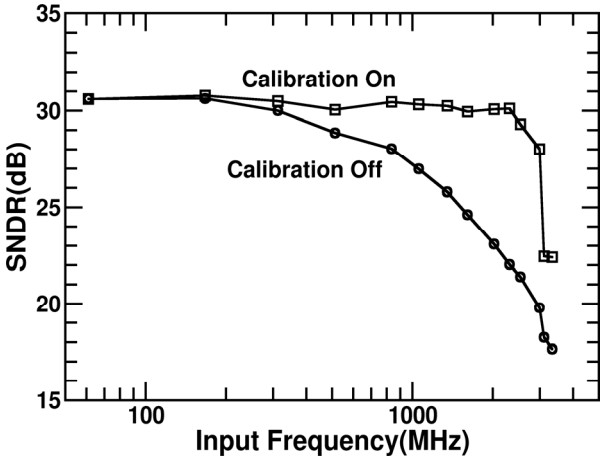

Figure 6: Measured SNDR. The equivalent sampling rate is 16GS/s