

Sidewall roughness control in advanced silicon etch process

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Abstract In ICP-RIE process, there have been many investigations on etching rate. However, only few published reports mentioned the sidewall roughness, which is a critical issue for optical devices. Here, experimental investigations about fabrication parameters in the STS advanced silicon etch (ASE) process for sidewall roughness are performed. In our experiments, several parameters in the ASE process like over time, ramping time, Ar flow rate, platen power, and etching cycle time have been systematically studied. It is found that sidewall mean roughness can be down to 9.11 nm at etching rate of 2.5 $\mu\text{m}/\text{min}$. Comparing with other published works at similar sidewall roughness (around 10 nm), our experimental data have the highest silicon etching rate. For the same STS ICP-RIE systems, our data have smallest sidewall roughness, comparing to previous data published in the literature.

1 Introduction

Dry etching technology is essential for the fabrication of microelectro-mechanical systems (MEMS) devices. In order to satisfy the goals of high etching rate and high aspect ratio, high density plasma systems like electron cyclotron resonance (ECR), helical resonator, and inductively coupled plasma (ICP) were developed for the demanding requirements in the MEMS applications. There are three major issues in the dry etching process: etching rate, silicon profile control, and sidewall roughness.

The silicon profile control was first demonstrated by Jansen et al. (1995). The proposed procedure is called the black silicon method, which uses the fact that the silicon is turned black when the vertical wall recipe is found. For high etching rate development, the advanced silicon etch (ASE) process invented by Lärmer and Schilp (1996) provides the alternative etching, and passivation steps. By using the STS ASE process, several experiment works were reported to improve silicon etching rate, and silicon etching rate to 7 $\mu\text{m}/\text{min}$ has been achieved (Asharf et al. 1998; Bhardwaj et al. 1997; Hynes et al. 1999). Although there have been many investigations on high etching rate and vertical profile, only few published reports mentioned the sidewall roughness (Chabloz et al. 2000; Hynes et al. 1999).

Sidewall roughness is a critical issue for optical devices. Parameter study of ramping control was performed by Hynes et al. (1999), and the sidewall roughness could be down to 40 nm and etching rate 1.7 $\mu\text{m}/\text{min}$. Chabloz et al. (2000) proposed a 3-step high-aspect-ratio silicon etching process to use the Plasma-Therm Shuttle Lock etch tool. The sidewall roughness along the entire etching depth was around 8 nm, and the silicon etch rate was about 1.4 $\mu\text{m}/\text{min}$.

Here, experimental investigations about fabrication parameters to improve sidewall roughness are performed in a STS ICP-RIE system. Several parameters in the ASE process like over time, ramping time, Ar flow rate, platen power, and etching cycle time are experimentally studied.

2 System description

The ASE process here is carried out in a surface technology system (STS) (Bhardwaj and Ashraf 1995) multiplex inductively coupled plasma system. In the STS multiplex inductively coupled plasma system, the source plasma is

Received: 2 September 2002 / Accepted: 1 November 2002

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The support from National Science Council of the Republic of China under grant number NSC89-2218E009-111 is acknowledged. Authors would like to thank the technical support from Precision Instrument Development Center of National Science Council, and Semiconductor Research Center of National Chiao Tung University. We especially thank Mr. Nien-Nan Chu and Mr. Sy-Hann Chen for their technical assistance in SEM and AFM.

Table 1. Typical results of the STS ASE process with standard recipe

Parameter	Value	Parameter	Value
Etch rate	1.3- $\mu\text{m}/\text{min}$	Selectivity to resist	50–100:1
Selectivity to SiO_2	120–200:1	Sidewall profile	$90^\circ \pm 2^\circ$
Aspect ratio	Up to 30	Feature size	1–500 μm
Etch depth capability	500 μm	Sidewall roughness	100–150 nm

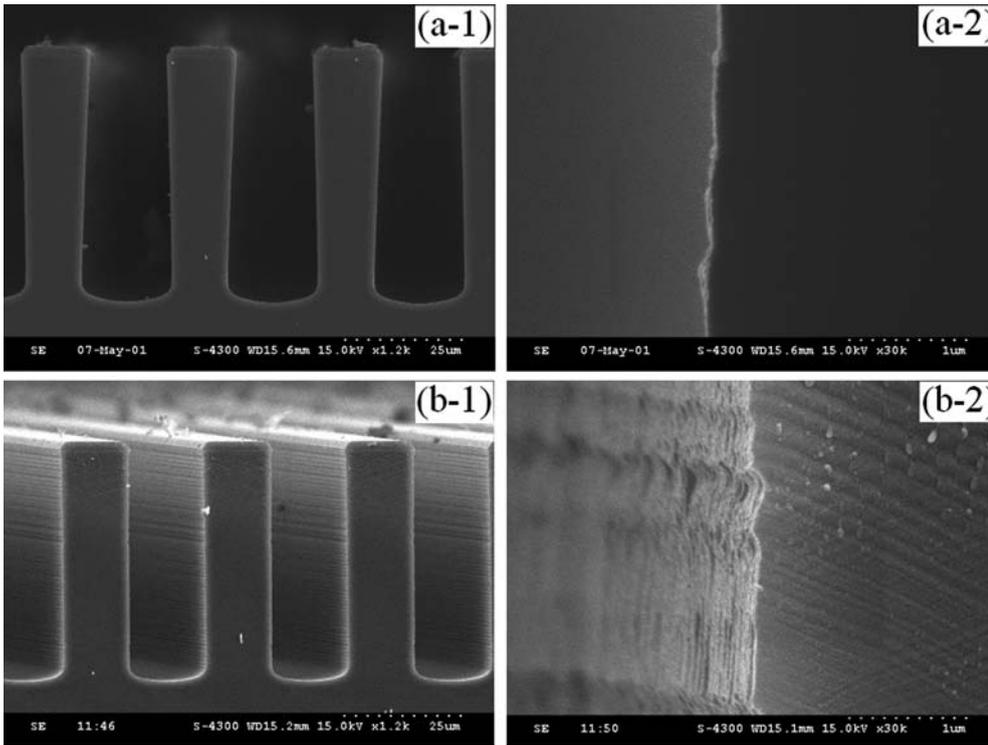


Fig. 1a, b. The effect of Ar in ASE etching step. a Trench and sidewall roughness with 40 sccm Ar flow rate; b Trench and sidewall without Ar in process

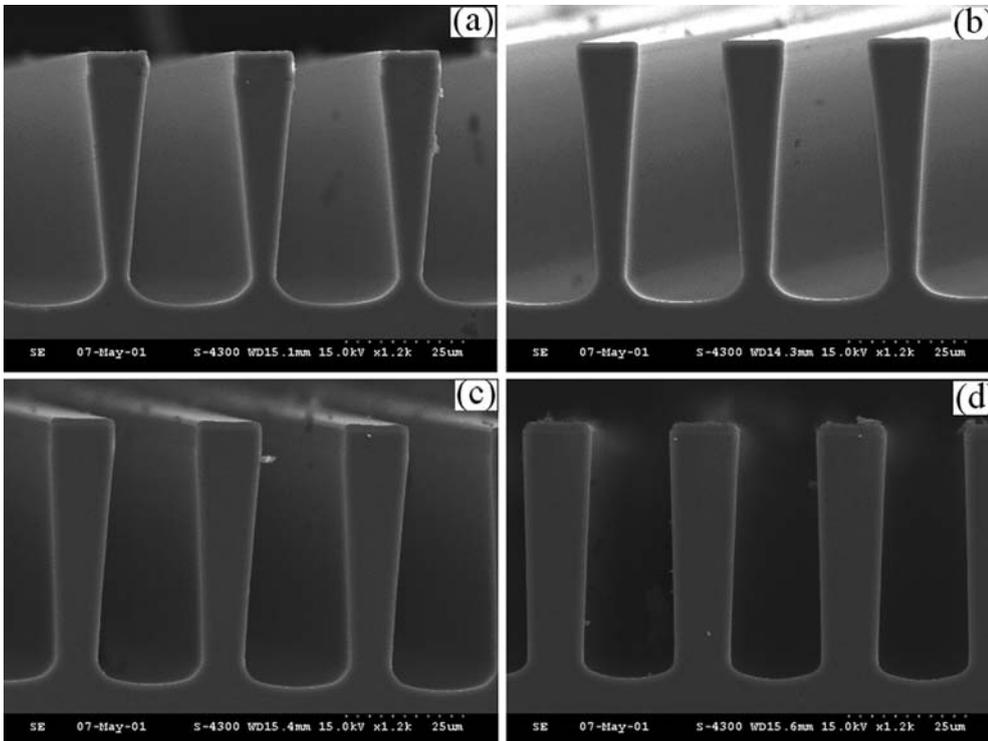


Fig. 2a, b. The effect of platen power on sidewall perpendicularity at 1000 W coil power and platen power at a 48 W; b 36 W; c 24 W; d 12 W

generated by an inductively coupled coil generator (1 kW, 13.56 MHz). The wafer is mechanically clamped to the platen electrode and the temperature can be maintained at 80 °C below. After performing the dry silicon etching, the etch profile of the trench is evaluated by a scanning electron microscope (SEM), and sidewall roughness of the trench is measured by an atomic force microscope (AFM).

3 ASE process

The ASE process is based on the technique invented by Lärmer and Schilp, where the deposition of passivation layer and etching take turns in the silicon etch process. SF_6 and C_4F_8 are used as the etching and deposition gases, respectively. The SF_6 gas supplies fluorine radicals for

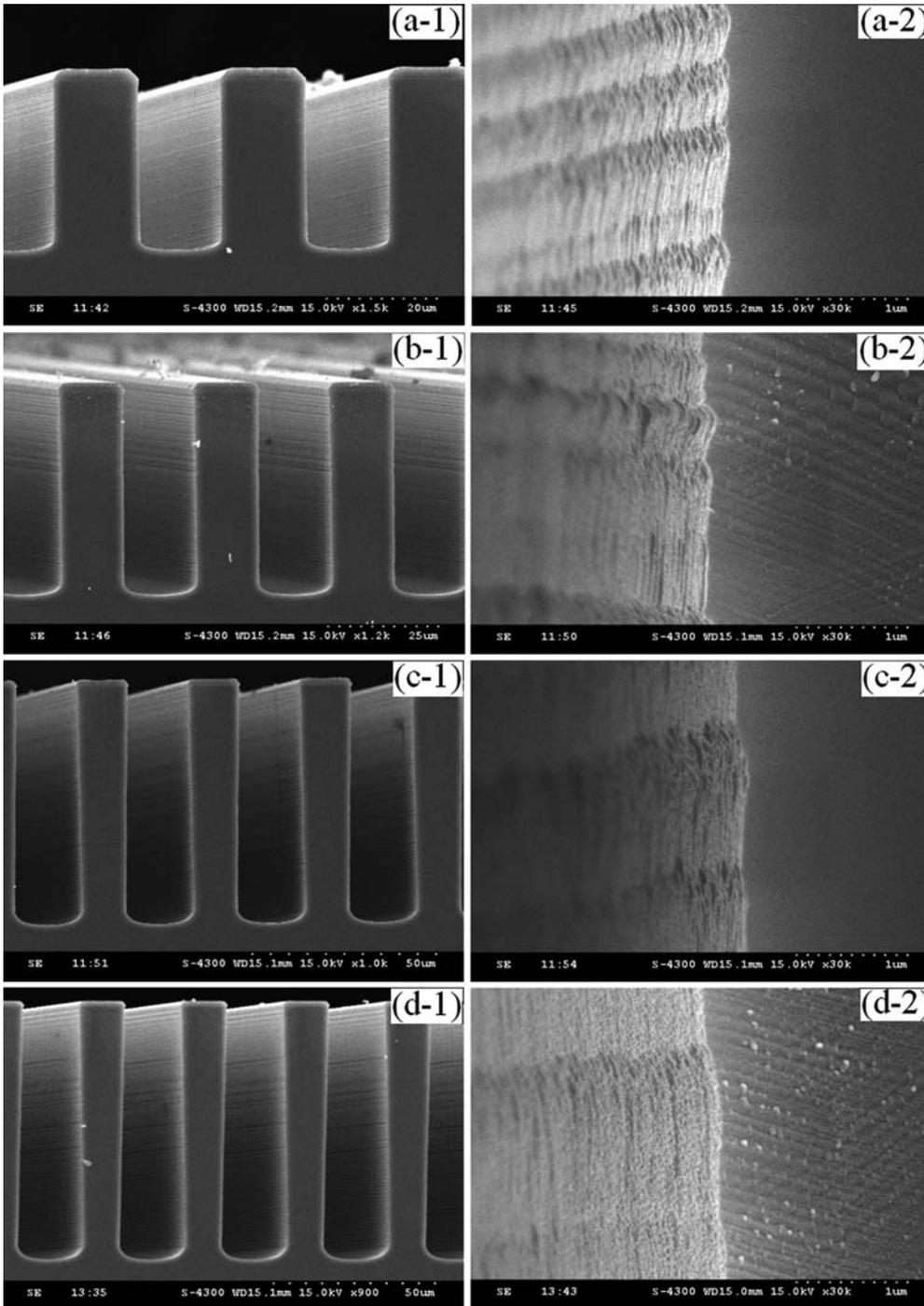


Fig. 3a, b. The trench profiles and sidewall roughness at etching cycle time of a 8 s; b 12 s; c 16 s, and d 20 s

spontaneous isotropic etching of exposed silicon. The C_4F_8 plasma deposits a $(C_xF_y)_n$ polymeric passivation layer on all substrate surface. The balance between etching and deposition determines the final process results, and this balance can be controlled through a wide variety of process parameters, which will be studied here.

4 Parameters study

In order to investigate the fabrication process to have smooth sidewall roughness and high etching rate, parameters study is performed, including ramping time, over time, Ar flow rate, platen power, SF_6 flow rate, and etching

cycle time, which are found to have obvious effect on sidewall roughness. The standard recipe used here is supplied by STS. Table 1 lists typical results of the ASE process by standard recipe. From our experimental investigations, these parameters are then adjusted one by one to improve sidewall roughness.

4.1 Ar flow rate and platen power

In RIE process, etching mode contains ion-bombardment and chemical etching. The Ar can be added to increase the effect of ion-bombardment. In standard recipe, it does not contain Ar flow rate. Here, Ar is added to observe its effect

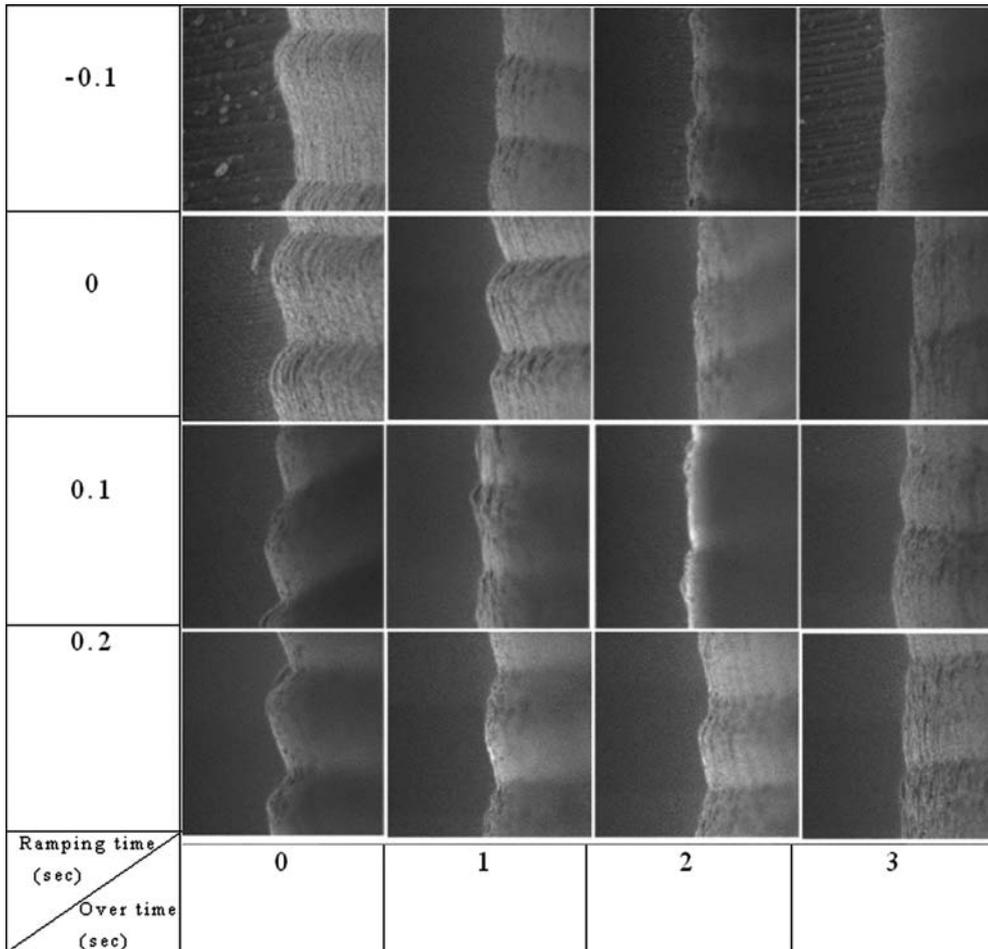


Fig. 4. The sidewall roughness at various ramping time and over time

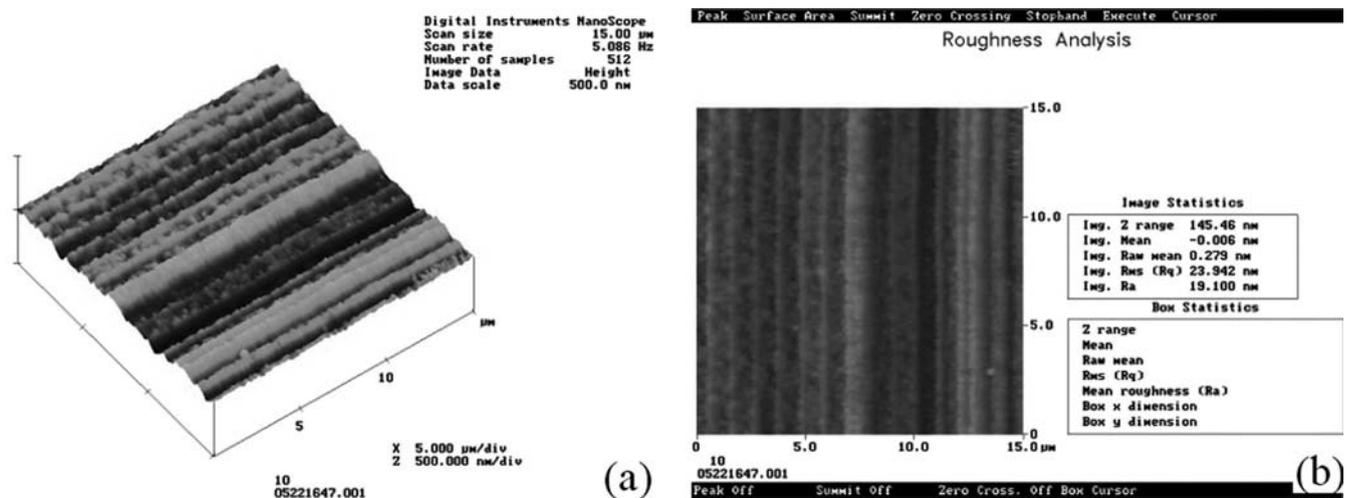


Fig. 5a, b. AFM images of trench sidewall at 2 s over time and zero ramping time. a 3-D diagram of sidewall surface; b Roughness analysis of sidewall surface

on sidewall roughness. Figure 1 shows the difference with and without Ar in ASE process, where the platen power and coil power are 12 and 1000 W, respectively. In Fig. 1a, 40 sccm of Ar flow rate is set in the etching step. From Fig. 1a-2 and 1b-2, adding Ar in ASE etching step is shown to improve surface roughness. However, it is found that, with Ar, sidewall inclined angle is worse than the result of

recipe without Ar, and 5% of Ar flow rate is suitable for sidewall roughness and profile control. The sidewall inclined angles are 88.85° in Fig. 1a-1 with Ar and 89.7° in Fig. 1b-1 without Ar. Anyway this negative taper profile can be improved by increasing the concentration of oxygen, so-called the black silicon method proposed by Jansen et al. (1995).

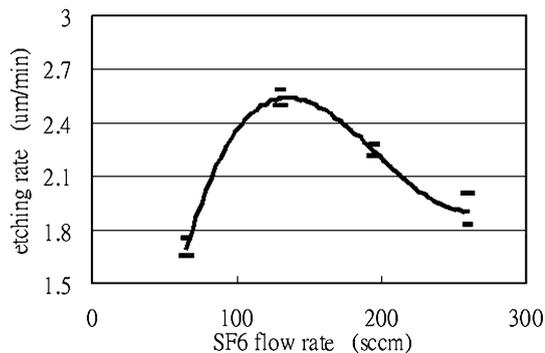


Fig. 6. Silicon etching rate at different SF₆ flow rates with fixed pressure of 25 m Torr

Not only Ar flow rate but also platen power is found to enhance the effect of ion-bombardment. The platen power source is located at the bottom of system. Figure 2 shows the relationship between the platen power and sidewall perpendicularity. Ar flow rate and coil power are set at 40 sccm and 1000 W, respectively, to observe the effect of platen power. Better sidewall perpendicularity is achieved at lower platen power. As shown in Fig. 2a and d, when the

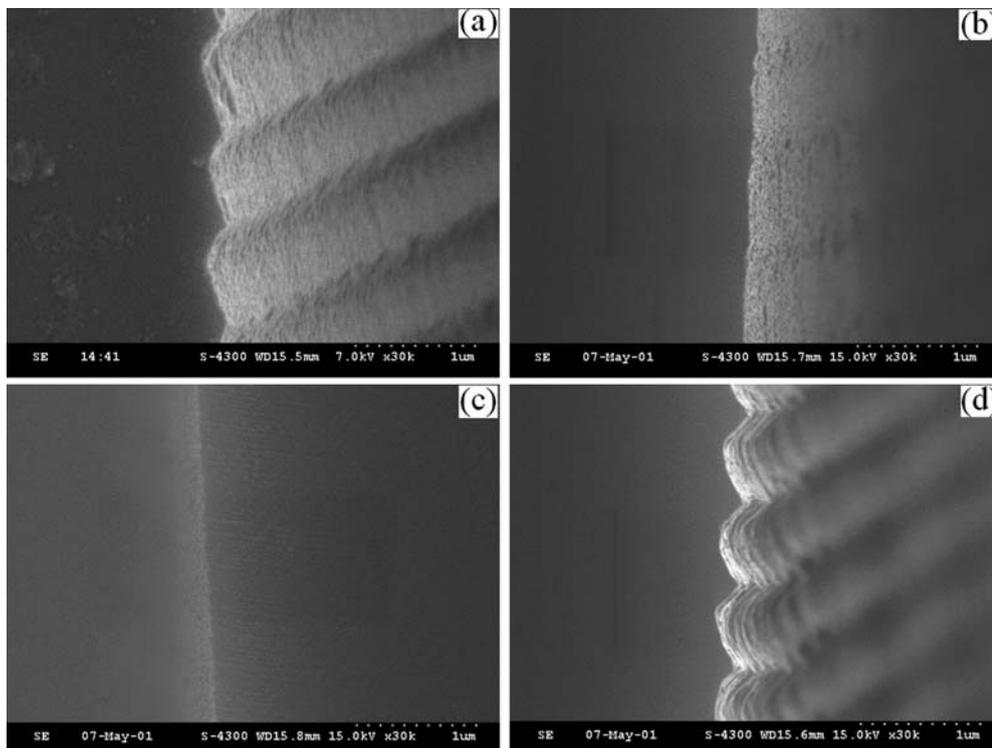


Fig. 7a, b. Sidewall roughness at SF₆ flow rate of a 65 sccm; b 130 sccm; c 195 sccm; d 260 sccm

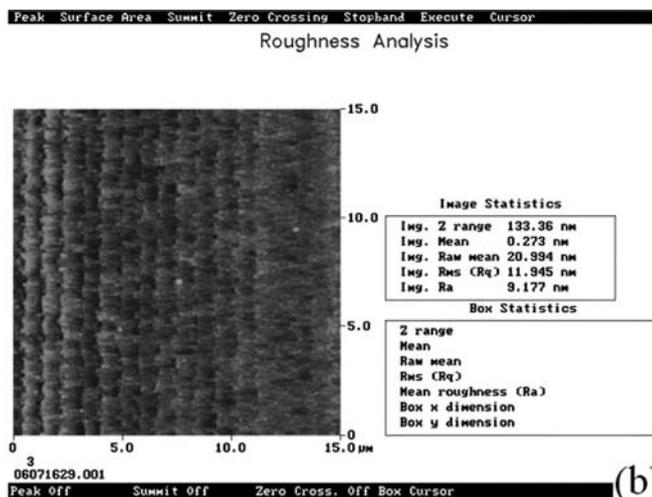
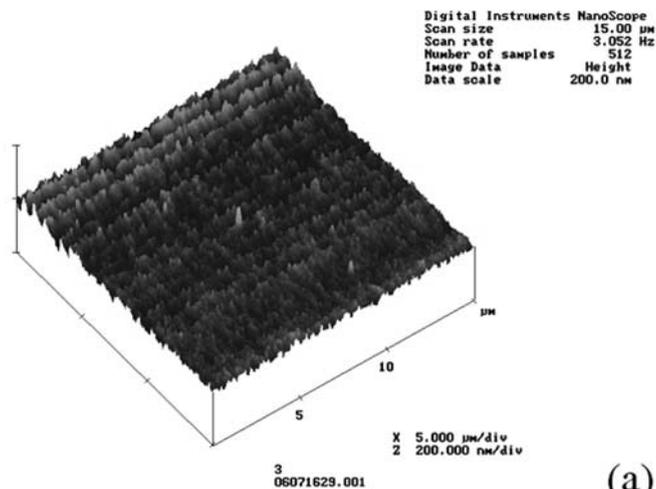


Fig. 8a, b. The AFM image of trench sidewall surface. The sample used here is obtained at 20 Ar flow rate and 2 s over time. a 3-D diagram of sidewall surface; b roughness analysis of sidewall surface

platen power is 48 W, sidewall inclined angle is 85°, and it becomes 88.85° at 12 W platen power. Because a strong electric field in the sheath provides heavier ion-bombardment to the surface close to the platen power source when a larger platen power is applied. It is also found that the selectivity of photoresist to silicon becomes worse, and the phenomenon of undercut is more serious at deeper etching depth with stronger platen power.

4.2

Time control

Here the influence of the etching cycle time to the sidewall roughness is studied. Figure 3 shows the trench profiles at different etching cycle time. With longer etching cycle time, the etching rate is higher and sidewall roughness is better, but sidewall perpendicularity becomes worse at the same time. At etching cycle time of 16 s, the inclined angle is 89.5°, etching rate is 2.8 $\mu\text{m}/\text{min}$, and sidewall roughness is 50 nm, as shown in Fig. 3c. When the etching cycle time is 20 s, the inclined angle is 88°, etching rate is 3.1 $\mu\text{m}/\text{min}$, and sidewall roughness is 40 nm, as shown in Fig. 3d.

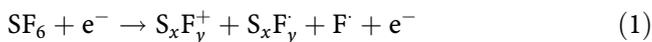
From the experimental investigations in Sects. 4.1 and 4.2, additional Ar flow rate, lower platen power, and longer etching cycle time are all found to be able to improve the sidewall roughness, but longer etching cycle time has less effect to sidewall perpendicularity.

In the STS ICP-RIE system, ramping time can change the supplying time of SF_6 and C_4F_8 in each cycle. Over time can control the overlap between etching and passivation cycle time. Figure 4 shows the SEM of trench sidewalls under different ramping time and over time. The tendency of sidewall roughness is evident. The sidewall roughness becomes smaller at longer over time and shorter ramping time in general. For example, with the standard recipe where the ramping time and the over time are all zero, the mean roughness is around 130 nm. When the ramping time is 0 s and the over time is 2 s per cycle, the mean roughness is calibrated as 19.1 nm, as shown in Fig. 5.

4.3

SF_6 flow rate

In etching cycle, SF_6 gas supplies fluorine (F) radicals for spontaneous isotropic etching of exposed silicon by mechanism illustrated below.



Etching rate is limited by the ratio of F radical and SiF_x (gas) and the mean free path of F radical. When the SF_6 flow rate is getting larger, etching rate is increased due to the higher concentration of F radical. However, too much F radical may dilute the SiF_x (gas) concentration and decrease the mean free path of F radical, so that the diffusion control will dominate the etching process to reduce the etching rate. Figure 6 shows the effect of SF_6 flow rate to

etching rate. From experimental data, the highest etching rate is achieved at a proper SF_6 flow rate, where the maximum etching rate of Si is 2.5 $\mu\text{m}/\text{min}$ at SF_6 of 130 sccm. This phenomenon also appears at the effect of SF_6 flow rate to sidewall roughness. Figure 7 shows sidewall roughness at different SF_6 flow rates, where sidewall roughness at SF_6 flow rates of 130 sccm and 195 sccm are better than the surface roughness at SF_6 flow rates of 65 sccm and 260 sccm.

4.4

Summary

By the experimental study above, the mean roughness can be effectively improved by adjusting SF_6 flow rate, etching cycle time, Ar flow rate, platen power, ramping time, and over time. When Ar flow rate is between 5% and 10% of SF_6 flow rate, platen power is 12 W, and over time is 2 s, a smoother and better perpendicular sidewall surface can be achieved. At this recipe, the sidewall mean roughness is 9.177 nm with etching rate 2.5 $\mu\text{m}/\text{min}$, as shown in Fig. 8.

5

Conclusion

A series of experiments are performed to improve the sidewall roughness with reasonable silicon etching rate and sidewall profile by adjusting various parameters in a STS ICP system here. The effects on parameters like gas flow rate, power, process cycle time are discussed. The sidewall mean roughness is demonstrated to be lower than 10 nm with etching rate about 2.5 $\mu\text{m}/\text{min}$. Comparing with other published works at similar sidewall roughness (around 10 nm), our experimental data have the highest etching rate. For the same STS ICP-RIE system, our experimental data show smallest sidewall roughness.

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