Journal of The Electrochemical Society, **150** (8) H178-H181 (2003)
0013-4651/2003/150(8)/H178/4/$7.00 © The Electrochemical Society, Inc.

A Novel Two-Step Annealing Technique for the Fabrication of High Performance Low Temperature Poly-Si TFTs

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Low temperature processed (LTP) poly-Si thin film transistors (TFTs) fabricated with a poly-Si film crystallized by a novel two-step annealing (NTSA) technique were investigated and compared with those using conventional solid phase crystallization (SPC) and excimer laser annealing (ELA) schemes. The NTSA scheme is characterized by the combination of an excimer laser induced formation of nucleation centers and a short-time low temperature furnace annealing (about 6 h at 600°C) creating clear crystalline grains with very few in-grain defects. The LTP poly-Si TFTs fabricated with a NTSA poly-Si film not only exhibit a better performance but also significantly shorten the crystallization time as compared to those fabricated using the conventional SPC (about 20 h or longer at 600°C). In addition, the uniformity of the device characteristics for the devices using the NTSA scheme is superior to that using the ELA scheme and is comparable to that using the SPC scheme.
 [DOI: 10.1149/1.1590997]

Manuscript received November 25, 2002. Available electronically July 1, 2003.

There is an increasing interest in the use of low temperature processed (LTP) polycrystalline silicon thin film transistors (poly-Si TFTs) for application in large-area display electronics, such as active matrix liquid crystal displays[1] (AMLCDs) and active matrix organic light-emitting displays[2] (AMOLEDs). It is well known that one of the most critical steps in the fabrication of high performance LTP poly-Si TFTs is the transformation of amorphous silicon (α-Si) active area into poly-Si. Generally, the poly-Si film used in the fabrication of TFTs has been traditionally obtained from α-Si film by solid phase crystallization (SPC), conducted at relatively low crystallization temperatures (about 600°C) for the fabrication of devices on a low cost glass substrate. SPC is a widely used scheme because of its simplicity and low cost as well as its ability to produce a smooth interface and excellent uniform film with a high reproducibility.[3,4] Unfortunately, SPC process at 600°C usually require a long anneal time of 20-60 h to ensure the formation of poly-Si films with large grain size, making it unattractive for manufacturing.[4,5] In addition, poly crystals made in this manner have a high density of in-grain defects due to low crystallization temperatures, which may deteriorate the electrical properties of the LTP poly-Si TFTs.[4-6] Thus, various measures have been employed to shorten the crystallization time as well as improve the device performance for the LTP poly-Si TFTs.[6-9]

Excimer laser annealing (ELA) has been actively investigated as an alternative method for the crystallization of α-Si films.[10,11] The major advantages of this technique are the formation of polysilicon grains with excellent structural quality and the ability to process selected areas without thermal damage to the glass substrate. However, the grain size of less than 100 nm as a result of extremely high solidification velocity inherent to the ELA process has been a troublesome problem. In addition, nonuniformity of laser-recrystallized poly-Si films may arise due to laser beam overlapping and poor pulse-to-pulse stability.[12,13] To cope with these problems, a number of schemes have been proposed to enlarge the grain size and improve the uniformity of poly-Si films.[11-14]

In this work, a novel two-step annealing (NTSA) scheme is proposed to transform the α-Si to poly-Si films for the fabrication of LTP poly-Si TFTs. The first step of the scheme, conducted on a thin α-Si layer, is an excimer laser annealing for the formation of a seed layer, which is followed by a second step short-time furnace annealing (about 6 h at 600°C) on a subsequently deposited thicker α-Si layer to create clear crystalline grains with very few in-grain defects. It turns out that the poly-Si TFTs fabricated with the NTSA technique not only exhibit a better performance than those fabricated with the conventional SPC technique but also possess a better uniformity in device characteristics as compared to those fabricated with the ELA process.

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Experimental

Figure 1 shows the comparison of the crystallization methods between the proposed NTSA technique and the conventional SPC/ELA technique for the fabrication of LTP poly-Si TFTs. In this work, the experimental devices made by the proposed NTSA technique were fabricated on thermal buffer oxide covered silicon wafer according to the following procedures. A thin 12 nm thick low pressure chemical vapor deposition (LPCVD) amorphous silicon (α-Si) layer was first deposited on the thermal oxide covered Si substrate at 550°C using a SiH_4 process. The α-Si film was then crystallized by a KrF excimer laser irradiation with a power density of 120 mJ/cm^2 in vacuum ($\sim 10^{-3}$ Torr) at room temperature into a poly-Si film. The wavelength, pulse width, and repetition rate of the excimer laser were 248 nm, 15 ns, and 10 Hz, respectively. A second layer of 100 nm thick α-Si was deposited, which was followed by a crystallization furnace annealing at 600°C for 2-24 h in an N_2 ambient, as shown in Fig. 1a. The crystallized poly-Si film was patterned into individual active device islands, and a 120 nm thick plasma-enhanced chemical vapor deposition (PECVD) tetraethylorthosilicate (TEOS) oxide was deposited at 300°C to serve as the gate insulator. A 200 nm poly-Si film was then deposited and patterned into the device gates. Next, the source/drain and gate regions were formed by phosphorus doping via self-aligned P^+ ion implantation at 40 keV to a dose of 5×10^{15} cm^{-2}. This was followed by an implant activation annealing at 600°C for 2 h in an N_2 ambient. Then, a 500 nm thick PE-TEOS passivation oxide was deposited at 300°C. After the contact holes were opened, metallization of Al electrodes was completed, followed by a sintering process at 400°C for 30 min in an N_2 ambient. For comparison, the control samples of devices were fabricated following the same process except that the NTSA process step was replaced by the conventional SPC or ELA process, as shown in Fig. 1b. It is noted that the conventional SPC was conducted by a furnace annealing at 600°C for 24 h in an N_2 ambient and the ELA was performed with the same conditions as used in the NTSA except that a laser energy density of 200 mJ/cm^2 was used.

In this study, all devices investigated have a gate width/length dimension of 24/4 μm and no hydrogenation is performed. XRD analysis was used to confirm the crystalline transformation of α-Si to poly-Si films. The current-voltage (I-V) characteristics of the fabricated devices were measured using an HP4145B semiconductor

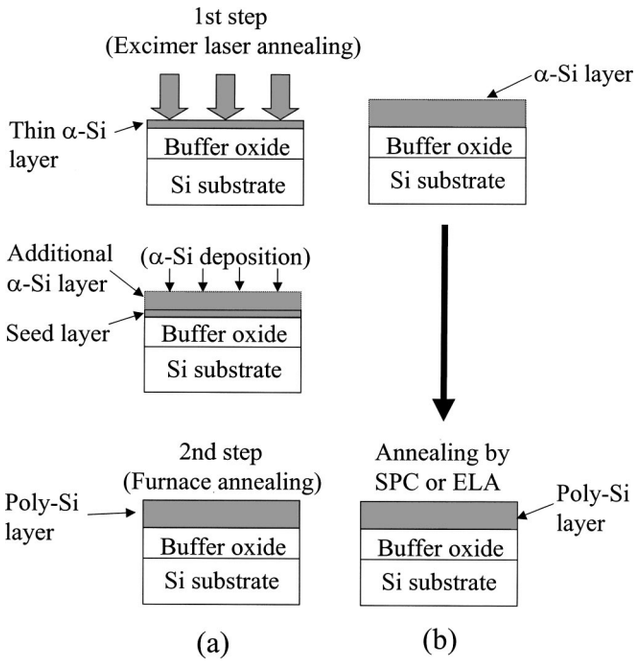

Figure 1. Comparison of crystallization techniques for the fabrication of LTP poly-Si TFTs (a) novel two-step annealing (NTSA) and (b) solid phase crystallization (SPC) or excimer laser annealing (ELA).

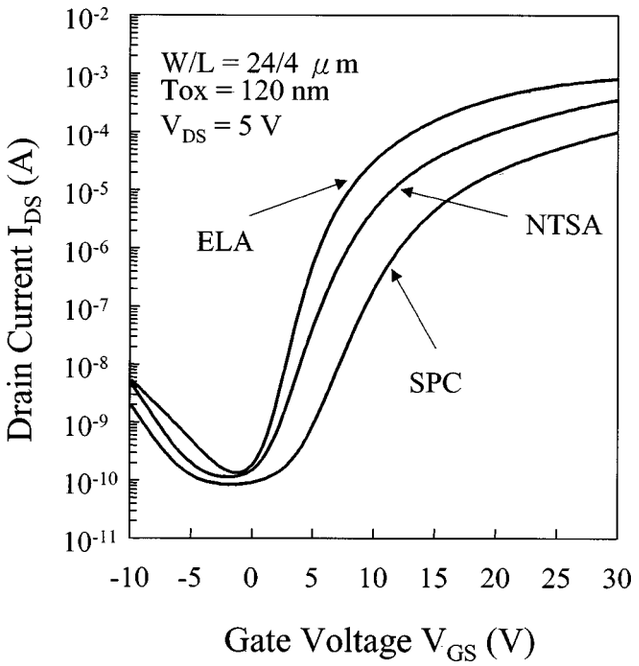

Figure 2. Typical transfer characteristics ($I_{DS} - V_{GS}$) of LTP poly-Si TFTs crystallized with different techniques of NTSA, SPC, and ELA methods.

parameter analyzer. Various device parameters including the threshold voltage (V_{TH}), the subthreshold swing (SS), the maximum drain current (I_{ON}) and the minimum drain current (I_{OFF}) were measured at a drain voltage of $V_{DS} = 5$ V. The threshold voltage is defined as the gate voltage that yields a drain current (I_{DS}) of 600 nA ($I_{DS} = 100\ \text{nA} \times \text{W/L}$). The maximum and minimum values of I_{DS} at $V_{DS} = 5$ V are designated as I_{ON} (on-current) and I_{OFF} (off-current), respectively. The field-effect mobility (μ_{FE}) is calculated from the maximum value of transconductance at $V_{DS} = 0.1$ V.

Results and Discussion

Device characteristics of LTP poly-Si TFTs using NTSA scheme.—Figure 2 shows the typical transfer characteristics ($I_{DS} - V_{GS}$) at $V_{DS} = 5$ V for the LTP poly-Si TFTs crystallized with different techniques of NTSA (at 600°C for 6 h) and conventional SPC and ELA. The measured as well as extracted key device parameters of the NTSA, SPC, and ELA processed LTP poly-Si TFTs are summarized in Table I. Note that the NTSA crystallization scheme is more efficient than the conventional SPC technique, though the ELA scheme produces an even better result. The SPC polysilicon film is characterized by its large grain size because of its slow rate of nucleation and grain growth; however, the large crystal grain contains a high density of in-grain defects, which is an inherent property of low temperature process.[15] Nevertheless, a significant improvement in device characteristics, in particular the μ_{FE} and V_{TH}, was obtained by using the NTSA scheme. This is attributed to the reduction of in-grain defects due to the formation of high quality poly-Si film by using the NTSA scheme. According to the NTSA scheme, the first layer of thin poly-Si film in the active region, formed by the excimer laser annealing, is used as a seed layer for the growth of poly-Si channel layer from the subsequently deposited thicker α-Si film. Since the laser-induced nucleation centers in the seed layer are formed from the molten stage as a result of excimer laser irradiation, they are very clear and free from any defective point. When the second layer of thicker α-Si film is deposited and then crystallized via the second step short-time furnace annealing, silicon grains will grow around these clear nucleation centers, resulting in crystallized grains with very few in-grain defect states,[16,17] which are beneficial to the device's electrical characteristics. On the other hand, the performance of the ELA poly-Si TFTs is superior to that of the NTSA poly-Si TFTs. For the laser crystallized polysilicon film, there are very few in-grain defects, such as stacking faults and twins, because the film is entirely crystallized from the molten stage, leading to the superior device performance.[10,11] Figure 3 compares the trap state densities (N_t) for the poly-Si TFTs crystallized with different techniques of NTSA, SPC, and ELA, as extracted by the Levinson and Proano method,[18,19] which can estimate the N_t from the slope of the linear segment of $\ln[I_{DS}/(V_{GS} - V_{FB})]$ *vs.* $1/(V_{GS} - V_{FB})^2$ at low V_{DS} and high V_{GS}, where V_{FB} is defined as the gate voltage that yields the minimum drain current at $V_{DS} = 0.1$ V. The device using ELA scheme had the lowest N_t while that using SPC scheme had the highest N_t. This is consistent with the above discussion and indicates that the ELA scheme results in poly-Si film of the highest quality. However, the uniformity of the ELA poly-Si film, discussed in the Results and discussion subsection on uniformity of device characteristics using NTSA scheme is a troublesome problem.

Crystallization time of NTSA scheme.—Figure 4 shows the effect of furnace annealing time (crystallization time) of the NTSA scheme on the crystallinity of polysilicon. The crystallization started to show saturation after about 6 h furnace annealing. It is well known that

Table I. Comparison of device characteristics for LTP poly-Si TFTs using different crystallization schemes of NTSA, ELA, and SPC.

Device parameters		Crystallization schemes		
		NTSA	ELA	SPC
Threshold voltage, V_{TH}	(V)	7.3	5.2	11.4
Subthreshold swing, S.S.	(V/dec)	1.53	1.15	1.97
Field-effect mobility, μ_{FE}	(cm^2/V s)	34.8	52.2	12.1
On/off current ratio, I_{ON}/I_{OFF}	(10^6)	3.1	6.1	1.2

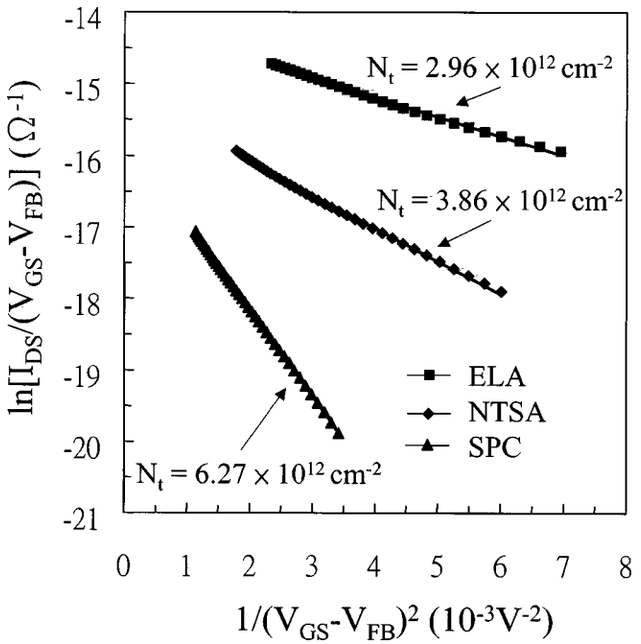

Figure 3. Trap-state densities (N_t) for the LTP poly-Si TFTs crystallized with different techniques, as extracted by the Levinson and Proano method; V_{FB} is defined as the gate voltage that yields the minimum drain current.

the crystallization using furnace annealing from an amorphous phase to a polycrystalline phase proceeds with two distinct processes: nucleation and grain growth.[16] As the crystallization annealing proceeds, nuclei will be first generated in the films and then grow into fine grains. These individual fine grains continue to grow and coalesce into larger grains. Nevertheless, the rate-limiting step of the crystallization process is the nucleation rate because the activation energy of nucleation is about two times larger than that of grain

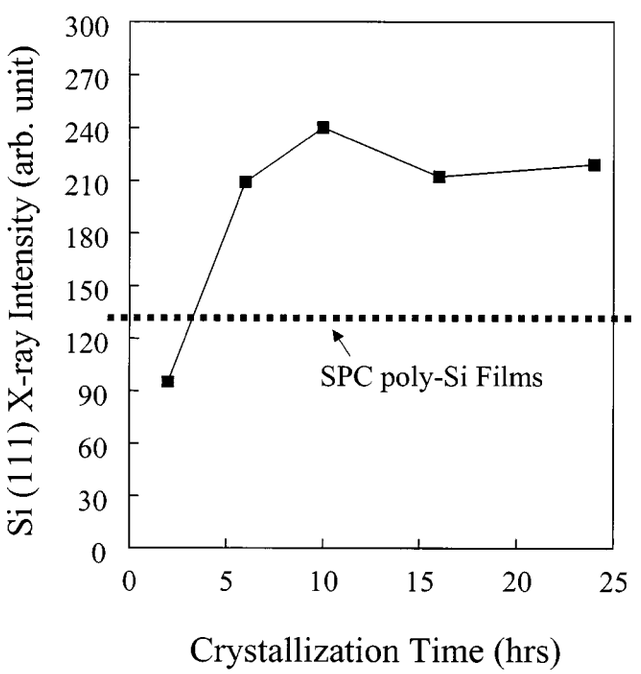

Figure 4. Si (111) X-ray reflection peak intensity *vs.* crystallization time of the NTSA scheme.

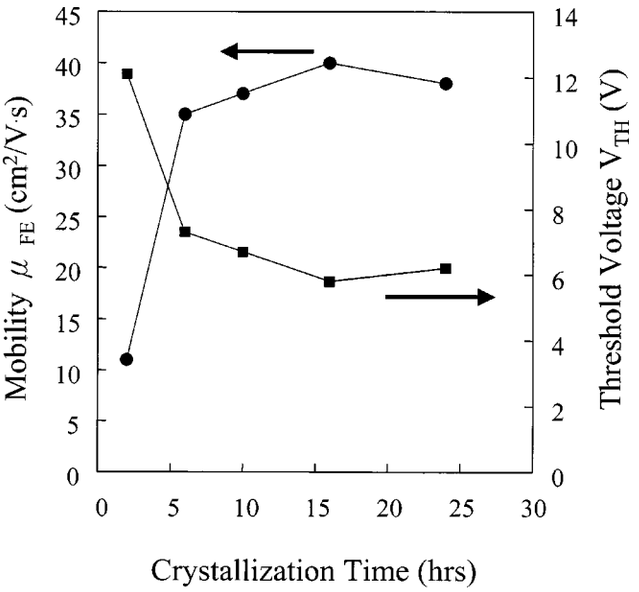

Figure 5. Field effect mobility and threshold voltage of the LTP poly-Si TFTs *vs.* crystallization time of the NTSA scheme.

growth for the furnace annealing at low temperatures.[20,21] In order to reduce the long annealing time of crystallization for α-Si films, it is necessary to reduce the incubation time of nucleation. We believe that the furnace annealing step (the second step annealing) of the NTSA scheme comprises only the growth of crystalline grains from the nuclei which are formed by the excimer laser irradiation (the first step annealing). Thus, the NTSA scheme significantly shortens the crystallization time in comparison with the conventional SPC method. In addition, the figure also demonstrates the crystallinity of SPC polysilicon film, which can identify the crystallinity of the saturated annealing NTSA polysilicon film is better than that of conventional SPC polysilicon film. This result of the better quality of NTSA poly-Si film is also consistent with the discussion of section A. Figure 5 shows the effects of crystallization time of the NTSA scheme on the field effect mobility (μ_{FE}) and threshold voltage (V_{TH}) of the LTP poly-Si TFTs. Similar tendency in the change of device characteristics (Fig. 5) and the change of polysilicon crystallinity (Fig. 4) was observed with respect to the crystallization time. Since the NTSA scheme significantly shortens the crystallization time to achieve a high performance LTP poly-Si TFTs, we believe that it is an advantageous and promising scheme for improving the performance and fabrication throughput of the LTP poly-Si TFTs.

Uniformity of device characteristics using NTSA scheme.—The statistical distribution of threshold voltage measured on the poly-Si TFTs located at various positions across the 100 nm diam substrate was used to evaluate the uniformity of the device characteristics. A total of 20 devices of each crystallization type were measured to construct the statistical distribution. Figure 6 shows the statistical distributions of the threshold voltage for the LTP poly-Si TFTs using different crystallization schemes of NTSA, ELA, and SPC. On each substrate wafer, there are 100 dies (in a matrix of 10 rows and 10 columns), and each die contains 64 devices of poly-Si TFTs. Two devices randomly chosen in each die located at the fifth row were measured, making a total of 20 measured devices, as shown in the insert in Fig. 6a. The NTSA and SPC schemes resulted in a comparable uniformity of threshold voltage, which is superior to that obtained from the ELA scheme. For laser crystallization system operated at the optimal energy density, even a small deviation in laser energy can result in a large change in the grain size, leading to poor uniformity of device characteristics.[22,23] The origin of non-

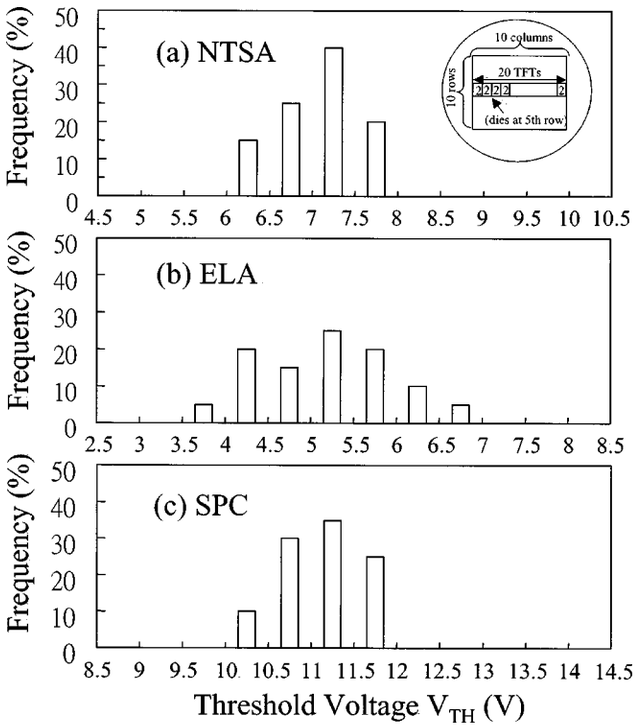

Figure 6. Statistical distributions of threshold voltage measured on devices located at positions across the 100 nm diameter substrate for the LTP poly-Si TFTs fabricated with different crystallization schemes of (a) NTSA, (b) ELA, and (c) SPC. The insert in Fig. 6a shows the locations of measured devices.

uniformity in device characteristics associated with the ELA process lies in the beam overlap regions.[13] Moreover, the pulse-to-pulse nonstability and laser beam nonhomogeneity may also contribute to the nonuniformity of the device characteristics. For the NTSA scheme, the poly-Si grain with uniform grain size is formed during the second step furnace annealing because the mechanism of the grain growth is similar to the conventional solid phase crystallized polycrystalline grain. Thus, the uniformity of device characteristics for the poly-Si TFTs using the NTSA scheme is comparable to that using the SPC scheme.[17]

Table II shows the qualitative comparison of different crystallization schemes for the fabrication of LTP poly-Si TFTs. The conventional SPC scheme produces excellent uniform distribution of grain size, but the device performance and the production throughput are not quite satisfactory. The ELA scheme is able to produce high performance poly-Si TFTs but the uniformity of the device characteristics is rather poor. However, from the manufacturing viewpoint, device performance and production throughput as well as uniformity of device characteristics must all be considered simultaneously. In this respect, we believe that the proposed NTSA scheme is a promising crystallization technique for the production of LTP poly-Si TFTs, in particular the product of uniformity issues, *e.g.*, the flat-panel displays fabricated by active matrix organic light-emitting diode driven by LTP poly-Si TFTs.

Table II. Qualitative comparison of different crystallization schemes for the fabrication of LTP poly-Si TFTs.

	Crystallization schemes		
Parameters	SPC	ELA	NTSA
Field effect mobility	Poor	Excellent	Good
Uniformity of device characteristics	Good	Poor	Good
Production throughput	Poor	Good	Fair

Conclusions

LTP poly-Si TFTs using an NTSA technique were investigated and compared with those using SPC and ELA schemes. The NTSA scheme resulted in a significant improvement in device characteristics with much less crystallization time, as compared with the conventional SPC scheme. This is attributed to the formation of crystalline grains with very few in-grain defects because these crystalline grains grew from the very clear nucleation centers formed on a seed layer induced by the excimer laser irradiation during the first step annealing. Since the furnace annealing of the NTSA scheme comprises only the growth of crystalline grains from the nuclei formed by the excimer laser irradiation, the crystallization time can be significantly shortened. In addition, the NTSA scheme was able to produce poly-Si TFTs with good uniformity in device characteristics because the mechanism of grain growth is similar to the SPC. From the manufacturing viewpoint, we believe that the NTSA scheme is a promising crystallization technique for the production of LTP poly-Si TFTs because of its superior tradeoff between device performance, device characteristics uniformity and production throughput.

The National Huwei Institute of Technology assisted in meeting the publication costs of this article.

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