Investigation of Grain Boundary Control in the Drain Junction on Laser-Crystalized Poly-Si Thin Film Transistors

Tien-Fu Chen, Ching-Fa Yeh, and Jen-Chung Lou

***Abstract*—This letter investigates the influences of grain boundaries in the drain junction on the performance and reliability of laser-crystalized poly-Si thin film transistors (TFTs). A unique test structure where the channel region includes 150-nm-thick laser-crystalized poly-Si with small grain sizes and a 100-nm-thick one with large grain sizes is fabricated. Different behaviors in the electrical characteristics and reliability of a single TFT are observed, first under measurements of the forward mode and then under measurements of the reverse mode. This is due to the different number of grain boundaries in the drain junction. Grain boundaries in the drain junction were found to cause reduced ON/OFF current ratio, variations in threshold voltage with drain bias, significantly increased kink effect in the output characteristics, and poor hot-carrier stress endurance.**

***Index Terms*—Drain junction, electrical characteristics, grain boundaries, kink effect, laser-crystalized poly-Si, reliability.**

I. Introduction

LASER-ANNEALED polycrystalline silicon thin film transistors (poly-Si TFTs) have widely been explored owing to their possibilities for integrating peripheral driver circuits with active matrix liquid crystal displays (AMLCDs) on large area glass substrates [1]. To achieve system on glass (SOG), poly-Si TFTs with high carrier mobility and good reliability are required [2]. Several techniques have been proposed for enhancing carrier mobility, such as enlarging the grains in the channel, and improving their reliability by reducing the electric field near the drain [3], [4].

However, the random distribution of the grain boundaries (GBs) in the channel impairs device performance uniformity. The influence of the grain-boundary location on the poly-Si TFTs was first considered from the data obtained in two-dimensional (2-D) device simulations [5]. To further control the performance of laser-crystalized poly-Si TFTs, the number of GBs in the drain junction have to be considered. In this letter, a TFT is fabricated that includes two different grain sizes of the laser-crystalized polysilicon in the channel. To avoid device-to-device variations, such as the difference in the number of GBs in the channel, and the channel shortening effect due to the diffusion of dopants from source and drain, this study adopted the measurements from both the forward and reverse modes in a single TFT [6]. The purpose in taking this approach was to study the influences of the GBs in the drain junction on the performance and reliability of laser-annealed poly-Si TFTs. Behaviors differed between the forward and reverse modes because of the different number of GBs in the drain junction.

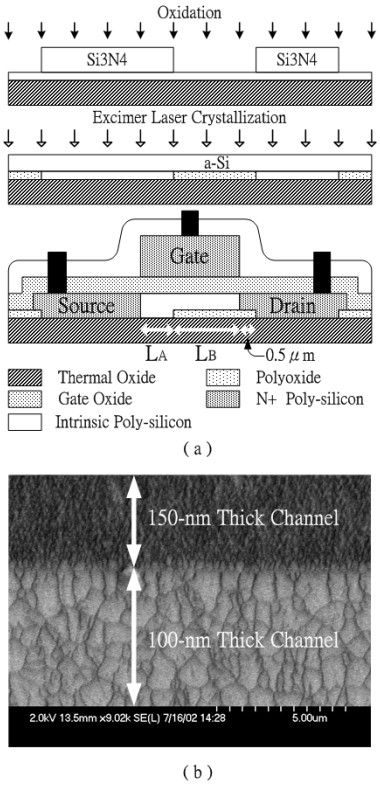

Fig. 1. (a) Key processes for fabricating this test structure showing source and drain region in relation to the channel thickness under measurements of forward mode. (b) SEM photograph of laser-crystalized poly-Si after Secco etching.

II. Experiment

The key processes to fabricate this test structure are displayed in Fig. 1(a). First, a 50-nm-thick amorphous silicon layer was deposited on thermally oxided (2-μm thick) Si wafers by decomposing SiH_4 in LPCVD system at 550 °C. Next, a 150-nm-thick silicon nitride layer was deposited and then patterned. The exposed silicon film was fully oxidized at 925 °C using silicon nitride patterns as a hard mask. Meanwhile, the silicon nitride patterns were selectively etched in a hot phosphoric acid bath

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at 165 °C. After removing the native oxide on silicon film region, a 100-nm amorphous silicon layer was deposited by the decomposition of SiH_4 in LPCVD system at 550 °C. The wafer was then placed on a 400 °C stage in a vacuum chamber under pressure of 10^{-3}Torr. The crystallization of amorphous silicon layer was carried out by irradiation using the KrF excimer laser. After defining the active channel region, a 135-nm-thick TEOS gate oxide was deposited by PECVD at 350 °C. Subsequently, a 250-nm amorphous silicon layer was deposited and then patterned as the gate electrode. The source and drain regions were formed by self-aligned ion implantation of phosphorous with a dosage of $5 \times 10^{15}\text{cm}^{-2}$ at 50 KeV. A 300-nm TEOS passivation oxide was deposited, and then the dopants were activated at 600 °C for 12 h. Finally, contact opening and metallization were performed. No further hydrogenation procedures were implemented after sintering at 400 °C for 30 min.

As shown in Fig. 1(a), the heavily doped region near the 100-nm-thick channel side is defined as drain when a TFT is measured in the forward mode. The other is defined as drain under measurements of the reverse mode. The channel length L comprises 150-nm thick channel length L_A and 100-nm-thick channel length L_B. A margin of 0.5 μm is assigned for the proposed TFTs, as presented in Fig. 1(a). The laser energy densities between completely melting 100-nm-thick silicon film and partially melting a 150-nm one were employed to form two different grain sizes of laser-crystalized polysilicon [3]. Meanwhile, Fig. 1(b) displays the SEM photograph of laser-crystalized poly-Si. Large and small grains are formed in the channel simultaneously. The different number of GBs in the drain junction are exhibited under measurements of the forward and reverse modes.

III. Results and Discussion

Fig. 2 illustrates the transfer characteristics of the laser-crystalized poly-Si TFT under first forward and second reverse mode. Notably, the leakage current in the reverse mode is significantly higher than that in the forward mode. This increase in the leakage current results from the marked increase of the GBs in the drain junction [7]. Many carriers generated from the GBs via thermionic-field emission result in higher leakage current in the reverse mode than the forward mode. The on-currents are almost identical for both mode measurements because of the TFT operated in linear region. Therefore, the order of magnitude in the on/off current ratio is reduced at high drain bias in the reverse mode compared to the forward mode. Fig. 2 also indicates that the threshold voltage V_{th} which is defined as the gate bias for a drain current of $(W/L) \times 100$ nA, is 5.78 and 5.20 V in the reverse mode at $V_{\text{DS}} = 6$ and $V_{\text{DS}} = 11$ V, respectively. However, the V_{th} is maintained at 5.90 V for both $V_{\text{DS}} = 6$ V and $V_{\text{DS}} = 11$ V in the forward mode. The reduction in V_{th} in the reverse mode results from the avalanche induced short channel effect [8]. This effect is not observed in the forward mode, because the drain junction contains large grains and fewer GBs.

As shown in Fig. 3, the kink effect which causes a rapid increase in drain current appears more prominently in the reverse mode than in the forward mode [9]. This phenomenon can be

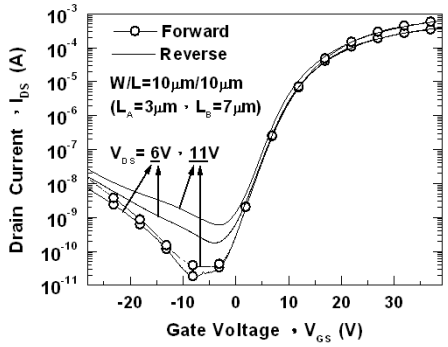

Fig. 2. Transfer characteristics of the laser-crystalized poly-Si TFT under forward and reverse mode measurements in one TFT.

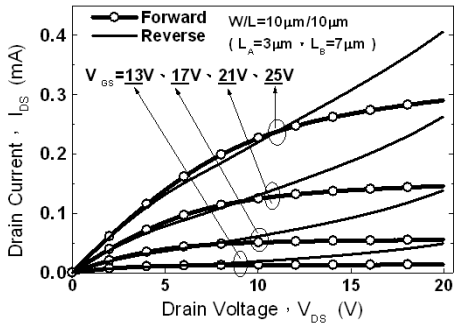

Fig. 3. Output characteristics of the laser-crystalized poly-Si TFT under forward and reverse mode measurements in one TFT.

attributed to the drain induced grain-boundary barrier lowering effect and the grain-boundary traps induced avalanche generation effect [10], [11]. The former effect is caused by the drain bias V_{DS} modulating the barrier height of the GBs in the drain junction to form an asymmetric barrier. Extra carriers which are injected from the lowered barrier side into the drain side cause the drain current to increase with the drain voltage [12]. The latter effect results from the higher electric field created by grain-boundary traps in the drain junction. Electron-hole pairs are generated by the impact ionization process, resulting in a lack of saturation in the output characteristics [13].

Fig. 4 shows the threshold voltage variations ΔV_{th} and the degradation of the maximum transconductance $G_{m\max}$ in a single TFT under static hot-carrier stress which is defined as the TFT being kept at a high electric field in the drain junction. The TFT is first stressed in the forward mode and then in the reverse mode. Notably, the dc stress conditions are $V_{\text{DS}} = 20$ V and $V_{\text{GS}} = 10$ V for 10 000 s. The ΔV_{th} is defined as $V_{\text{th},s}$-$V_{\text{th},i}$ where $V_{\text{th},i}$ denotes the initial V_{th} and $V_{\text{th},s}$ represents the V_{th} for etch stress time. Moreover, the degradation of the $G_{m\max}$ is defined as $\Delta G_{m\max}/G_{m\max,i}$, where $\Delta G_{m\max} = G_{m\max,s} - G_{m\max,i}$, $G_{m\max,i}$ denotes the initial $G_{m\max}$ and $G_{m\max,s}$ represents the $G_{m\max}$ for each stress time. The ΔV_{th} and $\Delta G_{m\max}/G_{m\max,i}$ are measured at $V_{\text{DS}} = 0.1$ V for etch stress time. One can see that the V_{th} and the $G_{m\max}$ are virtually unchanged in the forward stress but are strongly degraded in the reverse stress. This effect occurs due to the higher electric field at the drain junction in the reverse exceeding that in the forward mode. Notably, the high

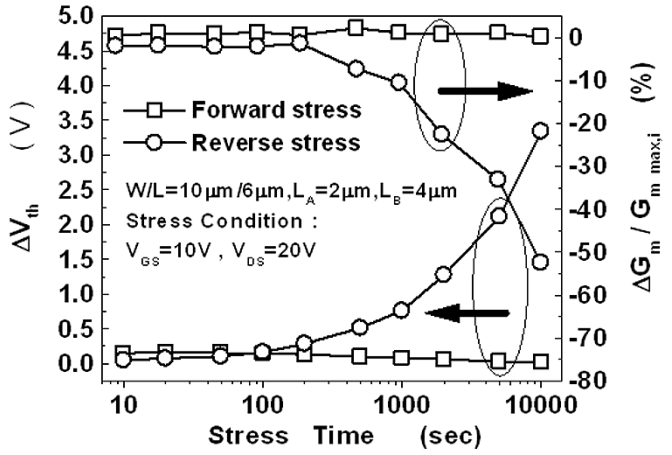

Fig. 4. Threshold voltage variation and degradation of maximum transconductance under static hot-carrier stress in a single TFT. The TFT is first stressed in the forward mode, and then second stressed in the reverse mode. Meanwhile, the threshold voltage $V_{\rm th}$ is defined as a drain current of $(W/L) \times 10^{-8}$ A at $V_{\rm DS} = 0.1$ V.

electric field promotes impact ionization, resulting in numerous grain-boundary traps being created in the drain junction.

IV. Conclusion

This investigation has demonstrated that GBs in the drain junction seriously impedes the performance and reliability of the laser-crystalized poly-Si TFTs. Grain-boundary traps in the drain junction boosted the leakage current, caused threshold voltage to vary with drain bias, enhanced the kink effect in the output characteristics, and degraded device performance under static hot-carrier stress. These effects are attributed to the high local electric field in the drain junction.

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