Radio-Frequency Small-Signal and Noise Modeling for Silicon-on-Insulator Dynamic Threshold Voltage Metal–Oxide–Semiconductor Field-Effect Transistors

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Radio-Frequency Small-Signal and Noise Modeling for Silicon-on-Insulator Dynamic Threshold Voltage Metal–Oxide–Semiconductor Field-Effect Transistors

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This paper presents small-signal and noise modeling for radio-frequency (RF) silicon-on-insulator (SOI) dynamic threshold voltage (DT) metal–oxide–semiconductor field-effect transistors (MOSFETs). The inherent body parasitics, such as source- and drain-side junction capacitances, and access body resistance have been incorporated in this model. In addition, the analytical equations useful for parameter extractions are derived. The modeling results show good agreements with the measured data both in RF small-signal and noise aspects up to 12 GHz. Besides, we have made comparisons of important model parameters for DT and standard MOSFETs. The extracted parameters show reasonable trend with respect to applying voltages and channel lengths, which reveals the accuracy of the extraction results using our proposed method.

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1. Introduction

The DC and AC characteristics of the dynamic threshold voltage (DT) metal–oxide–semiconductor field-effect transistor (MOSFET) have been widely studied since its introduction in 1994. Due to its larger driving ability with low leakage current, it is attractive for low power applications.[1)] To improve its performance, some optimized silicon-on-insulator (SOI)- or bulk-based fabrication processes have been reported as well.[2,3)]

Especially, several investigations have demonstrated its ability of radio-frequency (RF) applications with high cut-off frequency (f_t) and maximum oscillation frequency (f_{max}).[4–6)] On the other hand, a physical RF small-signal model along with an efficient parameter extraction method is very important for the RF process control and circuit simulations, but its related studies is deficient so far.

In this paper, we will conduct RF small-signal modeling for the SOI DT MOSFET and demonstrate a practical extraction method to facilitate the extraction work with physical accuracy. Based on the small-signal model structure, the RF noise model for the DT MOSFET will be built, and this model is shown to well capture its RF noise behavior. Finally, the accuracy of some important model parameters will be examined by comparing them to those of the standard devices with different channel lengths at various bias conditions.

2. Devices

The RF SOI DT MOSFETs used in this work were fabricated using UMC 65 nm SOI technology. These RF devices were laid out in the multi-finger and multi-group structure with the following denotations: L for channel length, W_F for finger width, N_F for the number of fingers, and N_G for the number of groups.

On-wafer two-port common-source S and high frequency noise parameters up to 12 GHz were measured using ATN noise parameter measurement system with microwave probes. To eliminate the inevitable parasitic accompanied with the probing pads, the S-parameters of devices' corresponding open dummy were measured and then used to perform the S and noise parameters de-embedding procedure. Furthermore, the proposed zero method has been used to extract the series resistances, and the good extraction results are shown in Fig. 1.[7)]

3. Model and Parameter Extraction

The small-signal equivalent circuit for SOI DT MOSFETs has been presented and is depicted in Fig. 2.[8)] For simplification, the neutral-body resistance between the two junction capacitances is ignored due to its lower effect below GHz.[9)] Based on this circuit, its simple and analytic two-port admittance (Y) parameters can be derived when the effect of series resistances compared to access body resistance (R_b) can be neglected. Following especially shows the expressions benefiting the parameter extraction:

$$\mathrm{Re}\,Y_{11} \approx \frac{(R_b + R_{bs}) + \omega^2\Delta^2/R_b}{den} \tag{1}$$

$$\frac{\mathrm{Im}\,Y_{11}}{\omega} \approx (C_{gs} + C_{gd}) + \frac{\Delta^2/[R_b^2(C_{bs} + C_{bd})]}{den} \tag{2}$$

$$\begin{aligned}\mathrm{Re}\,Y_{gain} &\approx \mathrm{Re}(Y_{21} - Y_{12}) \\ &= g_m + \frac{g_{mb}\Delta(R_b + R_{bs})/[R_b(C_{bs} + C_{bd})]}{den}\end{aligned} \tag{3}$$

$$\begin{aligned}\frac{\mathrm{Im}\,Y_{gain}}{\omega} &\approx \frac{\mathrm{Im}(Y_{21} - Y_{12})}{\omega} \\ &= -g_m\tau - \frac{g_{mb}\Delta^2/[R_b(C_{bs} + C_{bd})]}{den}\end{aligned} \tag{4}$$

$$\begin{aligned}\mathrm{Re}\,Y_{22} \approx{}& \frac{1}{R_{ds}} \\ &+ \frac{\omega^2\Delta C_{bd}[g_{mb}\Delta + C_{bd}(R_b + R_{bs})]/(C_{bs} + C_{bd})}{den}\end{aligned} \tag{5}$$

$$\begin{aligned}\frac{\mathrm{Im}\,Y_{22}}{\omega} \approx{}& (C_{gd} + C_{ds}) \\ &+ \frac{C_{bd}(R_b + R_{bs})[(R_b + R_{bs}) + g_{mb}\Delta/(C_{bs} + C_{bd})]}{den} \\ &+ \frac{\omega^2\Delta^2 C_{bd}[(C_{bs} + C_{bd}) - C_{bd}]/(C_{bs} + C_{bd})}{den}\end{aligned} \tag{6}$$

$$\frac{\mathrm{Im}\,Y_{12}}{\omega} \approx -C_{gd} - \frac{C_{bd}\Delta(R_b + R_{bs})/[R_b(C_{bs} + C_{bd})]}{den} \tag{7}$$

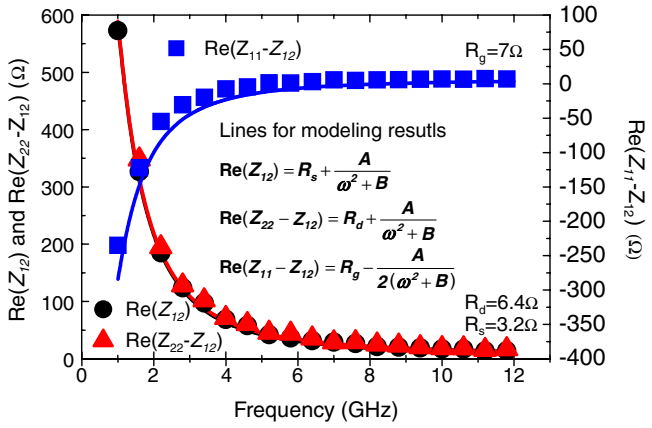


Fig. 1. (Color online) Model-data comparison for the extraction of series resistances using zero method ($L/W_F/N_F/N_G$ = 0.24 μm/1 μm/8/16, and V_{GS} = V_{DS} = 0 V).

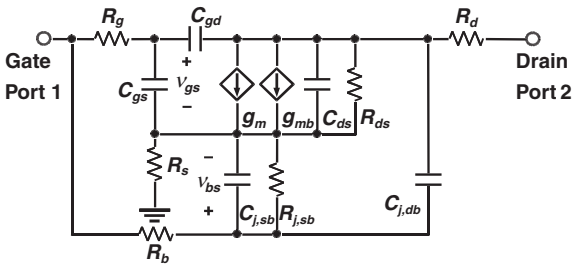


Fig. 2. RF small-signal equivalent circuit for the SOI DT MOSFET.

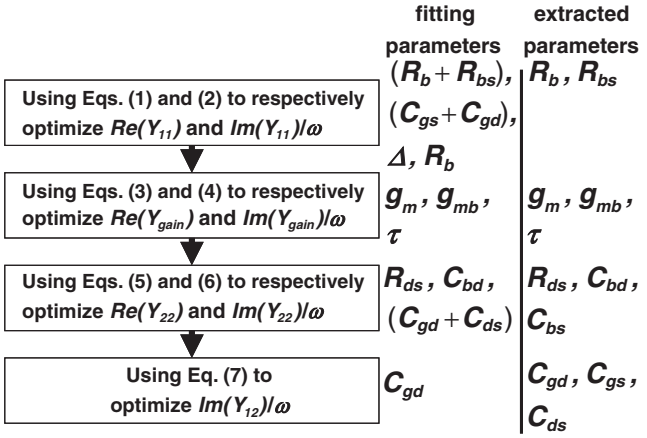
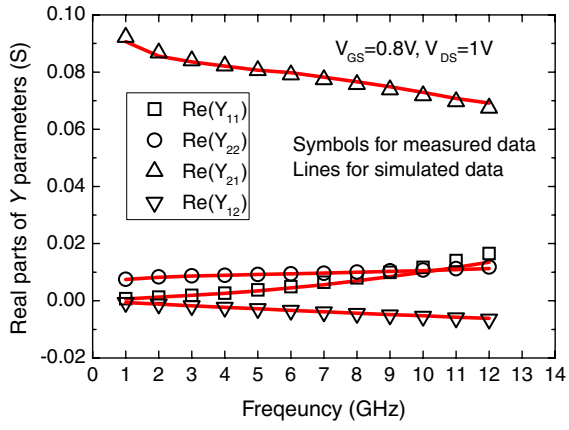


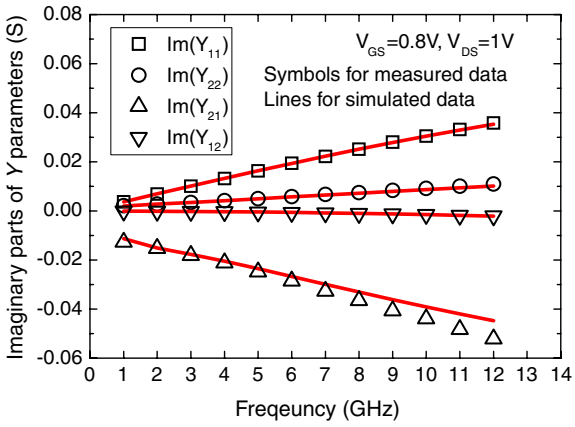
Fig. 3. Proposed parameter extraction flow.

where $den \equiv (R_b + R_{bs})^2 + \omega^2\Delta^2$ and $\Delta \equiv R_b R_{bs}(C_{bs} + C_{bd})$. A practical extraction procedure shown in Fig. 3 is then proposed. Compared to the method proposed in ref. 8, our extraction method relies only on local optimizations with definite fitting targets and model parameters, so the excellent modeling results with less than 10% relative root-mean-square errors for each real and imaginary part of Y-parameters, as shown in Fig. 4, can be expected. For the reader's reference, the extracted model parameters are listed in Table I.

Besides, as shown in Fig. 5, based on the RF small-signal equivalent circuit, the RF noise equivalent circuit can be built by adding the corresponding noise current sources. In



(a)



(b)

Fig. 4. (Color online) Modeling results for (a) Re Y and (b) Im Y ($L/W_F/N_F/N_G$ = 0.24 μm/1 μm/8/16).

Table I. Extracted model parameters for bias condition V_{GS} = 0.8 V, and V_{DS} = 1 V ($L/W_F/N_F/N_G$ = 0.24 μm/1 μm/8/16).

g_m (mS)	R_{ds} (Ω)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	τ (ps)	g_{mb} (mS)	R_b (Ω)	R_{bs} (Ω)	$C_{j,sb}$ (fF)	$C_{j,db}$ (fF)	$\overline{i_d}$ (pA/$\sqrt{\text{Hz}}$)
127	93	550	79	1.3	1.6	38	597	2083	246	20	60

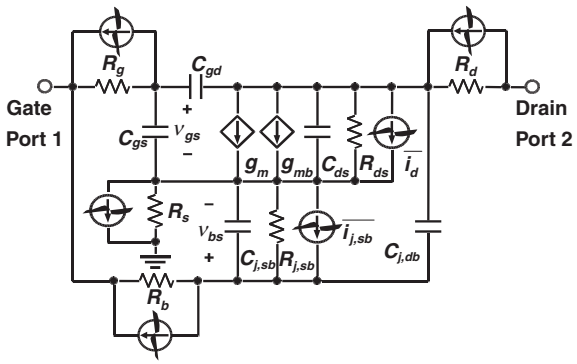
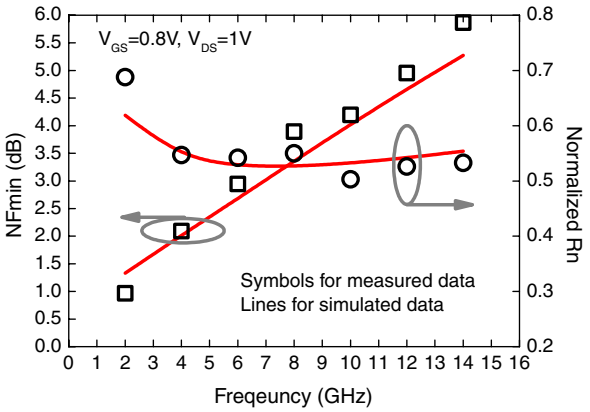
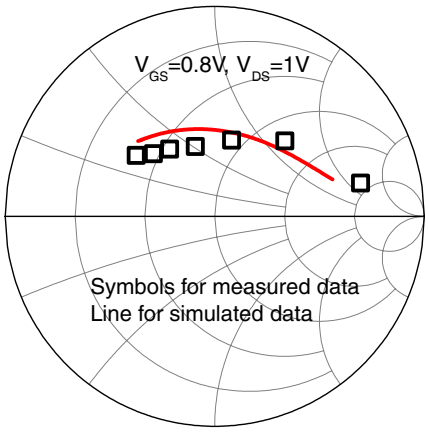


Fig. 5. RF noise equivalent circuit for the SOI DT MOSFET.

this noise equivalent circuit, $\overline{i_d}$ stands for the intrinsic channel noise current, and the assumption that the high-frequency prominent drain-induced gate noise can be neglected is adopted. This assumption had been shown to be reasonable especially for deep sub-micrometer devices.[10] Furthermore, the noise current sources related to series



(a)



(b)

Fig. 6. (Color online) Noise modeling results for (a) NF_{min}, R_n, and (b) Γ_{opt} ($\overline{i_d}$ = 60 pA/$\sqrt{\text{Hz}}$, and $L/W_F/N_F/N_G$ = 0.24 μm/1 μm/8/16).

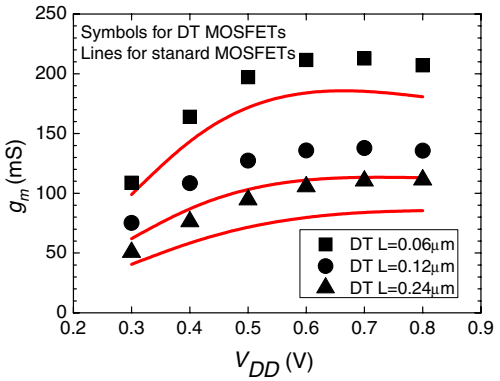


Fig. 7. (Color online) g_m vs V_{DD} characteristics for DT and standard MOSFETs with different channel lengths ($W_F/N_F/N_G$ = 1 μm/8/16).

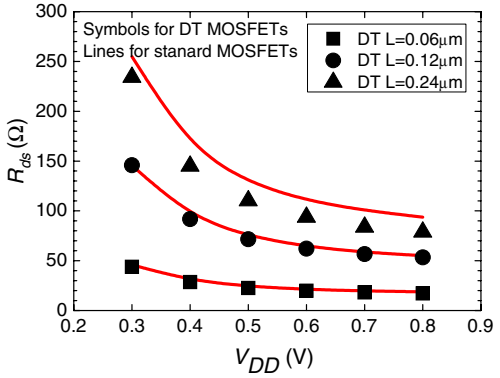


Fig. 8. (Color online) R_{ds} vs V_{DD} characteristics for DT and standard MOSFETs with different channel lengths ($W_F/N_F/N_G$ = 1 μm/8/16).

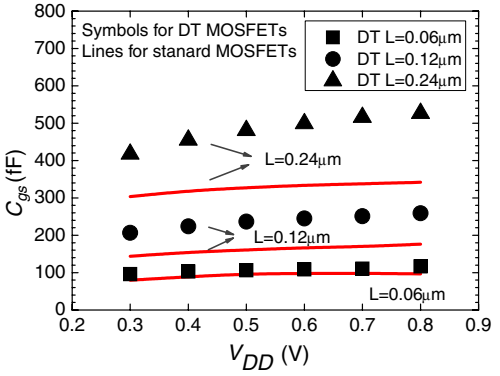


Fig. 9. (Color online) C_{gs} vs V_{DD} characteristics for DT and standard MOSFETs with different channel lengths ($W_F/N_F/N_G$ = 1 μm/8/16).

resistances and access body resistance are considered as thermal noise current sources ($\overline{i} = \sqrt{4kT/R}$, R: resistance value). Finally, the inherent shot noise current caused by the source-side junction current is estimated using shot noise current formula ($\overline{i_{j,sb}} = \sqrt{2qI_b} \approx \sqrt{2qI_g}$).

The only one unknown model parameter $\overline{i_d}$ can be directly obtained by optimizing the four measured high-frequency noise parameters ($NF_{min}, R_n, |\Gamma_{opt}|$, and $\angle\Gamma_{opt}$). The good noise modeling results are shown in Fig. 6.

4. Model Verification and Discussions

To further examine the accuracy of the modeling results, some important model parameters versus V_{DD} [the bias applying to both gate and drain terminals, i.e., $V_{DS} = V_{GS}(= V_{BS}) = V_{DD}$] for different channel lengths are examined. Figure 7 shows that compared to the standard device, the DT device has larger transconductance (g_m) due to its lower threshold voltage (V_T) and higher mobility arising from lower depletion charge.[1)] Hence, this phenomenon could be more obvious at larger V_{DD}. Besides, lower V_T and higher mobility can also help decrease the channel resistance. However, in the saturation region the DT devices may have lower channel electric field than the standard devices, which in turn tends to increase the channel resistance.[11)] This effect is more prominent for shorter DT devices, and it explains the smaller difference in channel resistance (R_{ds}) for shorter channel devices in Fig. 8.

Besides, lower threshold voltage also increases the channel charge, and hence increases the intrinsic capacitance.[1)] Therefore, as shown in Fig. 9, the DT device would have larger gate-to-source capacitance (C_{gs}) than the standard one. Figure 10 shows that the body transconductance (g_{mb}) tends to increase with V_{DD}. However, in the low-voltage regime where the DT device normally operates, compared to g_m, its value is small and hence its contribution to the total device performance could be negligible.

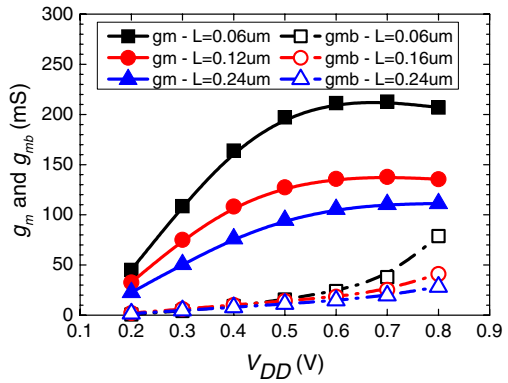


Fig. 10. (Color online) g_{mb} and g_m vs V_{DD} characteristics for DT MOSFETs with different channel lengths ($W_F/N_F/N_G$ = 1 μm/8/16).

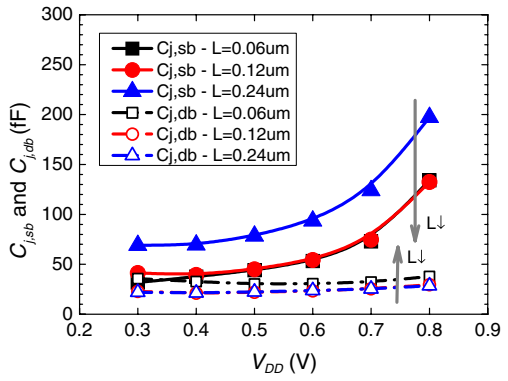


Fig. 11. (Color online) $C_{j,sb}$ and $C_{j,db}$ vs V_{DD} characteristics for DT MOSFETs with different channel lengths ($W_F/N_F/N_G$ = 1 μm/8/16).

Finally, the source- and drain-side junction capacitances ($C_{j,sb}$ and $C_{j,db}$) as well as access body resistance (R_b) versus V_{DD} are examined. In Fig. 11, $C_{j,sb}$ tends to exponentially increase as V_{DD} increases due to the nature of its forward-biased diffusion capacitance, while $C_{j,db}$ shows less bias dependence. Besides, decreasing channel length can help decrease $C_{j,sb}$, but increase $C_{j,db}$. Figure 12 shows that R_b may decrease with increasing V_{DD}, which results from the abundant positive charge supplied by the external DC source through the body contact. The figure also supports that because the shorter device has a smaller cross-section for current flowing into the body, it has larger R_b. Note that all the channel length dependences for $C_{j,sb}$, $C_{j,db}$, and R_b become weak for channel length below 0.12 μm.

5. Conclusions

In this paper, we have demonstrated the RF small-signal and noise modeling for SOI DT MOSFETs. Based on a set of simple and analytic expressions of Y-parameters, model parameters can be physically extracted, and the model has been shown to be valid up to 12 GHz.

Using our proposed extraction technique, we have compared several important parameters between DT and standard MOSFETs. Compared to the standard MOSFET, the DT MOSFET is shown to have larger g_m and smaller R_{ds} due to its lower threshold voltage and higher mobility. However, comparable R_{ds} would be observed for shorter devices because of its better suppression of short channel effect. The low threshold voltage also helps increase the channel charge and causes C_{gs} to increase. Besides, for the low-voltage regime where the DT device normally operates, our study indicates that the body transconductance g_{mb} can be neglected. Finally, with channel length scaling, the access body resistance seems to rise due to the decreasing cross section for body current to flow. The source-side junction capacitance can be minimized with channel length scaling as well.

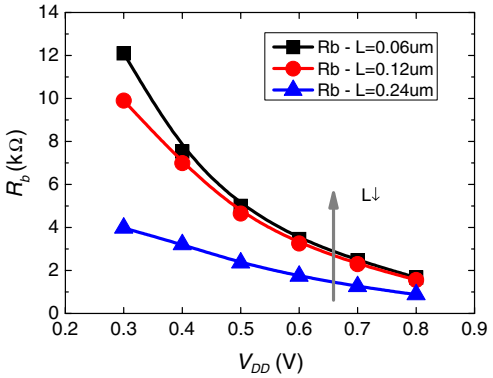


Fig. 12. (Color online) R_b vs V_{DD} characteristics for DT MOSFETs with different channel lengths ($W_F/N_F/N_G$ = 1 μm/8/16). Table I Extracted model parameters for bias condition V_{GS} = 0.8 V, and V_{DS} = 1 V ($L/W_F/N_F/N_G$ = 0.24 μm/1 μm/8/16).

Acknowledgements

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