Fully Silicided NiSi Gate on La_2O_3 MOSFETs

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***Abstract*—We have fabricated the fully silicided NiSi on La_2O_3 for n- and p-MOSFETs. For 900 °C fully silicided $CoSi_2$ on La_2O_3 gate dielectric with 1.5 nm EOT, the gate dielectric has large leakage current by possible excess Co diffusion at high silicidation temperature. In sharp contrast, very low gate leakage current density of 2×10^{-4} A/cm^2 at 1 V is measured for 400 °C formed fully silicided NiSi and comparable with Al gate. The extracted work function of NiSi was 4.42 eV, and the corresponding threshold voltages are 0.12 and −0.70 V for respective n- and p-MOSFETs. Electron and hole mobilities of 156 and 44 cm^2/V-s are obtained for respective n- and p-MOSFETs, which are comparable with the HfO_2 MOSFETs without using H_2 annealing.**

***Index Terms*—$CoSi_2$, La_2O_3, MOSFET, NiSi.**

I. Introduction

HIGH current drive capability is the main technology challenge for continuously scaling down the VLSI technology with improved MOSFET performance. To increase the drive current of MOSFET, the thickness of both inversion channel and poly gate depletion region should be decreased. Therefore, high-κ gate dielectrics [1]–[9] and metal gates [7]–[12] are required to increase the total gate capacitor density under inversion. Among various metal gates, the fully silicided poly-Si gate using $CoSi_2$ has low resistance ($\sim$ 2 $\Omega/\square$) and the potential of process compatibility with current VLSI technology [12]. In this study, we have compared the fully silicided $CoSi_2$ and NiSi gate on La_2O_3 MOSFETs. The NiSi has been applied to VLSI process for its low resistivity, low process temperature and immunity from narrow line effect. Both NiSi/La_2O_3 n- and p-MOSFETs using low temperature NiSi show much lower gate leakage current than $CoSi_2$/La_2O_3 MOSFETs and good device characteristics are evidenced from the comparable electron and hole mobilities with HfO_2 MOSFETs without H_2 annealing [2], [3].

II. Experimental

Standard 4-in p- and n-type Si wafers were used for n- and p-MOSFETs. The source and drain region were implanted with 50 KeV As^+ or 10 KeV B^+ for respective n- and p-MOSFETs, and followed by $900 \sim 950$ °C and $30 \sim 60$ s RTA. To form the La_2O_3 gate dielectric, the La film was first deposited thermally on HF-vapor passivated Si under high vacuum and followed by oxidation and annealing under low pressure condition at 425 °C [5]. An interface oxide of $0.3 \sim 0.6$ nm was found that may be due to lack of previous *in-situ* native oxide removal process [4], [5]. A formed La_2O_3 thickness of $\sim$ 5.5 nm is measured by Ellipsometer. The fully silicided gate electrode was formed by depositing 15 nm amorphous Si on La_2O_3, depositing 15 nm Ni or 10 nm Co, and followed by silicidation using RTA. For $CoSi_2$, conventional two step silicidation is used to achieve the required low resistivity: the first step silicidation was performed at 500 °C for 30 s and the second phase transformation was executed at 900 °C [13]–[15]. For NiSi, only one-step RTA at 400 °C for 30 s was performed because low resistivity silicide can be obtained at such low temperature [16]. For comparison, Al metal gate devices were also fabricated. The fabricated silicide/La_2O_3 MOSFETs were further characterized by capacitance–voltage (C-V) and current–voltage (I–V) measurements.

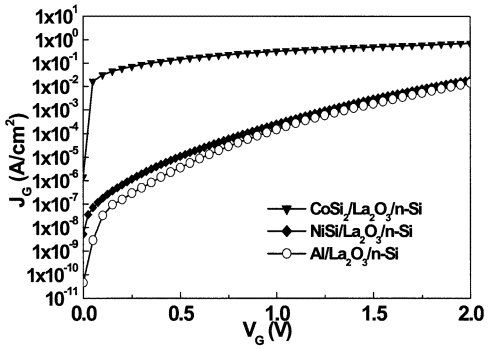

Fig. 1. J_G–V_G characteristics of NiSi/La_2O_3, Al/La_2O_3 and $CoSi_2$/La_2O_3 capacitors measured under accumulation. The large leakage current density in $CoSi_2$/La_2O_3 capacitor can not be used for device application. The device area is 100 μm× 100 μm.

III. Results and Discussion

Fig. 1 shows the comparison of gate dielectric leakage current of NiSi/La_2O_3, Al/La_2O_3 and $CoSi_2$/La_2O_3 capacitors. The large leakage current in $CoSi_2$/La_2O_3 capacitor may be due to the excess metal diffusion [17] at high silicidation temperature (900 °C) through La_2O_3 dielectric

$$L_D = (Dt)^{1/2} = D_0^{1/2} e^{-E_a/2kT} t^{1/2}. \quad (1)$$

Here, the L_D, D, t, and T are the diffusion length, coefficient, time, and temperature, respectively. The diffusion length depends on the annealing temperature exponentially, but such high temperature is required to achieve the low resistance of $CoSi_2$

Manuscript received January 24, 2003; revised March 13, 2003. This work was supported in part by the National Science Council of Taiwan, R.O.C., under Grant 90-2215-E-009-052. The review of this letter was arranged by Editor B. Yu.

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Digital Object Identifier 10.1109/LED.2003.812569

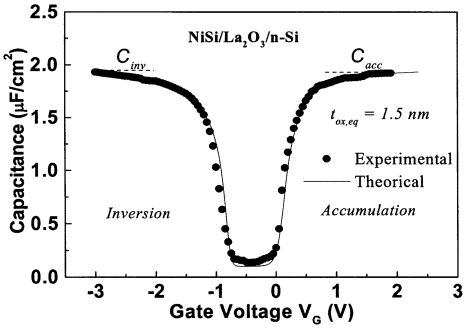


Fig. 2. C–V characteristics of NiSi/La_2O_3 transistor. The gate length is 10 μm and width is 100 μm. The measurement frequency is 100 kHz.

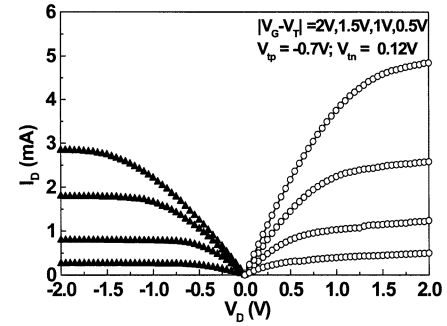
[13]–[15]. In addition, excess Co may be released during second 900 °C RTA for phase transformation from CoSi into $CoSi_2$ once underneath Si is fully consumed:

$$\mathrm{CoSi} \rightarrow \frac{1}{2}\mathrm{CoSi_2} + \frac{1}{2}\mathrm{Co}. \tag{2}$$

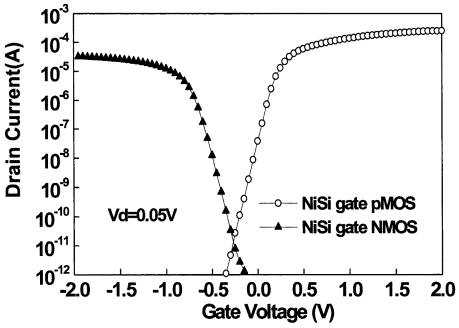
The difference between this result and previous report [12] may be due to the low metal diffusion through nitrided oxide [18]. In contrast, very low leakage current density of 2×10^{-4} A/cm^2 at 1 V is measured in fully silicided NiSi and comparable with Al gate. Besides, a low NiSi sheet resistance ($\rho_{\mathrm{NiSi}}/d_{\mathrm{NiSi}}$) of 8 $\Omega/\square$ is measured at 400 °C silicidation even at a thin NiSi thickness d_{NiSi} of $\sim$ 30 nm. Therefore, the low silicidation temperature for low resistivity NiSi is important to preserve the good gate dielectric integrity and prevent excess metal diffusion through gate dielectric.

We have further characterized the NiSi/La_2O_3 capacitor. Fig. 2 shows high frequency C–V characteristics of NiSi/La_2O_3 transistor. The identical value of inversion and accumulation capacitance indicates that the NiSi gate is fully silicided without poly-Si depletion. A relatively high interface trap density of $\sim 10^{12}$ eV^{-1}/cm^2 is measured without using previous H_2 annealing [5]. An equivalent-oxide-thickness (EOT) of 1.5 nm is obtained from the measured capacitance, which has $\sim$ 4 orders of magnitude lower leakage current than SiO_2 at the same EOT. Because excess Ni or Co must be used to avoid poly-Si depletion, the low silicidation temperature is the key step to maintain low Ni diffusion through gate capacitor and cause large leakage current. The extracted work function from the flat band voltage (V_{FB}) as a function of different La_2O_3 thickness is 4.42 eV, which is lower than the work function of Ni ($\sim$ 5 eV [10]). This result also suggests low metal diffusion into NiSi/La_2O_3 interface [17], [18] during RTA to control the work function, which is consistent with the low leakage current shown in Fig. 1.

Fig. 3(a) and (b) show the I_D-V_D and I_D–V_G characteristics of fully silicided NiSi/La_2O_3 MOSFETs, respectively. Reasonable subthreshold swing of 102 and 124 mV/dec are measured for respective n- and p-MOSFETs. The threshold voltage (V_{TH}) was further extracted from I_D–V_G plot at a $|V_D|$ of 50 mV, and V_{TH} of 0.12 and -0.70 V are obtained for n- and p-MOSFETs, respectively. The large V_{TH} for p-MOSFET may be due to the relatively small NiSi work function, because a larger work function ($\sim$ 5.6 eV [7]) is required for high-κ gate dielectric than conventional SiO_2.



(a)



(b)

Fig. 3. (a) I_D–V_D and (b) I_D–V_G characteristics of La_2O_3 ($EOT = 1.5$ nm) n- and p-MOSFETs using fully silicided NiSi gate electrode. The gate length is 10 μm and width is 100 μm.

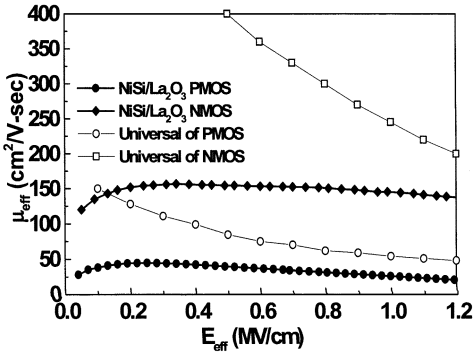


Fig. 4. Extracted electron and hole mobilities of La_2O_3 n- and p-MOSFETs using fully silicided NiSi gate electrode.

Fig. 4 shows the extracted electron and hole motilities versus gate electric field. The electron and hole mobilities for respective n-and p-MOSFETs are 156 and 44 cm^2/V-s. These mobility values are comparable with the Si_3N_4 [9] or HfO_2 MOSFETs without using H_2 annealing [2], [3], which indicates the successful integration of fully silicided NiSi gate on La_2O_3 MOSFETs. Further increasing mobility may be expected using H_2 or D_2 annealing to passivate the high-κ dielectric defects [2], [3], [5], [19].

IV. Conclusion

Good device performance of fully silicided NiSi/La_2O_3 n- and p-MOSFETs is demonstrated with a low NiSi resistance of 8 $\Omega/\square$ formed at 400 °C. In contrast, the same gate dielectric has large leakage using fully silicided $CoSi_2$ formed at a

high temperature of 900 °C. The low resistance at low temperature silicidation is the main advantage for fully silicided NiSi to avoid excess Ni diffusion through gate dielectric.

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