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Electrical properties of metal–ferroelectric–insulator–semiconductor using sol–gel derived $SrBi_2Ta_2O_9$ film and ultra-thin Si_3N_4 buffer layer

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Abstract

The electrical properties of the metal–ferroelectric–insulator–silicon memories with stacked gate configuration of Pt/$SrBi_2Ta_2O_9$ (SBT)/Si_3N_4/p-Si (1 0 0) were investigated. In an attempt to operate at low voltage with sufficient large memory window, various ultra-thin Si_3N_4 buffer layers in thickness of 3.5, 2, and 0.9 nm were employed. From the results of *C–V* measurements, the memory window can be as large as 0.8 V at the bias amplitude of 5 V for the sample with 0.9 nm Si_xN_y buffer layer. Well-crystallized perovskite structures have been further confirmed by the spectra of X-ray diffraction measurements. The leakage current, which plays a very important role in the data retention, of Pt/SBT (245 nm)/Si_3N_4 (0.9 nm)/p-Si (1 0 0) can be as low as 2.5×10^{-8} A/cm^2 at 200 kV/cm. Excellent fatigue-free performance with up to 10^{10} read/write cycles and good retention time of >2 h have been obtained. Optimization and scaling of SBT thin films are believed to be effective in pursuing extremely low voltage operation, high-density and liable 1T nonvolatile ferroelectric random access memories.
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1. Introduction

The metal–ferroelectric–insulator–semiconductor (MFIS) has been attracting much attention as a promising structure for the high-density and high-speed FET-type nonvolatile memories, which are usually denoted as FeMFET [1]. FeMFETs have several advantages over the ferroelectric random access memories with 1T1C cell structure, such as smaller cell size, simple process integration and, especially, nondestructive readout characteristic. The introduction of additional insulator in the system cannot only prevent the reaction and inter-diffusion between the ferroelectric film and silicon substrate, but also further improve the retention properties [2,3]. However, the presence of such additional insulator will distribute some voltage drop from the applied voltage, the magnitude of which depends on the capacitance ratio of the ferroelectric film and the insulator. This extra voltage drop will, therefore, result in the reduction of the electric field in the ferroelectric film and cause unfavorable non-saturated polarization behavior. Using ultra-thin Si_3N_4 insulator cannot only prevent inter-diffusion between ferroelectric film and Si substrate but also alleviate the electric field reduction issue in the MFIS structure. In this work, we employ the Pt/$SrBi_2Ta_2O_9$ (SBT)/Si_3N_4/p-Si (1 0 0) system to study the impacts of Si_3N_4 buffer layers on the electrical properties of the MFIS structures by varying the thickness of the buffer layer and ferroelectric annealing temperature.

2. Experimental

P-type (1 0 0) Si wafer was used as the starting substrate. Prior to the deposition of thin films, the Si wafer was cleaned using a Radio Corporation America method, followed by a chemical etching with diluted HF solution. The 2- and 3.5 nm-thick Si_3N_4 films were grown in SiH_2Cl_2 and NH_3 atmosphere at 780 °C by

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the low-pressure chemical vapor deposition, while the ultra-thin Si_xN_y film of ~0.9 nm was carried out by the surface nitridation in NH_3 atmosphere at 800 °C. The thicknesses of the insulators were determined using the n&k analyzer. Subsequently, the SBT films of 245 nm were deposited on the Si_3N_4/Si and Si_xN_y/Si substrates by the metal organic decomposition technique. After spin-coating of precursor solution on the SiN/Si substrate, the film was dried at 150 °C and then pyrolysized at 400 °C for 10 min in air. This process sequence was repeated 5 times until the desire thickness was obtained. Thereafter, the films were subjected to a 1-min rapid thermal annealing under an oxygen atmosphere at various temperatures for crystallization. The surface morphologies and thicknesses of the SBT films were examined by scanning electron microscopy (SEM). The film crystallinity was investigated by X-ray diffraction (XRD). In order to inspect the electrical properties of SBT thin films, 100 nm top electrode Pt was deposited by the sputtering using the shadow mask with 150, 250 and 350 μm diameters. After that, a 5 min 400 °C N_2 anneal was employed in order to form a good interface between Pt and SBT. Finally, a 500 nm back electrode Al was deposited using the thermal coater. The capacitance–voltage (C–V), current density–electric filed (J–E), fatigue, and retention characteristics were measured with a HP4284A LCR meter at a frequency of 100 kHz, HP4156A, and HP8110 function generator.

3. Results and discussion

The XRD patterns of the SBT films deposited on 2 and 3.5 nm Si_3N_4/Si and 0.9 nm Si_xN_y/Si substrate are shown in Fig. 1. The crystallization temperatures are 700, 750 and 800 °C, respectively. Clearly, strong peaks indicative of perovskite phase, such as (1 1 5) and (2 0 0) preferential orientations, have been observed. Unlike the results of the previous work [4], temperature only has a minor effect on the crystallinity of the SBT films. More importantly, even at the temperature of 700 °C, excellent crystallinity can be obtained. It seems that the incorporation of the buffer layer is helpful for crystallization in the lower temperature range. However, the thickness of the buffer layer has insignificant effect in improving the crystallinity. Fig. 2 shows the SEM images of the SBT films deposited on Si_xN_y (0.9 nm)/Si crystallized at different temperatures. The grain sizes become slightly larger with increasing annealing temperature and well-crystallized structures have been observed. Fig. 3 shows the capacitance–voltage (C–V) characteristics of the MFIS capacitors, in which SBT was annealed at 750 °C, where the measuring frequency was 100 kHz. The voltage was swept from +5 to −5 V and then reversed. The clockwise traces in the C–V hysteresis curves are clearly observed. It means that split of C–V curves in two opposite polarity is due to

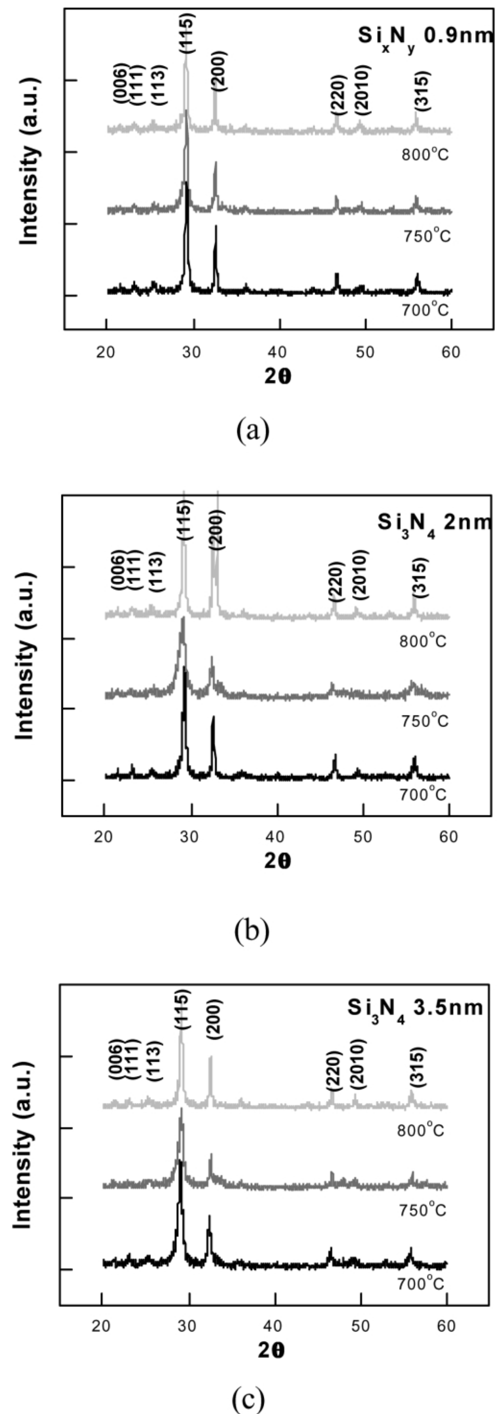
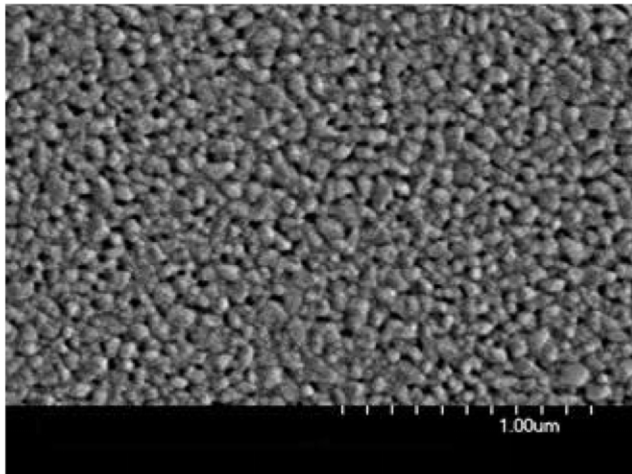
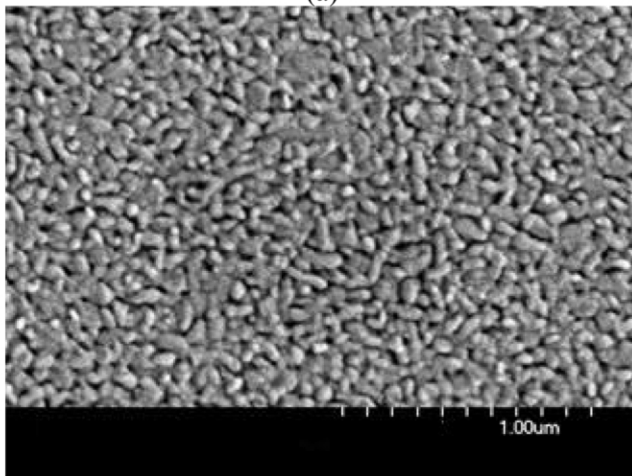


Fig. 1. XRD patterns of the SBT films deposited on (a) 0.9 nm Si_xN_y/Si; (b) 2 nm and (c) 3.5 nm Si_3N_4/Si substrates. The annealing temperatures vary from 700 to 800 °C.

the polarization of the SBT films, not caused by injection charge effect [3,5]. The hysteresis window widths for the MFIS capacitors with 0.9-, 2- and 3.5 nm-thick SiN buffer layer are 0.8, 0.5 and 0.6 V, respectively. Surface nitridation is more effective than thin SiN layers in improving the memory window. The rapid changes of



(a)



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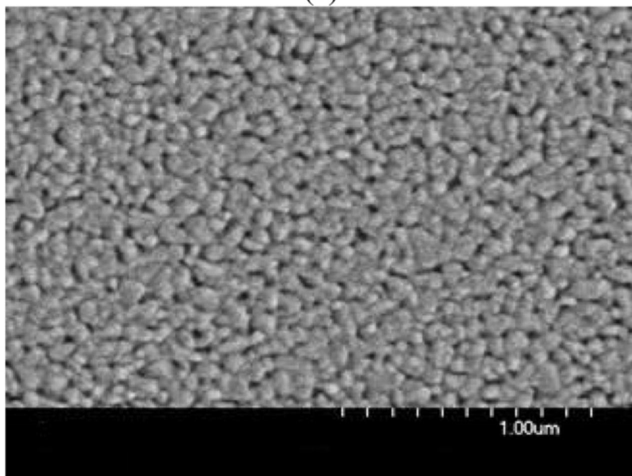


(c)

Fig. 2. SEM images of SBT films deposited on Si_xN_y (0.9 nm)/Si with (a) 700 °C; (b) 750 °C; (c) 800 °C annealing.

the capacitances in the depletion region indicate good interface properties have been achieved at the interface of the substrate and SiN buffer layers [3]. To evaluate

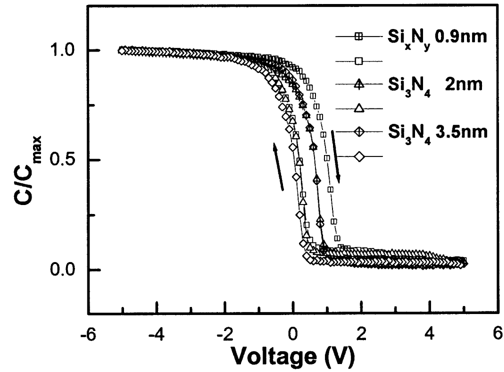
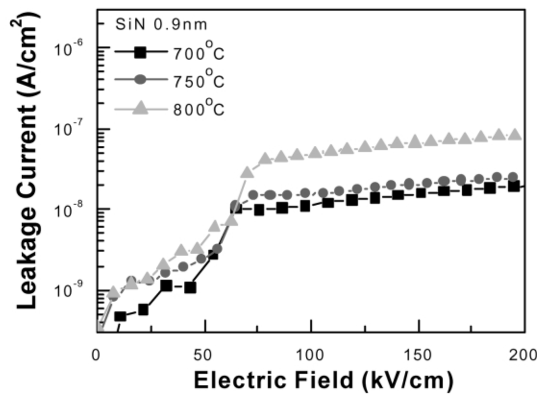
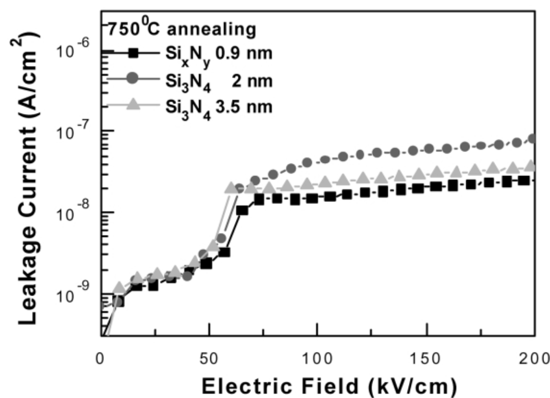


Fig. 3. Normalized capacitance–voltage $(C–V)$ characteristics of MFIS structures, in which SBT was annealed at 750 °C, measured at 100 kHz with a voltage sweep from $+5$ to -5 V and reverse.

the annealing temperature and insulator thickness effects on leakage mechanism of the Pt/SBT/insulator/Si capacitors, current density vs. electric field $(J–E)$ characteristics are measured in accordance with the annealing temperature and insulator thickness, as shown in Fig. 4. Fig. 4a shows the leakage current densities of the MFIS capacitors annealed at various temperatures. The magnitudes of current density are 1.8×10^{-8}, 2.5×10^{-8}, and 8.5×10^{-8} A/cm^2 at 200 kV/cm for the samples annealed at 700, 750 and 800 °C, respectively. Leakage current increases with increasing temperature. This is due to the larger grain size in higher temperature, which has been observed in the SEM results (Fig. 2). Larger grain size is likely to lead to rougher interface between SBT and Si_xN_y. Locally enhanced electric field could exist and, therefore, induce larger leakage current [2]. Fig. 4b shows the leakage current densities of the MFIS capacitors with different thicknesses of buffer layers. The magnitudes of current density are 2.5×10^{-8}, 7.7×10^{-8}, and 3.6×10^{-8} A/cm^2 at 200 kV/cm for the samples with 0.9-, 2-, 3.5 nm-thick SiN, respectively. Surface nitridation obviously suppresses the lowest leakage current even though its thickness is thinnest. It is speculated that surface nitridation forms denser films and smoother interfaces, than nitride reactive deposition. Thus, the MFIS capacitor with 0.9 nm Si_xN_y buffer layer can depict the lowest current density. While the leakage current densities of the capacitors with SiN layers are found to increase as the thickness of buffer layer decreases. This is consistent with the conventional effect of insulator thickness on the electrical properties of the system. The retention performance is shown in Fig. 5. The retention of a MFIS capacitor was measured by applying the writing pulses of ±5 V in height and 2 ms in duration, and then reading capacitance at a voltage of 0.5 V every 20 min for 2 h. It is found that the retention is strongly correlated to the magnitude of leakage current density through the stacked gate insulator. The capacitor with a 0.9 nm-thick Si_xN_y buffer layer,



(a)



(b)

Fig. 4. (a) Annealing temperature effects on leakage mechanism of the Pt/SBT/0.9 nm Si_xN_y/Si capacitors; (b) insulator thickness effects on leakage mechanism of the Pt/SBT/insulator/Si capacitors.

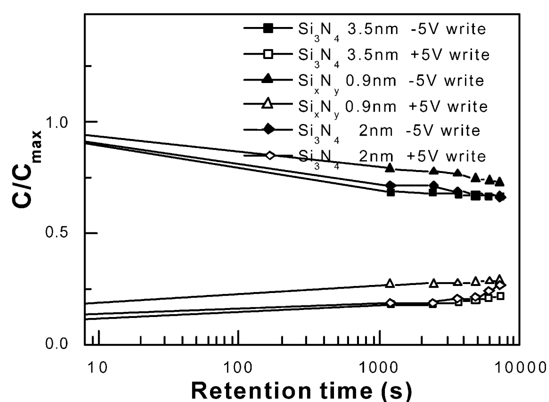


Fig. 5. Retention performances of the MFIS capacitors.

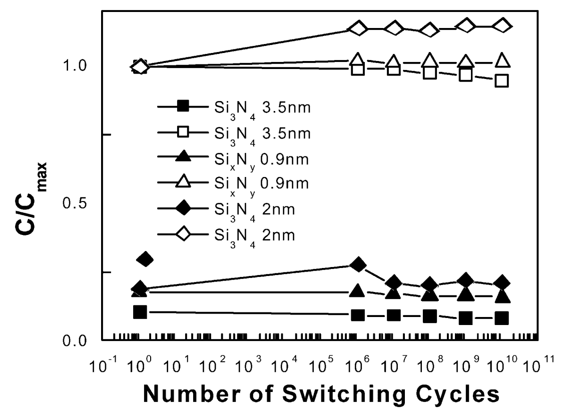


Fig. 6. Fatigue properties of the MFIS with various thickness insulators as a function of switching cycles of ±5 V in height and 1 MHz in frequency.

which has the lowest leakage current density, also exhibits the best retention performance. The fatigue properties of the MFIS capacitors with various insulators were also measured. Fig. 6 shows both accumulation and depletion capacitance readings at 0.5 V as a function of switching cycles. The amplitude of the bipolar pulse train is ±5 V in height and the frequency is 1 MHz. It can be clearly seen that all the capacitors demonstrate excellent nearly fatigue-free performance up to 10^{10} cycles as exhibited in SBT thin films.

4. Conclusion

Using SiN as buffer layer can lower the crystallization temperature of the SBT thin films down to 700 °C with only 1 min annealing. It has been proven with the strong peaks indicative of perovskite phases in the X-ray patterns. The memory window of 0.8 V can be achieved at voltage sweep ±5 V. The leakage current of the capacitor with the configuration of Pt/SBT (245 nm)/ Si_3N_4 (0.9 nm)/p-Si (1 0 0) can be as low as 2.5×10^{-8} A/cm² at 200 kV/cm. It was also found that the fabricated MFIS capacitors exhibit long retention performances and fatigue-free characteristics up to 10^{10} switching cycles.

Acknowledgments

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