RF Noise in 0.18-μm and 0.13-μm MOSFETs

C. H. Huang, C. H. Lai, J. C. Hsieh, J. Liu, and Albert Chin, *Senior Member, IEEE*

***Abstract*—We have studied the gate finger number and gate length dependence on minimum noise figure ($NF_{\min}$) in deep sub-micrometer MOSFETs. A lowest $NF_{\min}$ of 0.93 dB is measured in 0.18-μm MOSFET at 5.8 GHz as increasing finger number to 50 fingers, but increases abnormally when above 50. The scaling gate length to 0.13 μm shows larger $NF_{\min}$ than the 0.18-μm case at the same finger number. From the analysis of a well-calibrated device model, the abnormal finger number dependence is due to the combined effect of reducing gate resistance and increasing substrate loss as increasing finger number. The scaling to 0.13-μm MOSFET gives higher $NF_{\min}$ due to the higher gate resistance and a modified T-gate structure proposed to optimize the $NF_{\min}$ for further scaling down of the MOSFET.**

***Index Terms*—MOSFET, noise, RF, scaling trend, 0.13 μm.**

I. Introduction

AS CONTINUOUSLY scaling down the VLSI technology, the RF gain of deep sub-micrometer MOSFET is improved so that it can be used for wireless communication. However, it is still not clear what the dependence of the scaling trend is on RF noise that limits the noise floor of an RF system. It is known that the noise figure (NF) of current Si RF ICs is still larger than the GaAs counterpart, but the excess noise in Si ICs may come from the passive devices [1] that can be largely suppressed by using ion implantation processes developed by us [1]–[4]. Therefore, further reduction of noise in Si RF ICs close to GaAs depends on optimizing the active MOSFETs. In this paper, we have used multifingered layout and device scaling to optimize the RF noise in deep sub-μm MOSFETs. A lowest minimum NF ($NF_{\min}$) of 0.93 dB is reached in 0.18-μm MOSFET as increasing finger number to 50, but shows abnormal increase as finger number >50. The scaling to 0.13-μm MOSFETs gives larger $NF_{\min}$ than 0.18-μm devices at the same gate finger number. The abnormal finger dependence analyzed by a self-consistent dc, NF, and S-parameter model is due to the tradeoff between decreasing gate resistance (R_g) and increasing substrate loss [1]–[4] as increasing finger number. The gate length dependence is due to the increasing R_g as scaling down from 0.18 to 0.13 μm. However, the larger finger number will consume more device area and power that are opposite to the VLSI scaling trend. Besides, the current-gain cut-off frequency (f_T) may also be degraded due to the increasing parasitic gate–body capacitance (C_{gb}) used for contact. Thus, further scaling down of the MOSFETs will generate larger noise unless a modified T-gate MOSFET structure is used.

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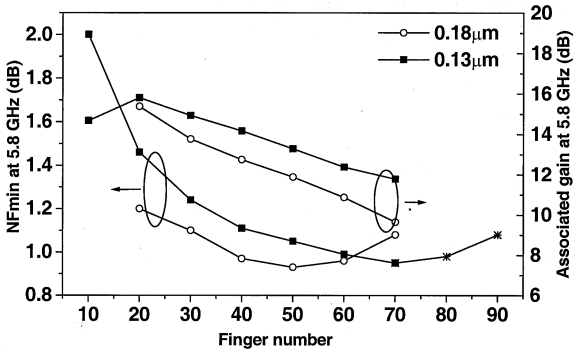

Fig. 1. $NF_{\min}$ and associated gain at 5.8 GHz of 0.18- and 0.13-μm MOSFETs. The $NF_{\min}$ for gate finger number >70 are obtained from simulation using the well-calibrated device model.

II. Experimental Procedure

To optimize the $NF_{\min}$ of MOSFETs, we have used multi-fingered layout and scaled gate length from 0.18 to 0.13 μm, where the finger number is from 10 to 70 with 5-μm finger width. This 5-μm finger width is chosen by trading off reducing R_g and increasing parasitic C_{gb} used for silicide gate–metal contact. Because the f_T equals $g_m/2\pi(C_{gs}+C_{gb})$, the use of too short a finger width with too many finger numbers will increase the C_{gb} and reduce the f_T. The fabricated MOSFETs are first characterized by dc I–V measurements. Then, standard S-parameters are measured up to 20 GHz using a HP8510B network analyzer and on-wafer probes, de-embedded from the probe pad. The $NF_{\min}$ and associate gain are measured using ATN-NP5B Noise Parameter Extraction System up to 7.2 GHz that covers the most important frequency range for wireless communication.

III. Results and Discussions

Fig. 1 shows the finger and gate length dependence on measured $NF_{\min}$ and the associate gain at 5.8 GHz for 0.13- and 0.18-μm MOSFETs. It is noticed that when scaling down the MOSFET from 0.18 m to 0.13 μm, the associate gain increases but also gives higher $NF_{\min}$ that is highly undesired. A lowest $NF_{\min}$ of 0.93 dB is obtained in 0.18-μm MOSFETs with 50 fingers, which is close to or better than the data published in the literature [5]–[10] and compatible with GaAs HEMTs [11]. The $NF_{\min}$ in 0.13-μm MOSFETs decreases monotonically while increasing gate fingers to 70, and a similar trend of decreasing $NF_{\min}$ while increasing fingers is also found in 0.18-μm MOSFETs, but shows an abnormal increase as finger number >50.

To understand such abnormal dependence on gate finger and length, we have used a self-consistent dc, NF, and S-param-

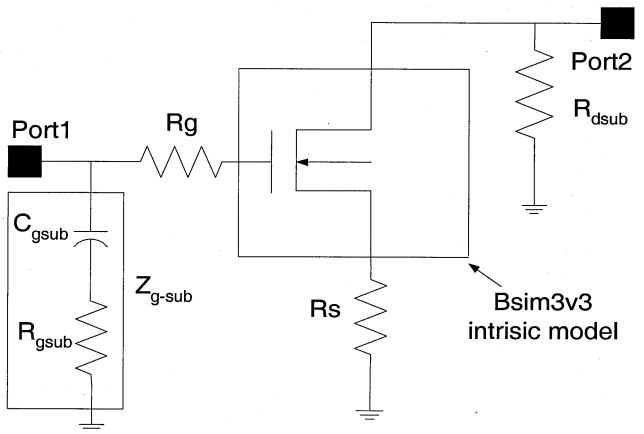

Fig. 2. Equivalent circuit model for 0.18- and 0.13-μm MOSFETs.

eter equivalent circuit model shown in Fig. 2 to simulate the devices and extract the important parameters. The device model contains an intrinsic BSIM3v3 model, additional R_g to gate, and additional shunt impedances to simulate the substrate loss. The suitability of this equivalent circuit model is examined from the good agreement between measured and modeled data shown below.

Fig. 3(a)–(c) shows the measured and simulated I_D–V_D characteristics, S-parameters up to 20 GHz, and $NF_{\min}$ up to 7.2 GHz of 0.13-μm MOSFETs with the largest finger number of 70. Good agreements between simulated and measured dc I_D–V_D, S-parameters, and $NF_{\min}$ are obtained for 0.13 μm MOSFETs with 70 fingers. Similar good agreements between measured and modeled dc I_D–V_D, S-parameters, and $NF_{\min}$ are also obtained in other finger numbers of 0.13-μm MOSFETs and all finger numbers of 0.18-μm MOSFETs (not shown). The good agreement between measured and modeled data for various gate finger numbers and gate length indicate the excellent accuracy of the equivalent circuit model that can be further used for device parameter extraction [3], [10].

Because the RF signal is input fromthe gate and amplified after passing though the output drain terminal, the dominant noise source is fromthe gate input terminal. This is because the noise in an amplification system is due to following equation [12]:

$$NF_T = NF_1 + \frac{NF_2 - 1}{G_1} + \cdots + \frac{NF_N - 1}{G_1 G_2 \ldots G_{N-1}}.$$

Thus, the noise of the system with amplification is governed by the input stage, where G_i is the gain of each stage amplifier. Fig. 4 shows the dependence of extracted R_g and gate substrate loss impedance (Z_{g-sub}) on gate fingers. A decreasing gate resistance as increasing finger number is observed is due to the parallel effect and explains the decreasing $NF_{\min}$ as the increasing finger number. From our device simulation, the reason for abnormally increasing $NF_{\min}$ when gate finger $>$50 in 0.18-μm MOSFETs is due to the decreasing Z_{g-sub} because of the large area-related substrate loss. The higher R_g in 0.13-μm MOSFETs also explains the higher $NF_{\min}$ while decreasing the gate length from 0.18 to 0.13 μm because of

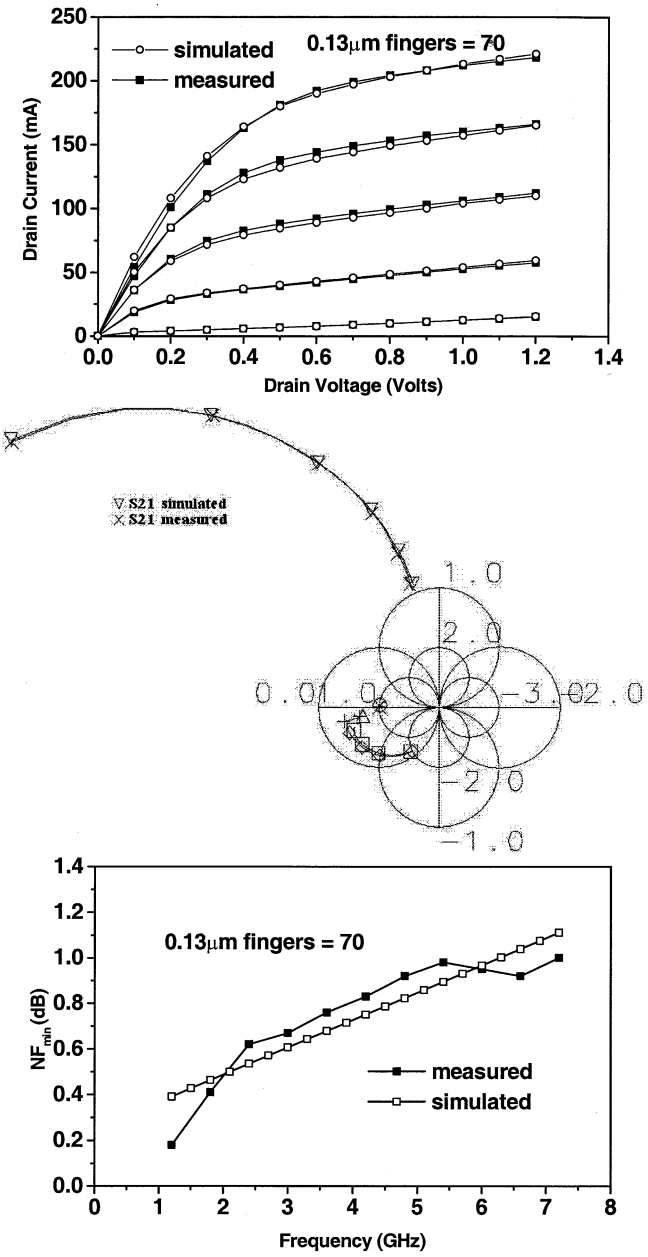

Fig. 3. The simulated and measured (a) dc I_D–V_D characteristics, (b) S-parameters, and (c) $NF_{\min}$ of 0.13-μm MOSFETs with the largest 70 fingers.

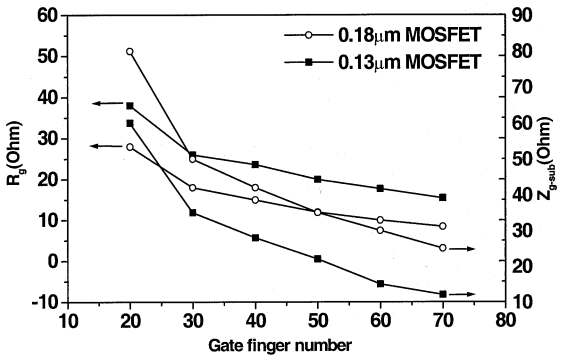

Fig. 4. Dependence of the gate finger number onthe gate resistance R_g and substrate loss impedance Z_{g-sub} of 0.18- and 0.13-μm MOSFETs.

the smaller gate area. From the extrapolated data of 0.13-μm MOSFETs and the well-calibrated device model, similar increasing noise figure after increasing gate finger >70 is also obtained, as shown in Fig. 1. This sets the upper limit of the increasing gate finger even without considering the device area and power consumption. Therefore, further scaling down the gate length will give a higher $NF_{\min}$ even though the associate gain is increased, unless a modified T-gate MOSFET structure is used.

IV. Conclusion

We have found a strong dependence of $NF_{\min}$ on a layout finger number and gate length that is due to the combined effect of R_g and substrate loss effect. A T-gate structure is necessary to reduce the RF noise for further scaling down the MOSFETs.

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