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Degradation of passivated and non-passivated N-channel low-temperature polycrystalline silicon TFTs prepared by excimer laser processing

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Abstract

The instability mechanisms of passivated and non-passivated low-temperature polycrystalline silicon thin film transistors (LTPS TFTs) under various bias stress conditions have been investigated. Irrespective of plasma treatment, the degradation was more severe under negative gate bias stress than that under positive gate bias stress. This could be due to Fowler–Nordheim tunneling electron induced impact ionization. For hot carrier stress, TFTs with NH_3 plasma treatment degraded more severely than those without plasma treatment. This might be attributed to collapsing of weak Si–H bonds in NH_3-plasma passivated devices. For the high current stress, it showed the opposite results against hot carrier stress. © 2002 Elsevier Science Ltd. All rights reserved.

Keywords: Poly-Si TFT; Excimer laser; Instability; Bias stress; Plasma treatment

1. Introduction

Polysilicon thin film transistors (TFTs) are widely used in many applications such as loading elements in SRAMs and addressing components in active matrix liquid crystal displays (AMLCD's). It is well known that the grain boundaries exert a profound influence on device characteristics. Therefore, hydrogen plasma passivation is performed to minimize the defect density in polysilicon films and to improve the electrical characteristics of TFTs. Recently, plasma passivation with different gas sources, such as N_2, H_2/N_2, NH_3, N_2O, has been reported in the literature [1,2]. Some of them exhibit better passivation efficiency than pure H_2 plasma treatment, and others have better hot carrier reliability and thermal stability. This is attributed to the passivation effects of other atom plasma radicals in addition to hydrogen themselves. Although all of them exhibit significant improvement of device performance, they are usually confined to high-temperature (>600 °C) processed poly-Si TFTs, and the passivation mechanisms remain relatively unclear.

In this paper, the effects of NH_3 plasma passivation on low-temperature poly-Si (LTPS) TFTs were studied. In order to investigate the effect of the plasma treatment, TFTs were stressed under various bias stress conditions. In addition, different instability mechanisms between plasma passivated and non-passivated N-channel poly-Si TFTs were found as well.

2. Experimental

Poly-Si TFTs were fabricated on thermally oxidized 4-in. (1 0 0) n-type silicon wafers. First, a 50-nm-thick

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amorphous silicon (α-Si) was initially deposited at 550 °C by low-pressure chemical vapor deposition (LPCVD). Then, the amorphous thin film were irradiated at optimum energy density by using a KrF excimer laser with approximately 25-ns pulse duration. A homogenizer was used to produce a 1.8×23.1 mm^2 laser spot onto the sample. The laser beam scanned over the surface of the sample with 95% overlap between successive shots in order to compensate for the lack of pulse-to-pulse reproducibility.

After definition of the active regions, a 50-nm-thick gate dielectric was deposited by using PECVD with TEOS/O2 mixture at 300 °C. Another 250-nm-thick amorphous silicon film was deposited by LPCVD at 550 °C, and patterned to form the gate electrode. A self-aligned phosphorus ion implantation at 40 keV with a dose of 5×10^{15} cm^{-2} was used to dope the drain, source, and gate areas simultaneously and then activated by a 20 h annealing at 600 °C in N_2 ambient in furnace. Next, some of the samples were then subjected to 4 h NH_3 plasma treatment in a parallel-plate plasma reactor at 300 °C with a power density of 0.7 W/cm^2. The plasma condition for NH_3 plasma treatment was optimized for device performance. After a 500-nm-thick SiO_2 was deposited by PECVD, contact holes for drain/source and gate electrode were formed. Finally, Al was deposited and defined for probing pads and the completed devices were sintering at 350 °C. The process flow of the device fabrication was shown in Fig. 1.

I–V characteristics of the polysilicon TFTs were measured by using a HP 4156 semiconductor parameter analyzer. The subthreshold swing SS and field effect mobility μ_{FE} were calculated at $V_d = 0.1$ V. The threshold voltage V_t was defined at a fixed drain current $I_d = I_{dn} \times W/L$, where I_{dn} was a normalized drain current, 10 nA. I_{min} was the minimum value of the drain current measured at $V_d = 5$ V. The on-state drain current I_{on} was defined as the drain current at $V_g = 15$ V and $V_d = 5$ V.

3. Results and discussion

Table 1 shows the all stress conditions for instability testing of the TFTs. For the positive and negative gate bias stresses, the 20 and −20 V of gate bias voltages with common grounded S/D electrode were applied for 10,000 s. For hot carrier stress, 10 V gate bias and 20 V drain-to-source bias were applied. As for high current

Table 1
Various stress conditions used in the experiments

Positive bias stress	Negative bias stress	Hot carrier stress	High current stress
$V_g = 20$ V	$V_g = -20$ V	$V_g = 10$ V	$V_g = 20$ V
$V_d = V_s = 0$ V	$V_d = V_s = 0$ V	$V_{ds} = 20$ V	$V_{ds} = 10$ V
10^4 s	10^4 s	10^3 s	10^3 s

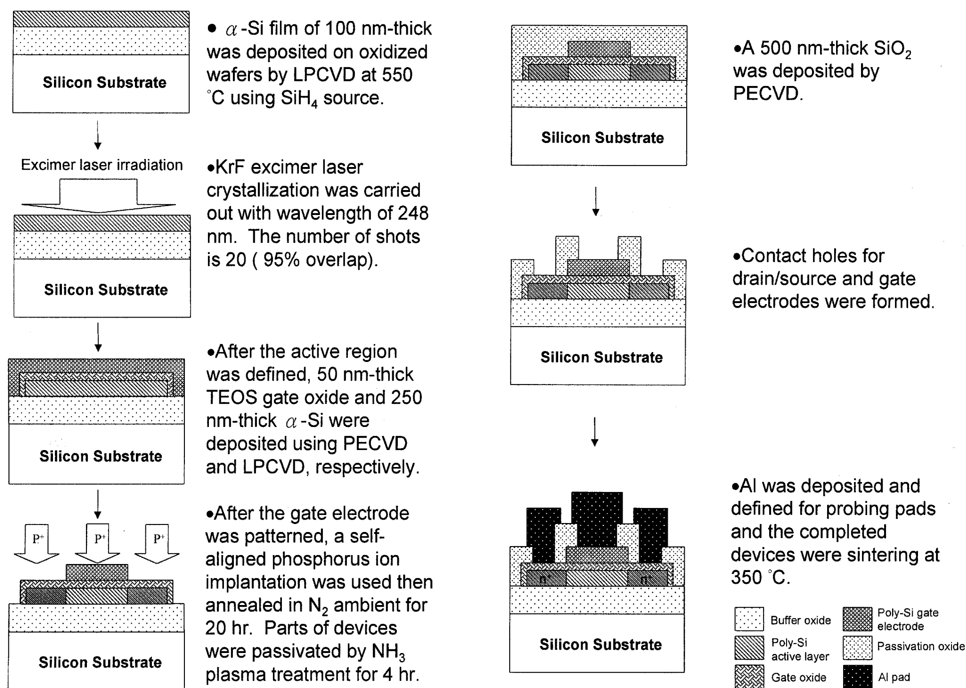


Fig. 1. The process flow of the top gate polysilicon thin film transistors used in our measurement.

stress, 20 V gate bias and 10 V drain-to-source bias were applied. Both hot carrier stress and high current stress were treated for 1000 s. Fig. 2(a) and (b) present the transfer curves of TFTs without plasma passivation and with NH_3-passivation under positive gate bias stress for different stress time. The TFTs with NH_3-passivation exhibit superior device characteristics to TFTs with no passivation. For positive gate bias stress, both passivated and non-passivated curves show that the on current decreases with increase of the stress time. This can be attributed to negative oxide charges and bulk states creation [3]. For positive gate bias stress, F–N tunneling electron induced impact ionization occurs near the gate region away from the channel. Positive oxide traps induced by stressing are near poly-Si gate electrode while negative oxide traps are near channel region. As a result, the threshold voltage shift is dominated by the negative oxide charges. Channel states are also created by positive gate bias stress, but are much fewer than those created by negative gate bias stress because most impact ionization induced by high energy electrons occurs at poly-Si gate electrode. In addition, depassivation induced hydrogen positive ions may diffuse into the channel and passivate channel states [4]. This is the reason that the NH_3-passivated TFTs have better performance. Fig. 3(a) and (b) show the transfer curves of TFTs without plasma passivation and with NH_3-passivation under negative gate bias stress for different stress time. Compared to positive gate bias stress devices, TFTs under negative gate bias stress show severe degradation. This can be explained from F–N tunneling electron induced impact ionization. Under negative gate bias stress, the electrons in poly-Si gate electrode will tunnel to channel region and generate electron-hole pairs accompanied with states at channel region. The generated hot holes at the channel region may be trapped into the oxide near the channel region, while some electrons may be trapped in the oxide near the poly-Si gate electrode. For NH_3-passivated TFTs under negative gate bias

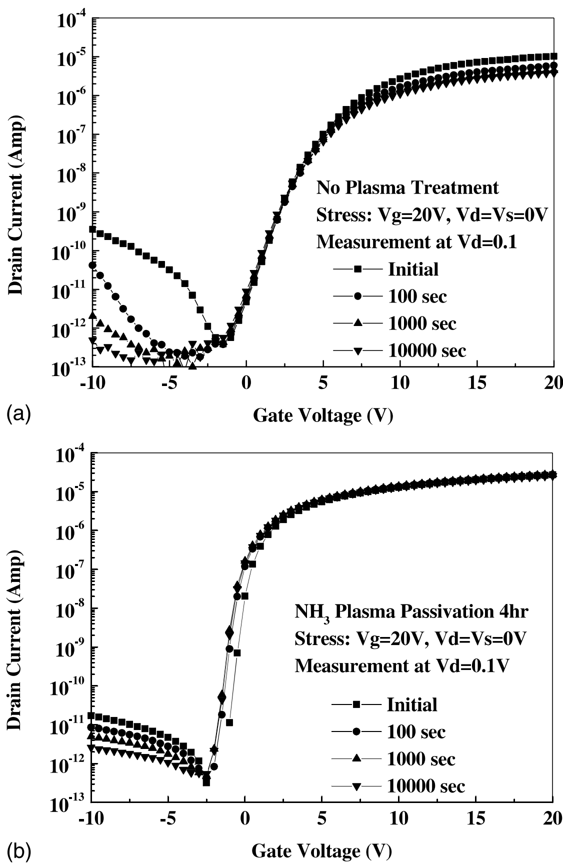


Fig. 2. (a) Transfer characteristics of non-passivated TFTs for $V_d = 0.1$ V measured at different times of 20 V gate bias stress, (b) transfer characteristics of NH_3-passivated TFTs for $V_d = 0.1$ V measured at different times of 20 V gate bias stress.

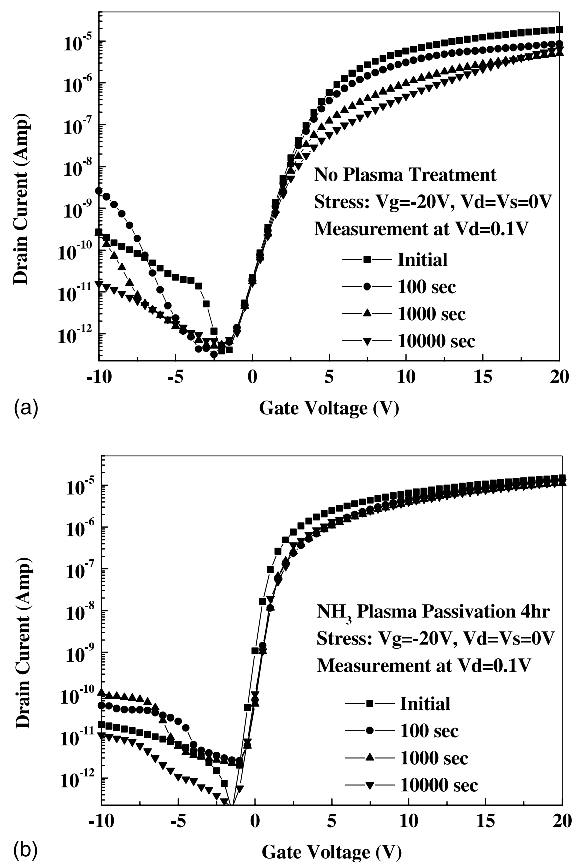
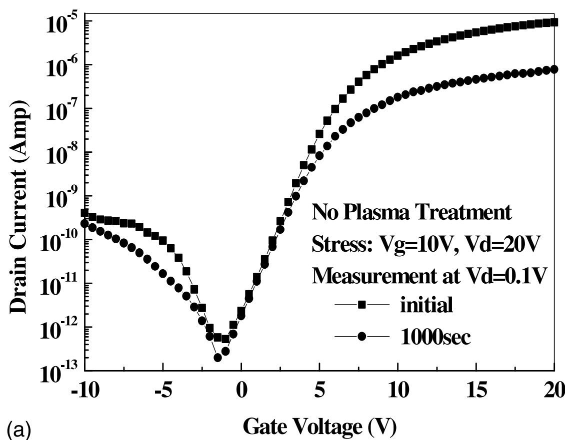


Fig. 3. (a) Transfer characteristics of non-passivated TFTs for $V_d = 0.1$ V measured at different times of -20 V gate bias stress, (b) transfer characteristics of NH_3-passivated TFTs for $V_d = 0.1$ V measured at different times of -20 V gate bias stress.

stress, the degradation can also be due to the abundance of weak Si–H bonds in NH_3 plasma-treated devices [5].

The instability of poly-Si TFTs under the hot carrier stress and the high current stress is shown in Figs. 4 and 5. For the hot carrier stress, the characteristics of plasma passivated TFTs are degraded more severely than the non-passivated ones. The degradation is caused by holes trapped in oxide and state creation in the bulk or at the poly-Si/SiO_2 interface, as weak Si–H or Si–Si bonds are broken by "hot" electrons. For NH_3-passivated poly-Si films, it could also be the trap state creation due to the bond breaking of Si–N. For the high current stress, the results are different from TFTs under hot carrier stress. The degradation of NH_3 plasma treatment is slighter because the conducting electrons have lower energy in the high current stress mode than electrons in the hot carrier stress mode. Only the Si–Si weak bonds are broken so this makes less created states in the channel. Another possible reason is that states created by high current flow are passivated by H^+ and N^+ ion drifting from oxide to poly-Si channel due to the favor of the electric field. These results are summarized in Table 2. This is the result of the instability of poly-Si TFTs under the hot carrier stress and the high current stress. Under hot carrier stress, TFTs with NH_3-passivation were degraded severely both in threshold voltage shift and subthreshold swing. However, under hot current stress, TFTs with NH_3-passivation shows less degradation than non-passivated TFTs.



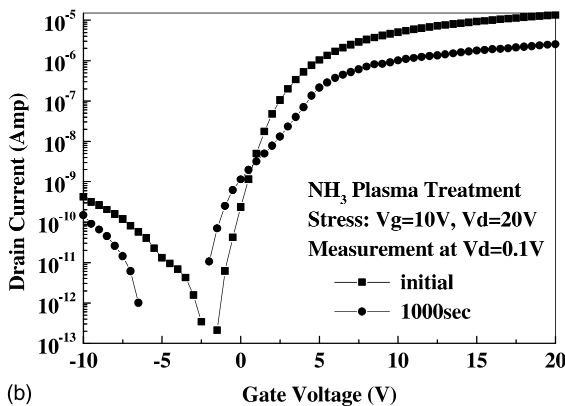
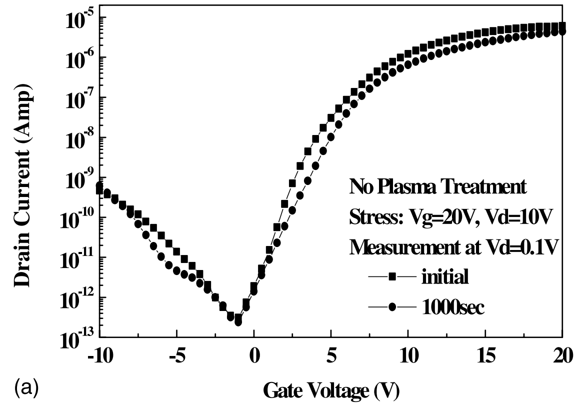


Fig. 4. Transfer characteristics of (a) non-passivated TFTs, (b) NH_3-passivated TFTs, before and after 1000 s hot carrier stress.



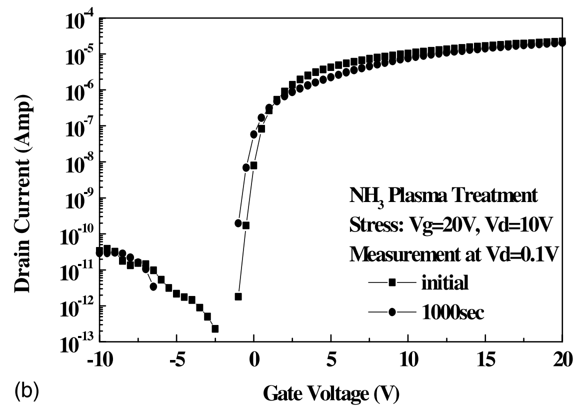


Fig. 5. Transfer characteristics of (a) non-passivated TFTs, (b) NH_3-passivated TFTs, before and after 1000 s high current stress.

Table 2
Instability of poly-Si TFTs stressed at hot carrier and high current stress

Plasma treatment	ΔV_{th} (V)		ΔS (V/dec)		Δg_m (nS)	
	Non	NH_3	Non	NH_3	Non	NH_3
Hot carrier stress	0.703	1.457	0.23	1.107	−768	−681
High current stress	0.814	0.032	0.231	0.005	−195	−14

4. Conclusions

The instability mechanisms of passivated and non-passivated LTPS TFTs under various bias stress conditions have been investigated. TFTs with NH_3 passivation exhibit superior electrical characteristics to their counterparts with no passivation. For positive and negative gate bias stresses, the on current decreases with increase of the stress time. The degradation was more severe under negative gate bias stress than that under positive gate bias stress. This could be due to Fowler–Nordheim tunneling electron induced impact ionization. Under hot carrier stress, TFTs with NH_3 plasma treatment exhibits inferior stress endurance compared to those with non-treated TFTs despite better initial electrical characteristics. For the high current stress, the degradation of NH_3 plasma treatment is slighter because the conducting electrons have lower energy compared to electrons under hot carrier stress. The NH_3-passivation process is of potential use for the fabrication of TFT/LCDs.

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