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Application of Field-Induced Source/Drain Schottky Metal-Oxide-Semiconductor to Fin-Like Body Field-Effect Transistor

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A novel Schottky barrier silicon-on-insulator (SOI) metal-oxide-semiconductor field effect transistor (MOSFET) device was proposed and demonstrated. The new device features a silicide source/drain and field-induced source/drain (S/D) extensions. Excellent ambipolar performance with a near-ideal sub-threshold slope ($\sim$ 60 mV/decade) and high on-/off-state current ratio (comparable to or higher than 10^9) is realized, for the first time, on a single device. These encouraging results suggest that the new device may be suitable for some niche applications requiring simple and low-temperature processing of complementary metal-oxide-semiconductor (CMOS)-like devices. [DOI: 10.1143/JJAP.41.L626]

KEYWORDS: Schottky barrier, ambipolar, silicon-on-insulator (SOI), silicide, electrical junction

A Schottky barrier metal-oxide-semiconductor (SB-MOS) transistor[1)] has been proposed for future nanoscale device applications.[2)] The device features more simple and low-temperature processing compared to conventional MOS transistors, by employing metal silicide, in lieu of a heavily-doped region, as the source/drain (S/D). However, the SB-MOS transistor fabricated on bulk silicon wafer using the conventional self-aligned structure, i.e., gate and S/D separated by oxide sidewall spacers, suffers from an intolerably high leakage current at the Schottky junction. For example, an on/off current ratio as low as 30 for SB-MOS devices with a channel length of 40 nm was previously reported.[3)] To reduce the deleterious leakage current, SB-MOS transistors were fabricated on silicon-on-insulator (SOI) wafers.[4–8)] Significant improvements of device characteristics in terms of reduced off-state leakage and low sub-threshold slope have been demonstrated.[4)]

Another approach to reducing the leakage current in SB-MOS transistor is the use of a field-induced junction.[9)] The device features a metal field-plate (or sub-gate) lying over the offset channel region near the drain. When a suitable fixed voltage is applied to the sub-gate, an electrical junction is induced in the offset channel. We have demonstrated that such a structure is very effective in suppressing the field emission of carriers from the drain junction to the channel[10,11)] during the off-state operation, so that the off-state leakage becomes almost independent of the bias between the gate and the drain.[9–11)] Moreover, depending on the polarity of the sub-gate bias, unique ambipolar operation capability is realized.

This approach was first demonstrated on poly-Si thin-film transistors (TFTs).[9–12)] More recently, ambipolar SB SOI devices with a channel length of 1.4 μm have also been reported.[12)] An excellent on-/off-state current ratio ($> 10^7$) was achieved. In this work, we present the ambipolar characteristics of a new SB MOS device with field-induced source/drain (S/D) extensions on three sides of the conduction channel. An extremely high on-/off-state current ratio ($> 10^8$) and nearly ideal sub-threshold slope (60 mV/decade) for both n- and p-channel operations are demonstrated, for the first time, in a single device.

Figure 1 shows the key process flow and device structure. E-beam lithography was employed for device patterning. Six-inch p-Si separation by implanted oxygen (SIMOX) wafers

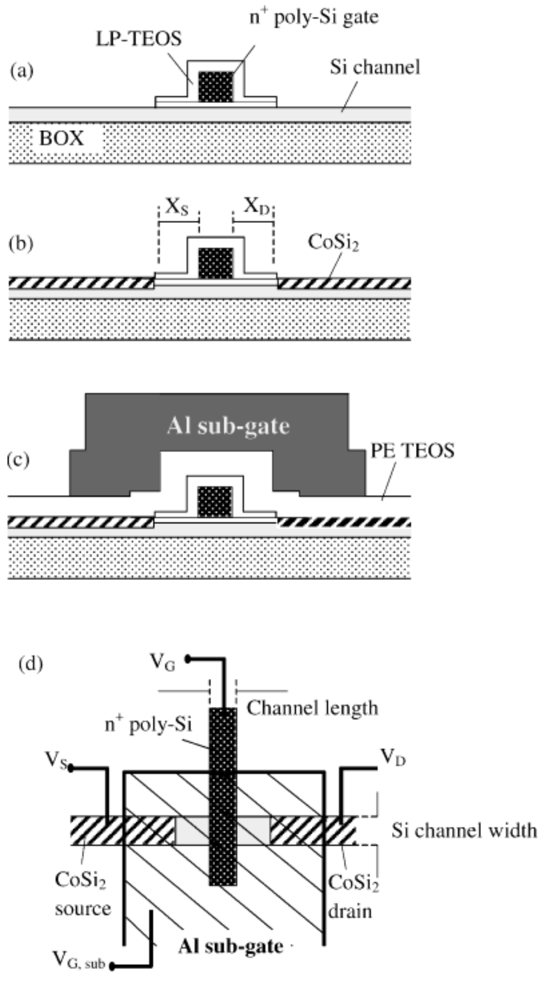

Fig. 1. (a)–(c) Cross-sectional views of the device after some key process steps, and (d) top view of the device's central portion.

with background doping of approximately 5×10^{15} cm^{-3} were used as the starting substrates. The active Si device layer was thinned to 80 nm by thermal oxidation. After device island (including S/D contact and Si channel regions) patterning, gate oxide (2.2 nm) and *in situ* doped n^+ poly-Si (150 nm) films were deposited. Gate electrodes were then defined and patterned using plasma etching with high poly-Si/oxide etch selectivity (> 100). An low pressure tetra-ethyl-ortho-silicate

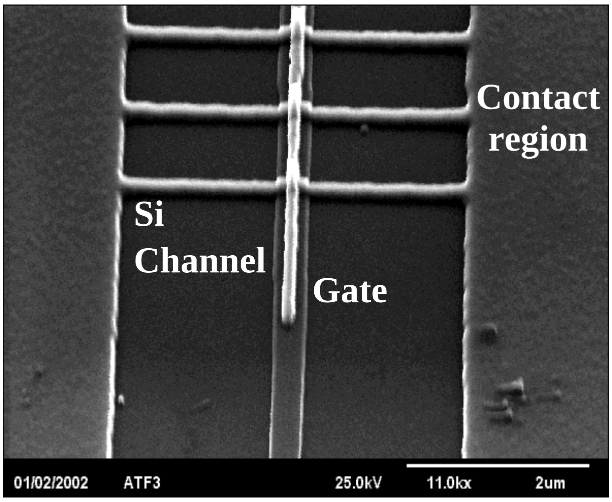

Fig. 2. SEM image of a fabricated device with three fins before silicide step (Fig. 1(a)).

(LP-TEOS) (20 nm) layer was then deposited and etched to define the offset (i.e., source/drain extension) regions (Fig. 1(a)). A Co silicide process was subsequently applied to form $CoSi_2$ in the S/D regions (Fig. 1(b)). Next, a 40-nm-thick plasma-enhanced TEOS layer was deposited, followed by contact hole and Al pad/sub-gate formation (Fig. 1(c)). It is worth noting that no implantation step was used in the process. The top view of the device's central portion is shown in Fig. 1(d). A scanning electron microscope (SEM) image of a fabricated sample is shown in Fig. 2. The offset length on both source and drain sides (X_S and X_D in Fig. 1(b)) of the devices reported here is fixed at 100 nm, and the spacing between the gate and the S/D contact region was 2 μm (Fig. 1(b)).

Note that, as the channel width is scaled down to less than 100 nm, the new device becomes similar to the double-gate FinFET reported previously.[13] In fact, the new device actually has a triple-gate structure,[14] i.e., both the top and sidewall surfaces of the Si film underneath the main gate serve as a conduction channel, since no hard mask was employed on the Si channel. As a result, the effective channel width should be the sum of the Si channel width (Fig. 1(d)) and twice of the Si thickness (80 nm).

Figure 3 depicts the ambipolar sub-threshold and output characteristics of devices with channel length $L = 470$ nm. The Si channel width is 50 nm in Fig. 3(a) and 2 μm in Fig. 3(b), respectively. $V_{G.\,sub}$ is fixed at 7.5 V for n-channel operation, and -7.5 V for p-channel operation. The sub-gate biases were chosen to be high enough to realize a sufficient on/off current ratio, and low enough not to jeopardize the underlying dielectric reliability. When a high sub-gate bias is applied, the tunneling barrier width at the source junction is significantly reduced,[15] as is the contact resistance of the Schottky junction. As a result, the on current will be significantly increased. It was also found that the sub-threshold slope is not significantly affected if the applied sub-gate bias is sufficiently large (data not shown), consistent with results of a previous study[16] which investigated the effect of sub-gate bias on the operation of an n-channel MOSFET. This indicates that the electrical junctions induced by the sub-gate become part of the source/drain during device operation. More detailed results regarding the effect of sub-gate bias on the device operation

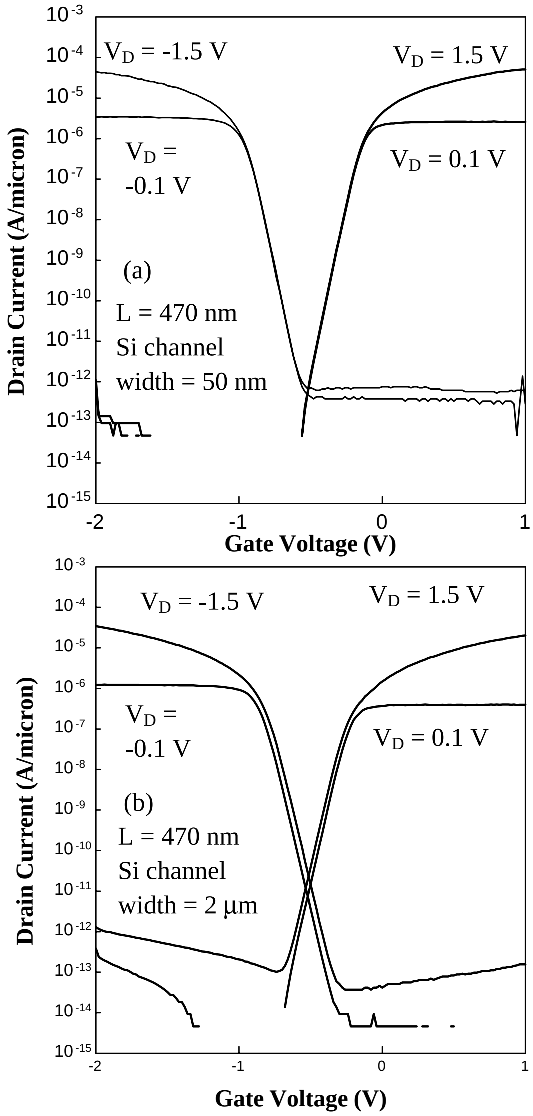

Fig. 3. Ambipolar sub-threshold characteristics of SB FinFET devices with channel width of (a) 50 nm, and (b) 2 μm. $|V_{G.\,sub}|$ is fixed at 7.5 V.

will be reported elsewhere.[17]

Our experimental results show that an extremely high on/off current ratio (comparable to or higher than 10^9) could be achieved in the new devices. For the device with a Si channel width of 50 nm, the sub-threshold slope is 60.6 mV/decade for n-channel operation, and 60.8 mV/decade for p-channel operation. These values are close to the ideal case, *e.g.*, 60 mV/decade. To the best of our knowledge, such superior ambipolar characteristics on a single device have never been achieved before.

When the Si channel width is increased to 2 μm, as shown in Fig. 3(b), the sub-threshold slope increases to around 66 and 67 mV/decade for n- and p-channel modes, respectively. In addition, the drain-induced barrier lowering (DIBL) effect ($\sim$40 mV) becomes apparent. This trend is further highlighted in Fig. 4, in which the sub-threshold slope is shown as a function of channel width. It can be seen that the sub-threshold slope increases with the Si channel width, consistent with the trend previously reported for MOS FinFET devices.[13] This indicates that when the Si channel is scaled down to the nanometer regime, the ultrathin body of the de-

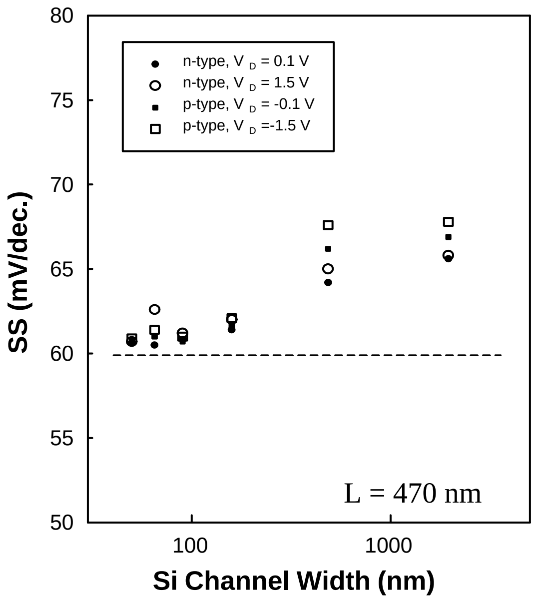

Fig. 4. Sub-threshold slope (SS) as a function of the fin width.

vice effectively prevents the S/D punch-through.

It should be noted that the on currents shown in Fig. 3 are not high, primarily due to the use of Co silicide which has a high barrier height for both electrons and holes. Optimum silicide materials with low barrier height, *e.g.*, ErSi for n-channel and PtSi for p-channel operation,[4,8] could further enhance the performance of each specific operation mode. I_D could also be further improved by reducing the offset length (Fig. 1(b)) and the spacing between the gate and the S/D contact region (Fig. 2).

The proposed Schottky-Barrier SOI device is very simple in terms of fabrication and requires no implantation or associated annealing steps. Also, it is capable of bi-channel operation, which is unique, noteworthy, and greatly simplifies complementary metal-oxide-semiconductor (CMOS) integration. Excellent device performance in terms of a near-ideal subthreshold slope and high on/off current ratio (comparable to or higher than 10^9) is demonstrated, suggesting that such a device is potentially useful for a number of CMOS-like device applications.

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1) M. P. Lepselter and S. M. Sze: Proc. IEEE **56** (1968) 1400.
2) J. R. Tucker, C. Wang and P. A. Carney: Appl. Phys. Lett. **65** (1994) 618.
3) C. Wang, J. P. Snyder and J. R. Tucker: Appl. Phys. Lett. **74** (1999) 1174.
4) J. Kedzierski, P. Xuan, E. H. Anderson, J. Bokor, T. J. King and C. Hu: IEDM Tech. Dig. (2000) p. 57.
5) M. Nishisaka and T. Asano: Jpn. J. Appl. Phys. **37** (1998) 1295.
6) W. Saitoh, A. Itoh, S. Yamagami and M. Asada: Jpn. J. Appl. Phys. **38** (1999) 6226.
7) M. Nishisaka, Y. Ochiai and T. Asano: 56th Annual Device Research Conf. Dig., Virginia, 1998, p. 72.
8) M. Nishisaka and T. Asano: Jpn. J. Appl. Phys. **37** (1998) 1295.
9) H. C. Lin, C. Y. Lin, K. L. Yeh, R. G. Huang, M. F. Wang, C. M. Yu, T. Y. Huang and S. M. Sze: IEDM Tech. Dig. (2000) p. 857.
10) H. C. Lin, K. L. Yeh, R. G. Huang, C. Y. Lin and T. Y. Huang: IEEE Electron Device Lett. **22** (2001) 179.
11) H. C. Lin, K. L. Yeh, R. G. Huang, T. Y. Huang and S. M. Sze: IEEE Trans. Electron Devices **49** (2002) 264.
12) K. L. Yeh, H. C. Lin, R. G. Huang, R. W. Tsai and T. Y. Huang: Appl. Phys. Lett. **79** (2001) 635.
13) D. Hisamoto, W. C. Lee, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. J. King, J. Bokor and C. Hu: IEEE Trans. Electron Devices **47** (2000) 2320.
14) J.-P. Colinge: *SOI Technology: Materials to VLSI* (Kluwer Academic Publishers, Boston, 1997) 2nd ed.
15) B. Winstead and U. Ravaioli: IEEE Trans. Electron Devices **47** (2000) 1241.
16) H. Noda, F. Murai and S. Kimura: IEDM Tech. Dig. (1993) p. 123.
17) H. C. Lin, M. F. Wang, F. J. Ho, J. T. Liu, F. H. Ko, H. L. Chen, G. W. Huang, Y. Li, T. Y. Huang and S. M. Sze: to be published in the 60th Annual Device Research Conf. Dig., Santa Barbara, 2002.