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Characteristics of $Pb(Zr_{0.53}Ti_{0.47})O_3$ on Metal and Al_2O_3/Si Substrates

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We have fabricated $Pb(Zr_{0.53}Ti_{0.47})O_3$ on Pt and $Pb(Zr_{0.53}Ti_{0.47})O_3$ on 4 nm Al_2O_3/Si substrates. Although $Pb(Zr_{0.53}Ti_{0.47})O_3$ on Pt has a larger dielectric constant and grain size than those on Al_2O_3/Si, the $Pb(Zr_{0.53}Ti_{0.47})O_3$ thin films on both substrates show good capacitance-voltage characteristics and the same threshold voltage shift of ~3.6 V. Moreover, the leakage current density of $Pb(Zr_{0.53}Ti_{0.47})O_3$ on Al_2O_3/Si at −10 V is nearly three orders of magnitude lower than that of $Pb(Zr_{0.53}Ti_{0.47})O_3$ on Pt. The comparable memory characteristics and the lower leakage current of $Pb(Zr_{0.53}Ti_{0.47})O_3$ on Al_2O_3/Si are important for continuous scaling down the ferroelectric memory.
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Ferroelectric random access memory (FRAM) using hysteresis characteristics of ferroelectric materials has the advantages of higher speed and lower power consumption than Flash memory and electrically erasable-programmable read-only memory (EEPROM).[1] Currently, the cell structure of FRAM is one-transistor and one capacitor (1T1C), and the ferroelectric thin films are deposited on metal to form a metal/ferroelectric/metal (MFM) capacitor structure.[2-8] On the other hand, one transistor (1T) ferroelectric metal oxide semiconductor field effect transistor (FeMOSFET) type memory is very attractive because it has not only the same small 1T cell structure as Flash memory but also the merits of FRAM mentioned above. Furthermore, the leakage current in a capacitor of 1T1C cell may limit further shrinkage because the thinner ferroelectric dielectric, smaller area, and hence the higher capacitance/area are the general scaling trends for memory. Therefore, 1T FeMOSFET is a highly desirable device for the next generation memory. However, little progress has been achieved in 1T FeMOSFET memory because ferroelectric materials must be integrated as a gate dielectric to form the metal/ferroelectric/Si (MFS), but the strong interface reaction between most ferroelectric materials and Si degrades the device characteristics.[9] In this paper, we have integrated $Pb(Zr_{0.53}Ti_{0.47})O_3$ (PZT) on Si using Al_2O_3[10,11] as both interface reaction barrier between PZT and Si and gate dielectric for MOSFET. We have compared PZT on Al_2O_3/Si with PZT on metal and the nearly three orders magnitude of lower leakage current is another advantage of the MFS structure using PZT on Al_2O_3/Si.

Experimental

Four inch, p-type Si(100) wafers were used in this study with a typical resistivity of 10 Ω cm. For the MFM structure, 150 nm Pt was first deposited on 20 nm Ti/200 nm SiO_2/Si by E-beam evaporation, which was used as the bottom electrode. For the fabrication of MFS structure, 4 nm Al_2O_3 gate dielectric was formed on Si following our previously reported procedure.[10,11] The typical dielectric constant and bandgap of Al_2O_3 are 9.5 and 8.8 eV, respectively. Then PZT ferroelectric thin films were deposited on both $Pt/Ti/SiO_2/Si$ and Al_2O_3/Si by chemical solution deposition method using multiple spin coating at 4000 rpm for 30 s. For the chemical solution synthesis, lead acetate trihydrate, zirconium isopropoxide, and titanium isopropoxide were used as precursors and dissolved in the solvents composed of acetic acid and methanol in sequence.[12] The advantages of chemical solution deposition used in this study are the simplicity and the accuracy of composition control. The Zr/Ti ratio of PZT was chosen to be 53/47, that is, near the morphotropic phase boundary. After each coating the wet films were pyrolyzed at 450°C for several minutes and the multiple-layer films were annealed at 700°C for 1 h. Au was used as the upper electrode for both capacitor structures with area of 5×10^{-4} cm^2, and Al the bottom electrode was used for MFS capacitor at the bake side of the Si substrates. We used X-ray diffraction (XRD) to determine the phase and the crystallinity of PZT. The surface morphology and the thickness of PZT were observed by atomic force microscopy (AFM) and secondary electron microscopy (SEM), respectively. Capacitance-voltage (C-V) and current density-voltage (J-V) characteristics were measured to check the electric properties of ferroelectric PZT.

Results and Discussion

Figures 1a and b show the XRD patterns of PZT films deposited on Pt and 4 nm Al_2O_3/Si, respectively. The thickness of each PZT film is determined from the cross-sectional SEM images, to be 250 nm. As shown in Fig. 1a, the structure of PZT on $Pt/Ti/SiO_2/Si$ is polycrystalline without a preferred orientation which is the typical XRD spectra for PZT on Pt electrode. The high Pt peak intensity in Fig. 1a suggests that Pt has a polycrystalline structure, and this is quite different from the amorphous Al_2O_3 structure on Si. As shown in Fig. 1b, the structure of PZT on Al_2O_3 is also polycrystalline, and the PZT film has the stable ferroelectric perovskite phase rather than the nonferroelectric pyrochlore phase. The full width at half-maximum (fwhm) for the main peaks of PZT on Pt and Al_2O_3 are 0.30 and 0.35°, and the relative peak intensity is 1.2 times higher for PZT on Pt than PZT on Al_2O_3. Thus, although the Al_2O_3 gate dielectric is only 4 nm, high quality ferroelectic PZT is still successfully produced in this process.

We have used AFM to study the microstructures of deposited PZT. As shown in Fig. 2a, the PZT film deposited on Pt has a grain size of 100 nm that is larger than the grain size of 65 nm for PZT deposited on Al_2O_3/Si shown in Fig. 2b. The reason for polycrystalline PZT on Pt with larger grain size than on Al_2O_3 is because polycrystalline PZT may be more easily nucleated on polycrystalline Pt than on amorphous Al_2O_3. The roughness of PZT on Pt is 4.48 nm that is also larger than 1.96 nm of PZT on Al_2O_3/Si. The larger rms roughness of PZT on Pt is due to the larger polycrystalline grains of PZT formed on polycrystalline Pt instead of amorphous Al_2O_3.

C-V characteristics at 1 MHz were further measured to study the electrical properties of PZT on Pt and Al_2O_3 buffered Si. Figure 3a shows C-V characteristics of PZT films on Pt and the C-V curves with a typical butterfly pattern because of the ferroelectric nature of PZT.[13,14] Although the C-V curves are slightly asymmetric, a large peak voltage difference of 3.59 V is obtained after ±10 V applied bias that is due to the ion shift by the electric field. This large memory window is important for memory device design rather than symmetric concern. Figure 3b shows C-V characteristics of PZT

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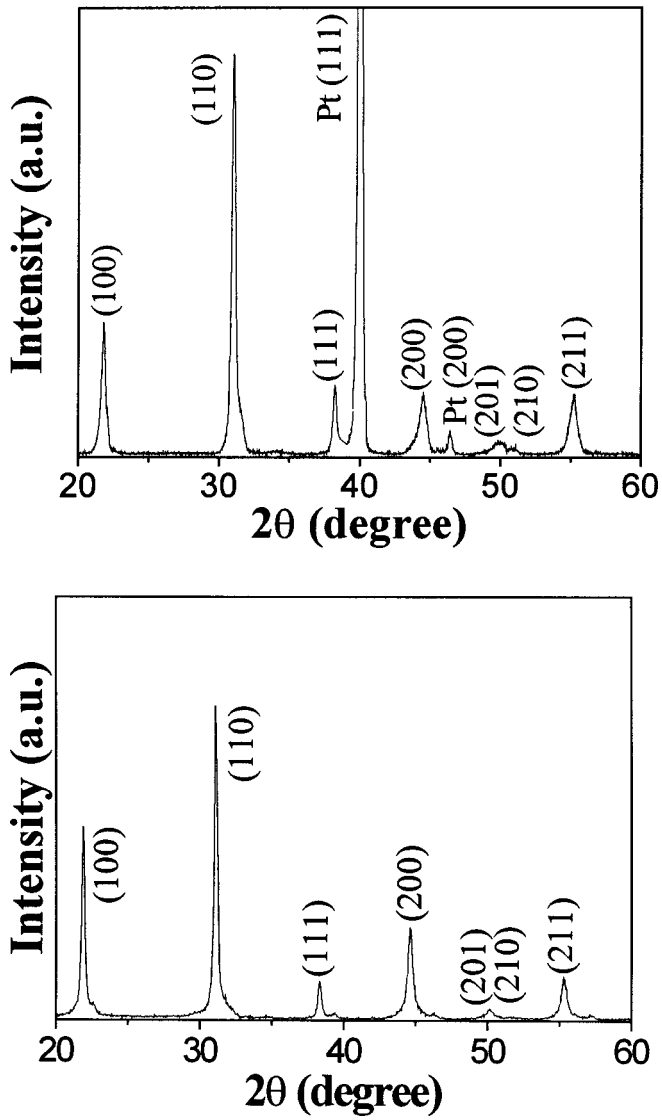

Figure 1. XRD patterns of 250 nm PZT on (a, top) $Pt/Ti/SiO_2/Si$ and (b, bottom) 4 nm Al_2O_3/Si.

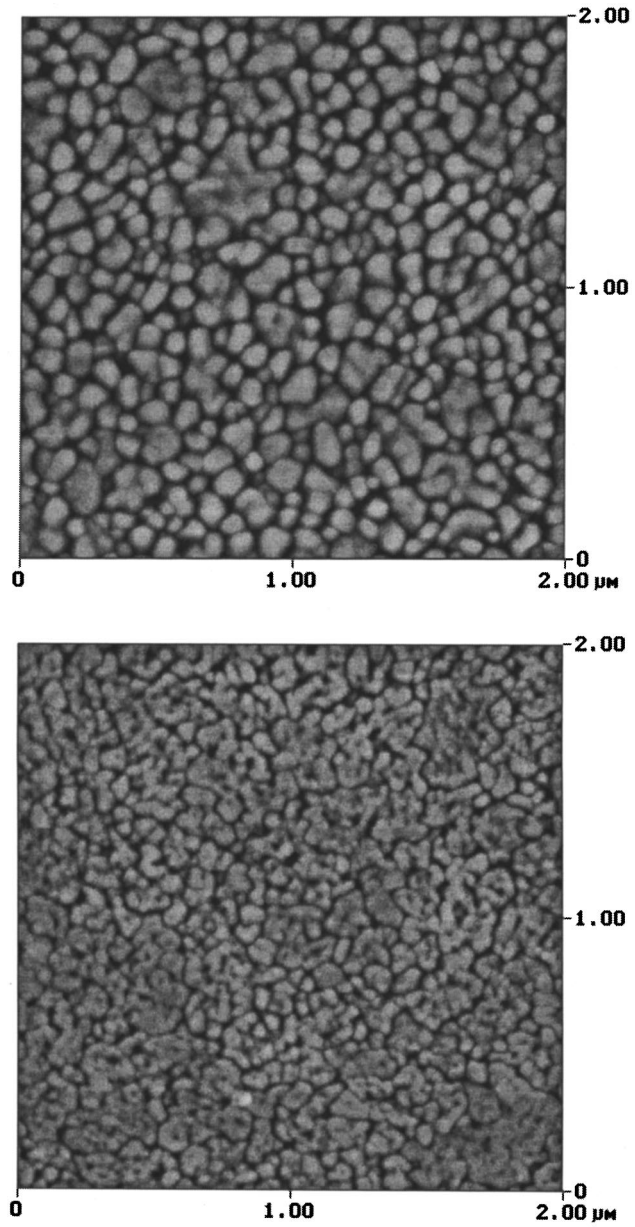

Figure 2. AFM images of 250 nm PZT on (a, top) $Pt/Ti/SiO_2/Si$ and (b, bottom) 4 nm Al_2O_3/Si.

films on Al_2O_3/Si. The hysteresis in C-V curves is due to the ferroelectric properties of PZT, which is negligible in Al_2O_3 gate dielectric.[10,11] The small capacitance value at positive gate bias shown in Fig. 3b is due to the small series capacitance in the Si depletion region. However, there is no such effect on the MFM structure shown in Fig. 3a because of the negligible depletion width of the metal. Besides the voltage drop in Al_2O_3 gate dielectric, the threshold voltage shift (ΔV_T) measured in PZT on Al_2O_3/Si is 3.6 V that is almost the same as that in MFM case shown in Fig. 3a. The higher threshold voltage shift is important because it will give a large memory window. Because the threshold voltage shift is directly related to the electric field in PZT (E_{PZT}), we have therefore solved the E_{PZT} of the stacked gate PZT/Al_2O_3 as

$$E_{PZT} = V_g \Big/ \left(d_{PZT} + \frac{\varepsilon_{PZT}}{\varepsilon_{Al_2O_3}} d_{Al_2O_3} \right) \qquad [1]$$

where ε is the dielectric constant and d the thickness of thin films. This equation is from the electric field continuity in PZT and Al_2O_3 by the relation

$$E_{Al_2O_3} = E_{PZT} \frac{\varepsilon_{PZT}}{\varepsilon_{Al_2O_3}} \qquad [2]$$

According to Eq. 1, a smaller dielectric constant or a thinner thickness of PZT will increase E_{PZT} in our stacked gate structure and hence increase the memory window. The large memory window for PZT on Al_2O_3/Si is due to the relative by smaller dielectric constant of 121 obtained from C-V, which is lower than that of 515 for PZT on Pt. The large dielectric constant in the MFM capacitance may be due to the larger grain size of ferroelectric films shown in Fig. 2a. We have also studied the thickness-dependent memory effect. Figure 3c shows a thicker 420 nm PZT on Al_2O_3/Si stacked gate dielectric. A small memory window of only 2 V is obtained for the same ± 10 V applied voltages, and the small gate capacitance of 60 pF is also not desirable for MOSFET application.

We have also investigated the capacitor leakage current because it is one of the important properties of capacitors. Figure 4a and b

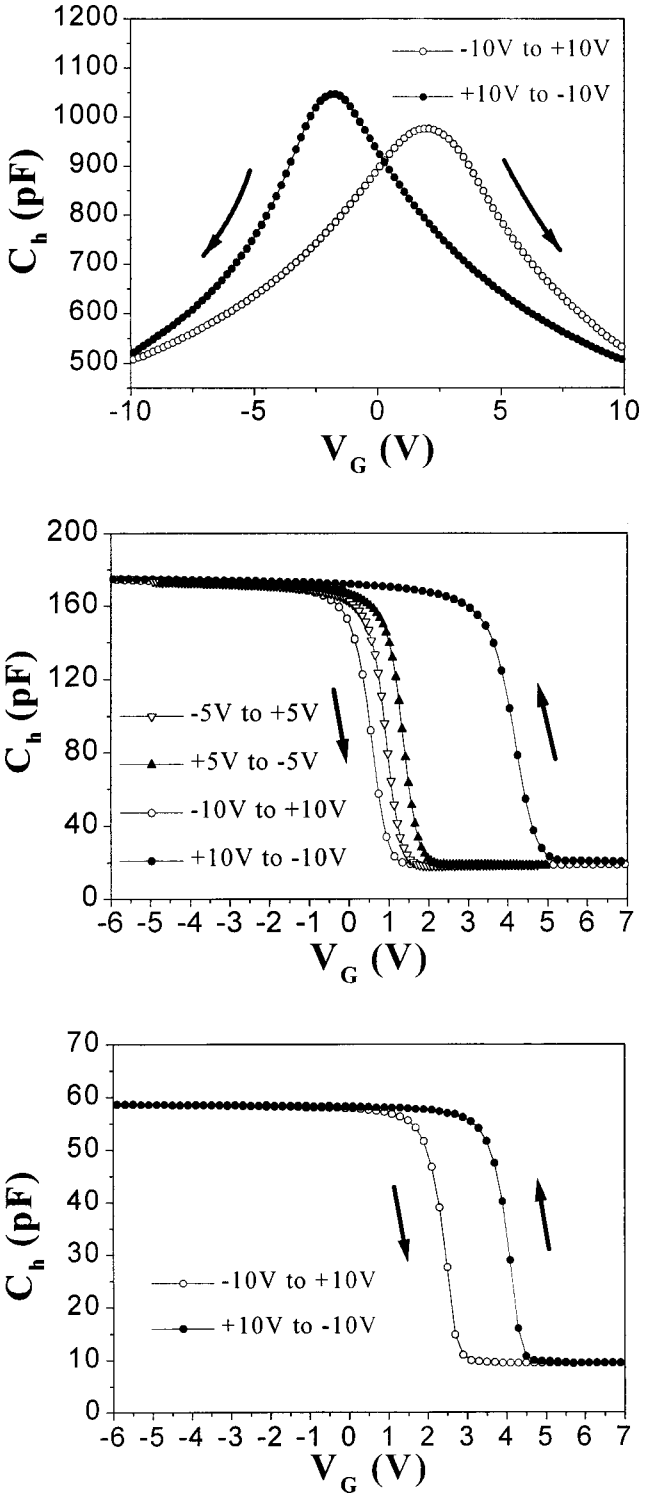

Figure 3. C-V curves of (a, top) 250 nm PZT on Pt/Ti/SiO_2/Si, (b, center) 250 nm PZT on 4 nm Al_2O_3/Si, and (c, bottom) 420 nm PZT on 4 nm Al_2O_3/Si.

show leakage current density-voltage (J-V) characteristics in MFM and MFS structures, respectively. The leakage current density of PZT on Pt is 1.0×10^{-5} A/cm^2 at -10 V that is comparable to the previously reported data.[15] A high breakdown electric field of 1.2×10^6 V/cm also suggests the good PZT quality. In contrast, the leakage current density of PZT on Al_2O_3/Si is only 3.1×10^{-8} A/cm^2 at -10 V that is nearly three orders of magnitude

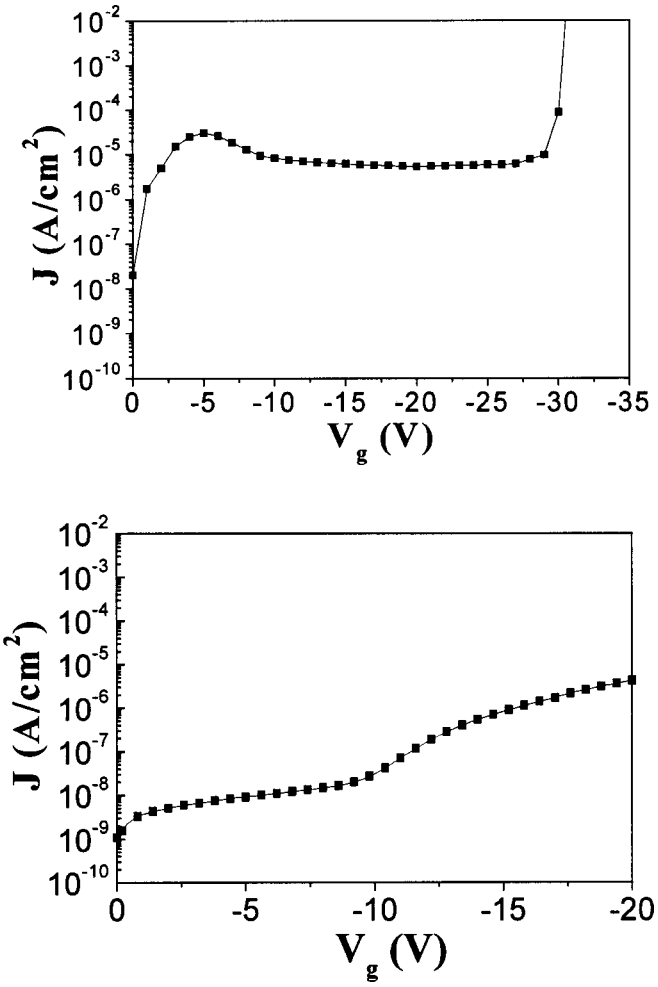

Figure 4. J-V curves of 250 nm PZT on (a, top) Pt/Ti/SiO_2/Si and (b, bottom) 4 nm Al_2O_3/Si.

lower than that in the MFM structure. Because the dielectric leakage current is the well known Fowler-Nordheim (F-N) tunneling at high field, the smaller leakage current is due to the additional large bandgap Al_2O_3 gate dielectric[10] because of the exponential dependence of F-N tunneling current on the bandgap

$$J = \frac{q^3 E_D^2}{16\pi^2 \hbar \phi_D m_D^*} \exp\left(-\frac{4(2m_D^*)^{0.5}\phi_D^{3/2}}{3\hbar q E_D}\right) \quad [3]$$

where E_D, m_D^*, and ϕ_D are the dielectric electric field, effective mass, and barrier height, respectively.

Table I summarizes the comparison of PZT on Pt and Al_2O_3/Si. The advantages of PZT on Al_2O_3/Si are the smaller leakage current, smoother surface, and comparable memory window with PZT on Pt. The relatively lower dielectric constant is desirable for PZT in a stacked gate dielectric because the larger electric field will drop on PZT which will in turn give a larger memory window. The successful integration PZT on Al_2O_3 without an interface reaction is important for further 1T FeMOSFET development.[16,17]

Conclusions

We have compared PZT on Pt and 4 nm Al_2O_3/Si substrates. Both MFM and MFS capacitors show good capacitance-voltage characteristics and almost the same threshold voltage shift of 3.6 V. The PZT/Al_2O_3/Si further has nearly three orders magnitude lower leakage current density at -10 V than that of PZT/Pt. The compa-

Table I. Characteristics of MFM and MFS capacitors.

	ΔV_T (V) at ±10 V	ε of PZT	Grain size (nm) of PZT	RMS roughness (nm) of PZT	Leakage current density (A/cm^2) at −10 V
MFM	3.59	515	~100	4.48	1.0 ± 10^{-5}
MFS	3.60	121	~65	1.96	3.1 ± 10^{-8}

rable memory characteristics and the lower leakage current of PZT on Al_2O_3/Si are important for continuous scaling down of the ferroelectric memory.

Acknowledgments

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