Improved Low Temperature Characteristics of P-Channel MOSFETs with $Si_{1-x}Ge_x$ Raised Source and Drain

Hsiang-Jen Huang, *Member, IEEE*, Kun-Ming Chen, *Member, IEEE*, Tiao-Yuan Huang, *Fellow, IEEE*, Tien-Sheng Chao, *Member, IEEE*, Guo-Wei Huang, *Member, IEEE*, Chao-Hsin Chien, and Chun-Yen Chang, *Fellow, IEEE*

***Abstract*—P-channel metal–oxide–semiconductor field-effect transistors with $Si_{1-x}Ge_x$ raised source and drain (RSD) have been fabricated and further studied for low temperature applications. The $Si_{1-x}Ge_x$ RSD layer was selectively grown by ANELVA SRE-612 ultra-high vacuum chemical vapor deposition (UHVCVD) system. Compared to devices with conventional Si RSD, improved transconductance and specific contact resistance were obtained, and these improvements become even more dramatic with reducing channel length. Well-behaved short channel characteristics with reduced drain-induced barrier lowering (DIBL) and off-state leakage current are demonstrated on devices with 100 nm $Si_{1-x}Ge_x$ RSD, due to the resultant shallow junction and less implantation damage. Moreover, temperature measurements reveal that $Si_{1-x}Ge_x$ RSD devices show more dramatic improvement in device performance at low temperature (−50 °C) operation, which can be ascribed to the higher temperature sensitivity of the $Si_{1-x}Ge_x$ sheet resistance.**

***Index Terms*—Low temperature measurements, PMOSFET, selective epitaxial growth (SEG), short channel effect, strained-SiGe, ultra-high vacuum chemical vapor deposition.**

I. INTRODUCTION

TO MEET the stringent demand of sub-0.1 μm devices, shallow junctions fabricated by out-diffusion from an *in situ* doped or ion-implanted p^+/n^+ $Si_{1-x}Ge_x$ layer have been reported [1]–[4]. Previously, pure Si selective epitaxy has been proposed to fabricate elevated source/drain (also known as raised source/drain) metal oxide semiconductor field effect transistor (MOSFET) to simultaneously achieve shallow junction for better device operation, and a thick sacrificial layer for reliable silicided contact to the junction [5]–[9]. In these regards, $Si_{1-x}Ge_x$ is better suited than pure Si. $Si_{1-x}Ge_x$ can not only be selectively deposited onto the exposed source and drain (S/D) area, similar to pure Si, it also enjoys a lower deposition temperature, which is beneficial for device application. Besides, $Si_{1-x}Ge_x$ can be selectively etched with high selectivity to Si and SiO_2 [10]. More importantly, $Si_{1-x}Ge_x$ has a lower Schottky barrier height with respect to p^+ junction because of the reduced band gap, which results in a lower contact resistivity and higher current drive, when compared to pure Si [11]–[13]. Recently, we have successfully fabricated p-channel metal oxide semiconductor field effect transistor (PMOSFET) with $Si_{1-x}Ge_x$ as the raised S/D layer, and its impacts on contact resistance and device performance have been studied [13]. In particular, we showed that by employing $Si_{0.86}Ge_{0.14}$ RSD, a drive current (measured at $V_D = -2.5$ V and $V_G - V_T = -2.5$ V) of 246 μA/μm, which represents a 17% improvement, compared to the counterpart with pure Si RSD, is achieved for an effective channel length of 0.24 μm. Furthermore, the improvement is found to increase with reducing channel length. For example, the improvement is only 15% when $L_{\text{eff}} = 0.5$ μm. However, the improvement can reach 29% when L_{eff} is reduced to 0.16 μm. This demonstrates the importance of maintaining a low series resistance as device is scaled down, thus makes the device with $Si_{0.86}Ge_{0.14}$ RSD even more attractive for future sub-0.1 μm technologies.

In this work, we report, for the first time, the temperature dependence on the $Si_{1-x}Ge_x$ RSD device performance. Detailed electrical characteristics of PMOSFETs with and without various RSD structures were measured and compared at three different temperatures, i.e., room temperature, −50 °C, and 100 °C. In addition, the drain-induced barrier lowering (DIBL) characteristics of PMOSFETs with $Si_{1-x}Ge_x$ RSD and the specific contact resistivity and sheet resistance variation as a function of temperature were also studied in detail.

II. EXPERIMENTS

The fabrication of P-channel MOS transistors with various raised source/drain structures started with a standard baseline process [13]. Briefly, following a 4 nm gate oxide growth and polysilicon gate formation, source/drain extension implant (1×10^{15} cm^{-2}, 10 KeV) was performed. Then, a 800 °C, 20 min furnace anneal and a 1050 °C, 10 s rapid thermal anneal

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H.-J. Huang was with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. She is now with IBM Semiconductor Research and Development Center, Hopewell Junction, NY 12533 USA.

K.-M. Chen was with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University. He is now with the National Nano Device Laboratories, Hsinchu, Taiwan, R.O.C.

T.-Y. Huang and C.-Y. Chang are with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. (e-mail: cyc@cc.nctu.edu.tw).

T.-S. Chao is with the National Nano Device Laboratories and also with the Department of Engineering and System Science, National Tsing Hua University, Hsinchu, Taiwan, R.O.C.

G.-W. Huang and C.-H. Chien are with the National Nano Device Laboratories, Hsinchu, Taiwan, R.O.C.

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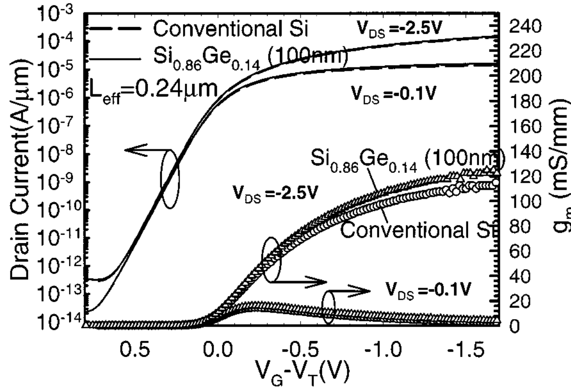

Fig. 1. $I_D - V_G$ and transconductance characteristics of a conventional Si RSD and a $Si_{0.86}Ge_{0.14}$ RSD devices, both with gate oxide thickness of 4 nm.

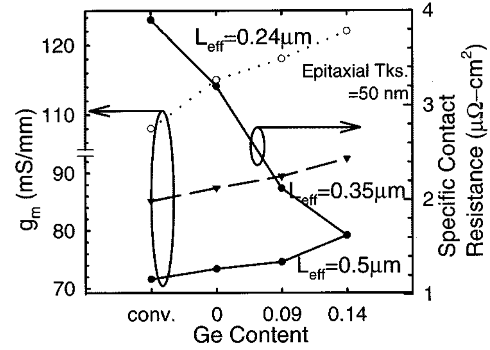

Fig. 2. Transconductance as a function of Ge mole fraction for various device channel length. The specific contact resistivity as a function of Ge mole fraction is also plotted in this figure.

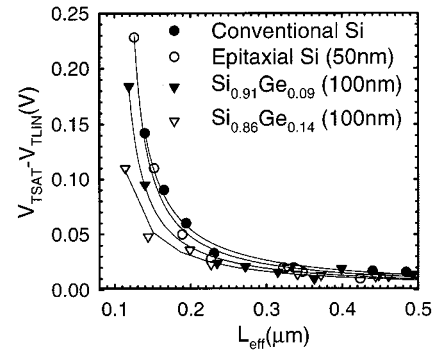

Fig. 3. Drain-induced barrier lowering DIBL ($V_{TSAT} - V_{TLIN}$) for PMOS transistors with various RSD structures.

(RTA) were performed for dopant activation. Afterwards, a 150 nm sidewall spacer was formed. Next, wafers were split to receive either SiGe or Si selective epitaxial growth (SEG) on the exposed S/D regions by an ANELVA SRE-612 cold-wall ultra-high vacuum chemical vapor deposition (UHVCVD) system [14]. The standby base pressure was kept at 2×10^{-10} torr. For growing B-doped strained $Si_{1-x}Ge_x$ layers, Si_2H_6, GeH_4, and 1% B_2H_6 diluted in H_2 were introduced to achieve a growth rate of 41 Å/min for $Si_{0.91}Ge_{0.09}$ and 43 Å/min for $Si_{0.86}Ge_{0.14}$ at 550 °C, respectively. The maximum operation time for maintaining selective epitaxial growth of $Si_{0.91}Ge_{0.09}$ or $Si_{0.86}Ge_{0.14}$ layer (i.e., epitaxy on Si region only, but not on field oxide region) at 550 °C is above 90 min. Samples with epitaxial thickness of 50 nm and 100 nm were processed in order to study the effects of the epitaxial layer thickness on the device performance. For comparison, conventional Si MOS transistors (i.e., without any raised S/D layer) were also fabricated in the same run. To obtain higher degree of boron concentration in S/D region, a 5×10^{15} cm^{-2}, 20 KeV BF_2 implant was adopted, which is followed by a 900 °C, 30 s RTA for activation. Afterwards, a 500 nm TEOS was deposited, and a Ti/TiN/Al–Si–Cu/TiN 4-layer metal was deposited and patterned to complete contact metallization. Electrical characterizations at various temperatures ranging from −50 °C to 100 °C were performed with a HP4156 system, which was equipped with a thermal controller connected to the Cascade semi-auto probe station. Sheet resistance was extracted using bridge resistor test structures, while the contact resistance was measured by Kelvin cross-bridge structures.

III. Results and Discussions

Fig. 1 compares the $I_D - V_G$ and transconductance (g_m) characteristics of MOS transistors with $Si_{0.86}Ge_{0.14}$ and Si RSD samples. Both devices have the same epitaxial RSD thickness of 100 nm and the same effective channel length of 0.24 μm. By using $Si_{0.86}Ge_{0.14}$ RSD, g_m and I_D values (measured at $V_{DS} = -2.5$ V and $V_G - V_T = -1.8$ V) of 127 mS/mm and 158.6 μA/μm, which are 19.02% and 16.11% higher than those of the counterpart device with Si RSD device, are obtained. These improvements are believed to be due to the lowering of the Schottky barrier height (SBH) in metal/$p^+Si_{1-x}Ge_x$ junction, which leads to the reduction of sheet resistance and specific contact resistivity [6]. The energy band gap (Eg) of $Si_{1-x}Ge_x$ is known to change from 1.12 to 0.66 eV with increasing Ge mole fraction [15]. For pseudomorphic p-$Si_{0.86}Ge_{0.14}$ layer, the SBH is expected to be lower than that of metal/p^+Si by 0.07 eV [16], thus effectively reduces the specific contact resistivity (ρ_C).

As shown in Fig. 2, the transconductance and relative contact resistivity measured by transmission line method (TLM) are plotted as a function of Ge mole fraction for devices with various channel lengths. The thickness of the epitaxial RSD layer is 50 nm. It can be seen that the effects of ρ_C on device performance become more dramatic when the devices are scaled down. For $L_{\rm eff} = 0.24$ μm, a 13% improvement in g_m value could be obtained for PMOSFET with 50 nm $Si_{0.86}Ge_{0.14}$ RSD, compared to the device with Si RSD.

With a thicker epitaxial RSD layer (e.g., 100 nm), shallower p^+ S/D junction could be obtained, especially for $Si_{1-x}Ge_x$ layer with higher Ge mole fraction [2], [17], [18]. Thus the susceptibility to punch-through and short channel effect could be alleviated, which is advantageous especially for sub-0.1 μm devices. Fig. 3 shows the drain-induced barrier lowering (DIBL) effects for PMOSFETs with various structures. V_{TLIN} is defined as the threshold voltage extracted at maximum transconductance at the drain voltage of 0.1 V, while V_{TSAT} is the saturation threshold voltage extracted at drain voltage of 2.5 V. While the device with a thin 50 nm Si RSD displays essentially the same DIBL characteristics as the conventional Si PMOSFET

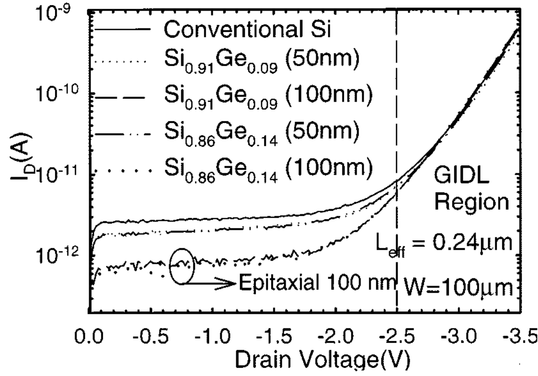

Fig. 4. Drain leakage current I_D as a function of drain bias V_{DS} in off-state ($V_G = 0$ V) for conventional Si RSD and SiGe RSD devices.

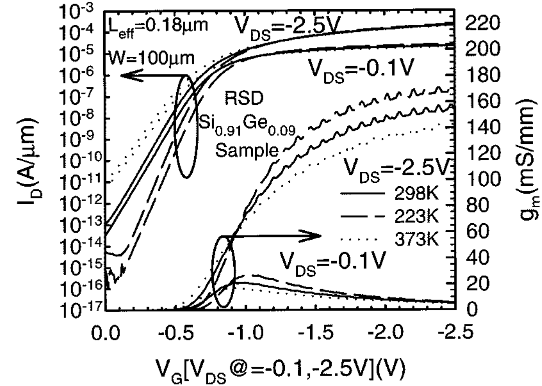

Fig. 6. Subthreshold characteristics and transconductance of $Si_{0.91}Ge_{0.09}$ RSD PMOS transistor measured at various temperatures.

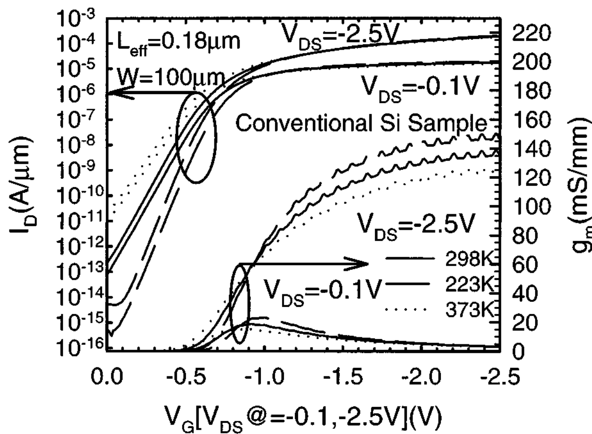

Fig. 5. Subthreshold characteristics and transconductance of conventional Si PMOS transistor measured at various temperatures.

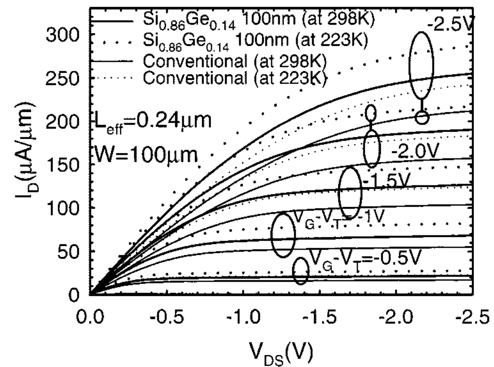

Fig. 7. Drain current versus drain voltage for conventional and $Si_{0.86}Ge_{0.14}$ RSD PMOS transistors.

without any RSD, improvement in DIBL is observed for the device with 100 nm $Si_{1-x}Ge_x$ RSD because the junction depth of the 100 nm $Si_{1-X}Ge_X$ RSD in the source and drain region would be as shallow as the depth of the extension region (<800 Å). In addition, the improvement in DIBL indeed increases with increasing Ge mole fraction. It is worthy to note that for device with a thick 100 nm $Si_{1-x}Ge_x$ RSD, the implant damage could be alleviated, because the damage region is located away from the p^+–n S/D junction. Thus no high temperature anneal (>900 °C) is necessary to anneal out defects caused by the implant damage, as is required in conventional Si PMOSFETs. The remarkable leakage current reduction at low V_{DS} level is indeed confirmed in Fig. 4 for devices with $Si_{1-x}Ge_x$ RSD, all devices with an effective channel length of 0.24 μm. On the other hand, there is essentially no difference in the gate induced drain leakage current (GIDL) that is measured at high V_{DS} bias. This is because the interface quality between gate and drain region for all samples remains essentially the same.

The effects of $Si_{1-x}Ge_x$ RSD on the low temperature operation of the transistors were also studied. Figs. 5 and 6 showed the subthreshold and transconductance characteristics measured at three different temperatures (i.e., 223, 298, and 373 K) for a conventional p-channel device (i.e., without any RSD) and the device with 100 nm $Si_{0.91}Ge_{0.09}$ RSD, respectively. Both the transconductance and the drain current increase with reducing temperature due to increased carrier mobility. At -50 °C, the transconductance value is 145 mS/mm and 169 mS/mm (measured at $V_{DS} = -2.5$ V) for the conventional device and the device with $Si_{0.86}Ge_{0.14}$ RSD, respectively. Leakage current also achieves its lowest value at the lowest measurement temperature (i.e., -50 °C), because of reduced scattering rate and increased carrier mean free path. Generally, all aspects of I–V characteristics approach their optimum conditions with reducing temperature. Threshold voltage V_T decreases while temperature increases due to increased number of intrinsic carriers. Finally, the thermal behavior of the parasitic components in a transistor could also affect the output characteristics of the transistors. Standard I_D versus V_{DS} characteristics for the conventional non-RSD device and the device with 100 nm $Si_{1-x}Ge_x$ RSD are shown in Fig. 7 for two operation temperatures, i.e., 223 K (-50 °C) and 298 K (25 °C). The channel width of the transistors is 100 μm. In the figure, solid and dotted lines denote the conventional device and the device with $Si_{0.86}Ge_{0.14}$ RSD operating at -50 °C (coarse lines) and 25 °C (thin lines), respectively. The improvements with reduced temperature are more dramatic for the device with $Si_{0.86}Ge_{0.14}$ RSD, as compared with the conventional device. The drain current (measured at $V_{DS} = -2.5$ V, $V_G - V_T = -2.5$ V) are 286.5 μA/μm and 254.8 μA/μm for RSD $Si_{0.86}Ge_{0.14}$ and the conventional device at -50 °C. In order to confirm this phenomenon further, the saturation transconductance g_m versus effective channel length L_{eff} is plotted in Fig. 8. It reveals the superior room tempera-

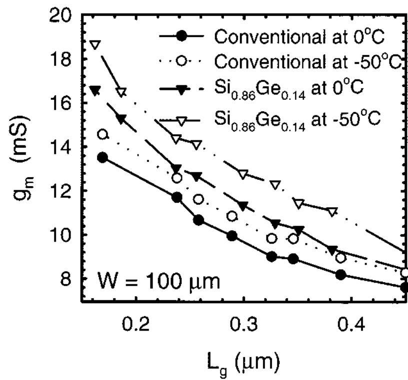

Fig. 8. Saturated transconductance g_m versus effective gate length measured at various temperatures for conventional and $Si_{0.86}Ge_{0.14}$ RSD devices.

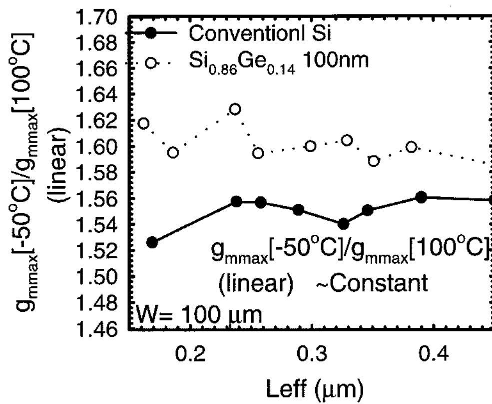

Fig. 9. Normalized $g_{m\ \max}[-50\ °C]/g_{m\ \max}[100\ °C]$ versus effective channel length for conventional and $Si_{0.86}Ge_{0.14}$ RSD devices.

ture and low-temperature performance in g_m value for the device with $Si_{0.86}Ge_{0.14}$ RSD. For an effective channel length of 0.17 μm, the transconductance increases from 166 to 187 mS/mm as temperature changes from 25 °C to −50 °C for the device with $Si_{0.86}Ge_{0.14}$ RSD, which represents a 12.5% improvement in g_m. In contrast, the g_m value changes from 135 to 146 under the same condition for the conventional device, which represents only 7.8% improvement for low-temperature operation.

To calculate the degree of improvements in transconductance, the normalized maximum linear g_m value measured at −50 °C with respect to the same parameter measured at 100 °C is plotted as a function of the effective channel length in Fig. 9. The average ratio of enhancement is roughly 1.6 and 1.54 for the $Si_{0.86}Ge_{0.14}$ RSD device and the conventional device, respectively. For device operation in saturation mode, normalized drive current $I_{\rm on}[-50\ °C]/I_{\rm on}[100\ °C]$ (measured at $V_{DS} = -2.5$ V and $V_G = -2.5$ V) as a function of the effective channel length $L_{\rm eff}$ is shown in Fig. 10. A remarkable improvement in the normalized drive current as temperature varied from 100 °C to −50 °C is again observed for devices with $Si_{1-x}Ge_x$ RSD, as compared with the conventional devices. It is worthy to note here that the normalized drive current $I_{\rm on}[-50\ °C]/I_{\rm on}[100\ °C]$ reduces with decreasing $L_{\rm eff}$ for all devices. This trend is different from that of the normalized maximum linear g_m which remains essentially constant with

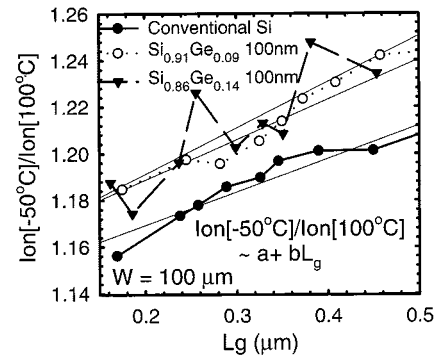

Fig. 10. Normalized $I_{\rm ON}[-50\ °C]/I_{\rm ON}[100\ °C]$ versus effective channel length for conventional and $Si_{0.91}Ge_{0.09}$ RSD, and $Si_{0.86}Ge_{0.14}$ RSD devices.

reducing $L_{\rm eff}$. This is because when the device is operating in linear region (e.g., $V_{DS} = -0.1$ V), carrier velocity is under low electric field condition, mobility μ_P which is independent of channel length plays an important role in maximum linear g_m. As a result, a constant value in maximum linear g_m versus $L_{\rm eff}$ that is dependent only on temperature is observed for all devices. However, when the device is operating in saturation mode (e.g., $V_G = -2.5$ V, and $V_{DS} = -2.5$ V), a high electric field is generated along the channel and would become even higher as $L_{\rm eff}$ decreases. Several factors, including velocity saturation, reduced carrier mobility caused by carrier scattering, and extrinsic component at high current drive would dominate and determine the $I_{\rm on}[-50\ °C]/I_{\rm on}[100\ °C]$ behavior, thus reduces the enhancement ratio as devices are scaled down.

In order to study further the temperature variations in intrinsic and extrinsic components of the transistors, sheet resistance ρ_S and contact resistivity ρ_C as a function of temperature were measured, and the results are shown in Figs. 11 and 12, respectively. Generally, sheet resistance in source and drain region, extension layer, and channel resistance decreases with reducing temperature due to enhanced mobility. On the contrary, specific contact resistivity increases with reducing temperature because less number of carriers would be able to overcome the metal/semiconductor energy barrier (SBH) by thermionic emission. This is especially true for the conventional device with higher energy barrier. The superior low-temperature behavior of the $Si_{1-x}Ge_x$ RSD device can be elucidated by the basic MOSFET model [19]. A MOSFET can always be broken down into an intrinsic MOS device and extrinsic source and drain resistive components. The entire extrinsic transconductance is

$$g_m = \frac{1}{\dfrac{1}{g_{mo}} + R_{Source}} \tag{1}$$

where g_{mo} is the transconductance of the intrinsic device, R_{Source} denotes the parasitic resistance including sheet resistance, contact resistance, and extension resistanc, etc. The measured contact resistance values for a 2 × 2 μm contact are 45.82, 3.17, and 1.94 Ω, while the sheet resistance values at 298 K are 132.5, 84.6, and 96.48 Ω/□ for conventional, $Si_{0.91}Ge_{0.09}$ RSD, $Si_{0.86}Ge_{0.14}$ RSD, respectively. Since the contact resistance is relatively small, the entire R_{Source} is

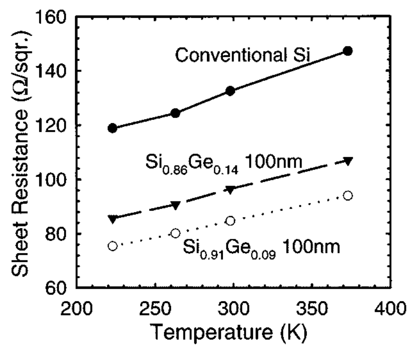

Fig. 11. Sheet resistance as a function of temperature for various structures.

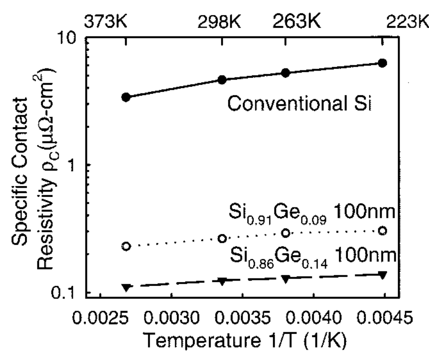

Fig. 12. Specific contact resistivity as a function of reciprocal temperature $(1/T)$ for metal with different contact layer structures.

mainly determined by the sheet resistance (ρ_S) and extension resistance. So the temperature dependence of the device's electrical performance would basically follow the temperature behavior of the sheet resistance. However, the temperature dependence of the sheet resistance is more sensitive for $Si_{1-x}Ge_x$ RSD device than that of the conventional device. For example, ρ_S changes from 132.47 to 118.86 as temperature changes from 298 K to 223 K, which represents a 10.27% reduction, for the conventional device. In comparison, a 10.98% and 11.21% reduction ratio could be obtained for devices with $Si_{0.09}Ge_{0.91}$ RSD and $Si_{0.86}Ge_{0.14}$ RSD, respectively. The more sensitive temperature behavior of $Si_{1-x}Ge_x$ RSD devices can thus explain their dramatic improvement in device performance at low temperature.

IV. Conclusion

In this paper, the drain-induced barrier lowering effects and low-temperature characteristics of p-channel transistors with $Si_{1-x}Ge_x$ raised source and drain (RSD) were studied. We found that $Si_{1-x}Ge_x$ RSD devices show better device performance including better drive current, transconductance, and reduced short-channel effects, compared to pure Si RSD devices. The improvements, which become more dramatic with reducing channel length, are believed to be mainly due to the lowering of the Schottky barrier height in metal/$p^+Si_{1-x}Ge_x$ junction, which leads to the reduction of sheet resistance and specific contact resistivity. Moreover, $Si_{1-x}Ge_x$ RSD devices are also found to depict a larger improvement rate under low temperature operation, which can be explained by the higher temperature sensitivity of the resistance of $Si_{1-x}Ge_x$ RSD. These performance improvements thus make $Si_{1-x}Ge_x$ RSD structure very attractive for future sub-0.1 μm p-channel MOS transistors.

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Hsiang-Jen Huang (M'00) was born in Kaohsiung, Taiwan, R.O.C., in 1974. She received the B.S. degree and the Ph.D. degree in electrical engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1996 and 2000, respectively.

In 1996, she was with the RF Group, National Nano Device Laboratories working on RF CMOS processing and device analyses. She changed her subject into SiGe PMOSFETs and related material analyses in 1997. Her research interests are in the general area of high-speed and low-power integration technologies. She is now working at IBM Semiconductor Research and Development Center, Hopewell Junction, NY.

Kun-Ming Chen (M'00) was born in Miaoli, Taiwan, R.O.C., in 1971. He received the M.S. degree and the Ph.D. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1996 and 2000, respectively.

He joined the National Nano Device Laboratories, Hsinchu, Taiwan, in 2000, as an Associate Researcher. He was engaged in research on the SiGe and microwave device process and characterization.

Tiao-Yuan Huang (F'95) was born in Kaohsiung, Taiwan, R.O.C., on May 5, 1949. He received the B.S.E.E. and M.S.E.E. degrees from National Cheng Kung University, Taiwan, in 1971 and 1973, respectively, and the Ph.D. degree in electrical engineering from the University of New Mexico, Albuquerque, in 1981.

After serving two years in the Taiwanese Navy, he joined the Chung Shan Institute of Science and Technology, Lungtan, working on missile development. He left for the U.S. in 1977. After a two-year stint with Semiconductor Process and Design Center, Texas Instruments, he moved on to Silicon Valley and had since worked with several companies, including Xerox Palo Alto Research Center, Integrated Device Technology, Inc., and VLSI Technology, Inc. He had worked in various VLSI areas including memories (DRAM, SRAM, and nonvolatile memories), CMOS process/device technologies and device modeling/simulation, ASIC technologies, and thin film transistors for LCD display. In 1995, he returned to Taiwan to become an Outstanding Scholar Chair Professor with National Chiao-Tung University and Vice President with National Nano Device Laboratories, National Science Council, Taiwan. He has published over 150 technical papers in international journals and conferences, and holds over 40 patents.

Dr. Huang received the 1988 Semiconductor International R&D Technology Achievement Award for his invention of the fully overlapped LDD transistors. He served on the technical committee of the IEEE International Electron Devices Meeting (IEDM) in 1991 and 1992. He also served on the program committee of the International Conference on Solid States Devices and Materials (SSDM) from 1996 to 1998.

Tien-Sheng Chao (M'96) was born in Penghu, Taiwan, R.O.C., in 1963. He received the Ph.D. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1992.

He joined the National Nano Device Laboratories (NDL) as an Associate Researcher in July 1992, and became a Researcher in 1996. He was engaged in developing the thin dielectrics preparations, cleaning processes, and CMOS devices fabrication.

Guo-Wei Huang (M'97) was born in Taipei, Taiwan, R.O.C., in 1969. He received the B.S. degree in electronics engineering and the Ph.D. degree from National Chiao-Tung University, Hsinchu, Taiwan, in 1991 and 1997, respectively.

He joined National Nano Device Laboratories, Hsinchu, in 1997, as an Associate Researcher. His current research interests focus on the design, characterization, and modeling of SiGe and microwave devices.

Chao-Hsin Chien is with the National Nano Device Laboratories, Hsinchu, Taiwan, R.O.C.

Chun-Yen Chang (F'88) was born in Feng-Shan, Taiwan, R.O.C. He received the B.S. degree in electrical engineering from Cheng Kung University, Taiwan, in 1960, and the M.S. degree in tunneling in semiconductor–superconductor junctions and the Ph.D. degree in carrier transport across metal-semiconductor barrier, both from National Chiao-Tung University (NCTU) Hsinchu, Taiwan, in 1969.

He has devoted himself to education and academic research for more than 40 years. He has contributed profoundly to the areas of microelectronics and optoelectronics, including the invention of the method of low-pressure-MOCVD-using tri-ethyl–gallium to fabricate LED, laser, and microwave transistors, Zn-incorporation of SiO_2 for stabilization of power devices, and nitridation of SiO_2 for ULSIs, etc. From 1962 to 1963, he fulfilled his military service by establishing at NCTU Taiwan's first experiment TV transmitter that formed the founding structure of today's CTS. In 1963, he joined NCTU to serve as an instructor establishing a high vacuum laboratory. In 1964, he and his colleague established the semiconductor research center (SRC) at NCTU with a very up-to-date, albeit homemade, facility for silicon device processing, where they made the nation's first Si Planar transistor in April 1965, and subsequently the first IC in August 1966. In 1968, he published Taiwan's first-ever semiconductor paper in the international journal *Solid State Electronics*. In 1969, he became a Full Professor, teaching solid state physics, quantum mechanics, semiconductor devices and technologies. From 1977 through 1987, he single-handedly established a strong electrical engineering and computer science program at NCKU where GaAs, α-Si, poly-Si researches were established in Taiwan for the first time. Since 1987 he served consecutively as Dean of Research (1987–1990), Dean of Engineering (1990–1994), and Dean of Electrical Engineering and Computer Science (1994–1995). Simultaneously he was serving as the founding president of National Nano Device Laboratories (NDL) from 1990 through 1997. In 1997, he became Director of the Microelectronics and Information System Research Center (MIRC), NCTU (1997–1998). Many of his former students have since become founders of the most influential Hi-Tech enterprises in Taiwan, namely UMC, TSMC, Winbond, MOSEL, Acer, Leo, etc. In August 1, 1998, he was appointed as the President of NCTU. As the National-Chair-Professor and President of NCTU, his vision is to lead the university for excellence in engineering, humanity, art, science, management and bio-technology. To strive forward to world class multidisciplinary university is the main goal to which he and his colleagues have committed.

Dr. Chang received the IEEE third millennium medal in 2000. He is a member of Academia Sinica and a Foreign Associate of the National Academy of Engineering.