Stack Gate PZT/Al_2O_3 One Transistor Ferroelectric Memory

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***Abstract*—We have developed single transistor ferroelectric memory using stack gate PZT/Al_2O_3 structure. For the same $\sim$40 Å dielectric thickness, the PZT/Al_2O_3/Si gate dielectric has much better C–V characteristics and larger threshold voltage shift than those of PZT/SiO_2/Si. Besides, the ferroelectric MOSFET also shows a large output current difference between programmed on state and erased off state. The $<$100 ns erase time is much faster than that of Flash memory where the switching time is limited by erase time.**

***Index Terms*—Al_2O_3, ferroelectric, memory, PZT.**

I. Introduction

FERROELECTRIC material devices have been discovered for over three decades to be good candidates for memory [1], and currently 4 MB one-transistor and one-capacitor (1T1C) structure has been developed [2]. In comparison with Flash memory or DRAM, the 1T1C ferroelectric RAM has much faster access time than Flash memory and much longer retention time than DRAM [2]. However, it is desirable to further develop 1T ferroelectric MOSFET (FeMOSFET) structure for memory application because the 1T structure has simpler process steps and smaller size than 1T1C cell. Unfortunately, achieving good interface between ferroelectric dielectric and Si is difficult because most ferroelectric films will easily react with Si to form a nonferroelectric interfacial layer even at temperatures as low as 500 °C [3], [4]. Furthermore, the diffusion of Pb from ferroelectric Pb(Zr,Ti)O_3 (PZT) or Li from $LiNbO_3$ into Si may also be expected to degrade the device integrity and cause process integration problem, because metal ion contamination is an important concern in VLSI [5]. In this letter, we have developed 1T FeMOSFET memory using Al_2O_3 gate dielectric [6], [7] as a buffer layer between PZT and Si. In comparison with other buffer layers used for 1T ferroelectric memory [8]–[10], high k Al_2O_3 has not only good gate dielectric integrity but also excellent diffusion barrier property. The stack gate PZT/Al_2O_3 FeMOSFET memory also has the advantage of structure compatible with high k Al_2O_3 MOSFET logic used for sub-100 nm VLSI generation [11].

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II. Experimental

P-type 4-in (100) Si wafers were used in this study. After device isolation and source/drain definition, the 22 Å Al layer is deposited by evaporation where HF-vapor passivation and *in-situ* desorption [6], [7], [12] are used to suppress the native oxide formation before Al deposition. The deposited Al is first oxidized at a temperature of 400 °C for 1 h by oxygen to a thickness of 38 Å followed by an 800 °C annealing for 30 min in nitrogen ambient. Then the 2500 Å PZT layer was spin-coated on Al_2O_3 gate dielectric by the sol-gel method [13], dried at 90 °C for 30 sec, and finally annealed at 700 °C. Al electrodes were formed by thermal evaporation for source, drain and gate, and the channel length and width were 4 μm and 100 μm, respectively. The reason why using Al metal gate on PZT is because Al is widely used for VLSI process, even though Pt, Ir, and their oxide compounds have higher work-function and probably lower leakage current than Al. For comparison, FeMOS capacitor using 40 Å thermal SiO_2 as buffer layer was also fabricated. The device performance was characterized by C–V and I–V measurements.

III. Results and Discussion

Fig. 1(a) and (b) show the 1 MHz C–V characteristics of FeMOS capacitor with stack gate PZT/SiO_2/Si and PZT/Al_2O_3/Si structures, respectively. As shown in Fig. 1(a), the PZT/SiO_2 gate dielectric has only a small threshold voltage shift of 1.3 V, and the distorted C–V curves without proper depletion suggest strong interdiffusion or interface reaction between PZT and Si. In sharp contrast, PZT/Al_2O_3 gate dielectric shown in Fig. 1(b) has well-behaved C–V characteristics from inversion to depletion regions, which suggests the good barrier property of Al_2O_3 gate dielectric. Furthermore, larger threshold voltage shift and higher capacitance than those of PZT/SiO_2 are observed that are important for memory application. The threshold voltage change increases from 0.5 to 5 V for applied gate voltage increasing from $\pm$5 to $\pm$15 V difference, which can be used for multilevel memory. The threshold voltage difference is due to polarization reversal in ferroelectric PZT film after applying different polarity of gate voltage.

Fig. 2(a) and (b) show the I_D–V_D characteristics of the 4 μm PZT/Al_2O_3/Si FeMOSFET after writing on ($+$10 V) and off ($-$10 V) gate voltage for 1 s, respectively. Then small gate voltages from $-$1 to 3 V are applied for the I_D measurements, and good transistor I_D–V_D characteristics are obtained in both cases. The large I_D difference after writing $+$10 V and $-$10 V

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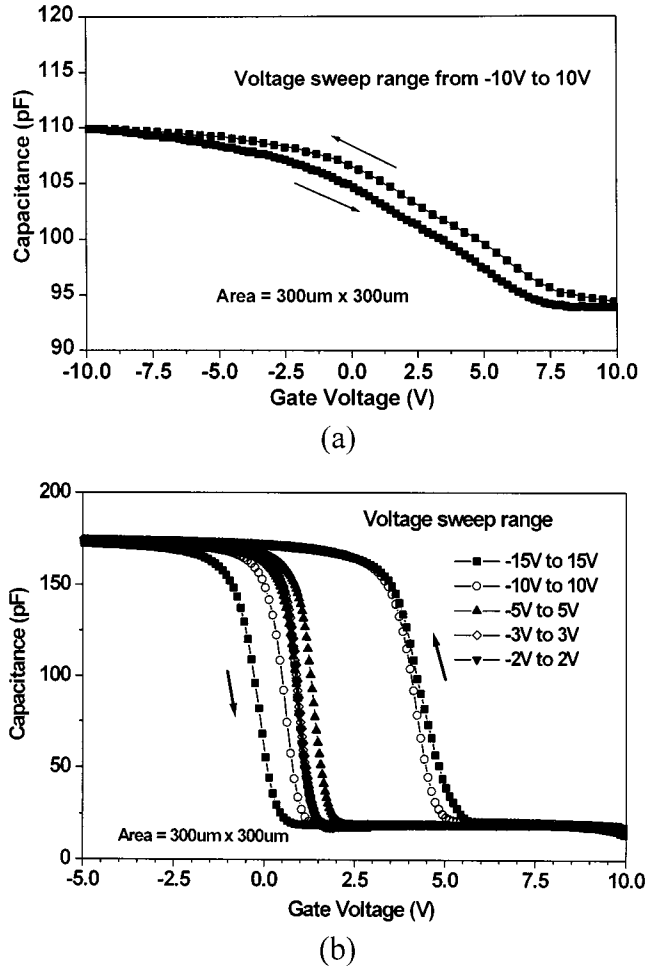

Fig. 1. C–V characteristics of (a) PZT/SiO_2/Si and (b) PZT/Al_2O_3/Si capacitors. The capacitor size is 9×10^{-4} cm^2.

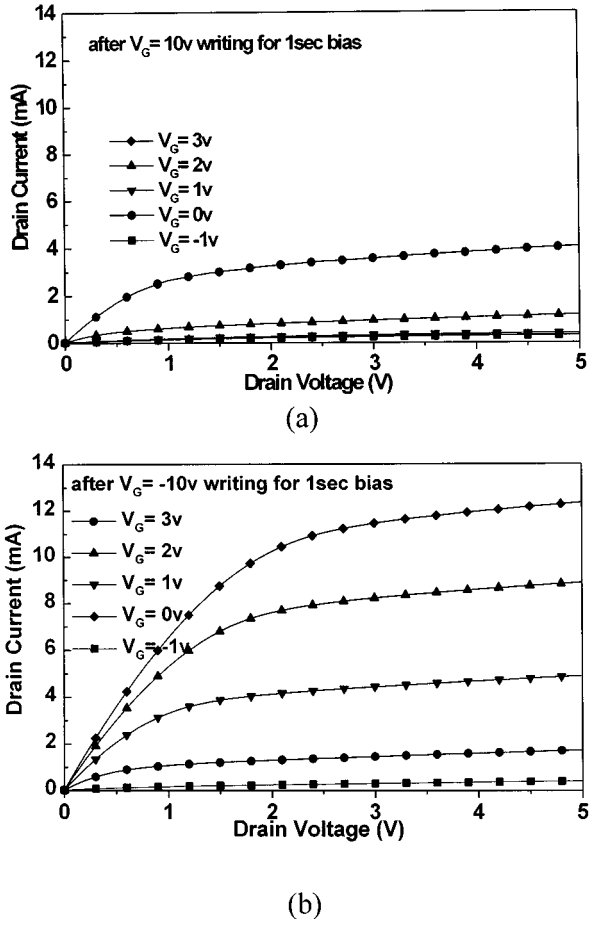

Fig. 2. I_d–V_d characteristics of PZT/Al_2O_3 FeMOSFET after applying (a) 10 V and (b) -10 V for 1 s, respectively. The gate length of the FeMOSFET is 4 μm.

gate voltage is due to the threshold voltage shift that is consistent with C–V results in Fig. 1(b). This result clearly demonstrates the memory operation of the stack gate PZT/Al_2O_3/Si FeMOSFET. The high drive current of 125 μA/μm at 4 μm gate length is desirable for high speed memory circuit, which is due to the small thickness of Al_2O_3 and high k property of PZT.

Gate dielectric property is another important factor for practical VLSI application. Fig. 3 shows the gate leakage current density of the PZT/Al_2O_3/Si FeMOS. A high breakdown voltage of 30 V is measured that gives a breakdown electric field of 1.2 MV/cm for a 2500 Å dielectric thickness. This large breakdown voltage ensures possible multiple-level memory application shown in Fig. 1(b). Low leakage current densities of 1×10^{-6} and 3×10^{-5} A/cm^2 are measured at applied gate voltage of 10 and 15 V respectively, which allows parallel program/erase like Flash memory to further increase the write speed.

We have further characterized the erase speed of this 1T memory. Fig. 4(a) shows the erase pulse (write 0) width dependent I_d–V_d characteristics from 10 ns to 100 ms and Fig. 4(b) is the time-dependent drain current evolution. Only less than 100 ns at 8 V is needed to switch from on state to off state,

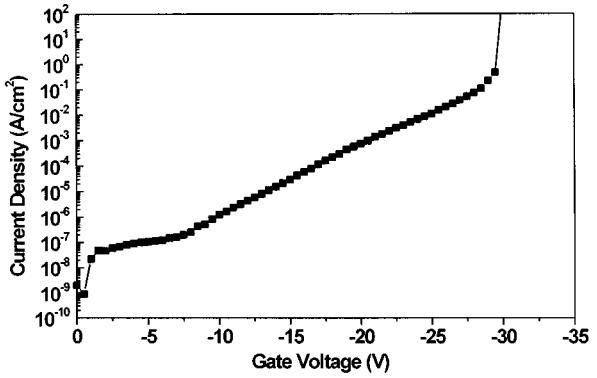

Fig. 3. Gate leakage current of PZT/Al_2O_3/Si capacitor with size of 50 μm $\times$ 50 μm.

which is due to the rapid polarization reversal of ferroelectric PZT film. Furthermore, the obtained one order magnitude of I_D difference between on and off states can be distinguished by the sense amplifier in a memory circuit. Because the access time of Flash memory is limited by the slow erase time, the much faster erase time of this new device is important for nonvolatile memory application. The other important memory characteristics of fatigue and retention of this 1T memory will be discussed in our future research.

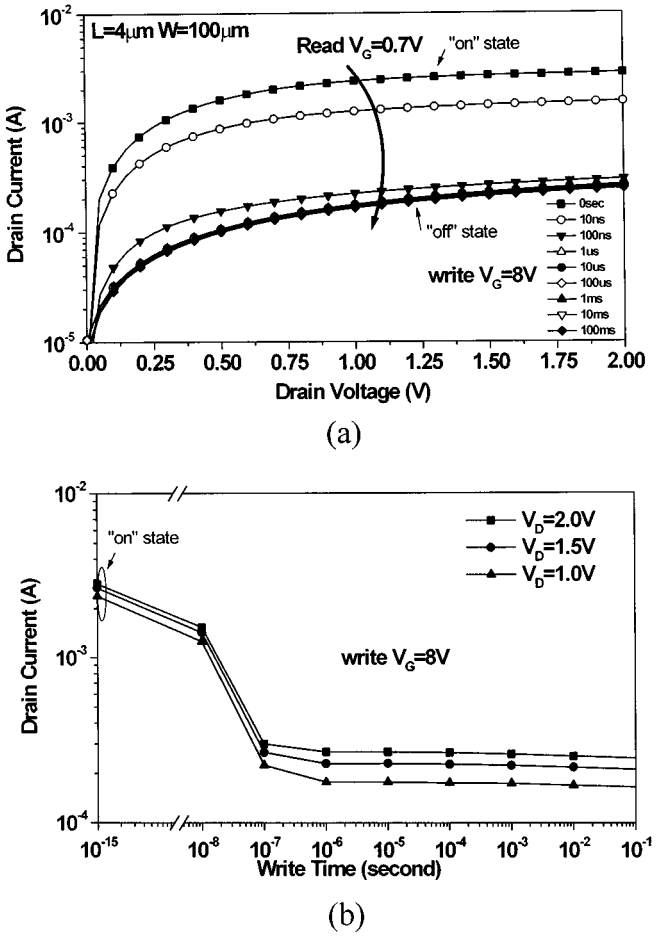

Fig. 4. (a) I_d–V_d characteristics of FeMOSFET after 8 V voltage applied to gate with different erase pulse width, and (b) time-dependent drain current evolution from (a).

IV. Conclusion

Ferroelectric 1T memory with low gate leakage current density and high erase speed has been successfully demonstrated using PZT/Al_2O_3/Si structure. The use of high k Al_2O_3 in the stack gate 1T memory makes this device compatible with advanced VSLI process.

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