# Characterization of Ultrathin Oxynitride (18–21 Å) Gate Dielectrics by $NH_3$ Nitridation and $N_2O$ RTA Treatment

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***Abstract*—In this paper, we developed a new method to grow robust ultrathin oxynitride ($E_{OT} = 18$ Å) film with effective dielectric constant of 7.15. By $NH_3$-nitridation of Si substrate, grown ultrathin $Si_3N_4$ with $N_2O$ annealing shows excellent electrical properties in terms of significant lower leakage current, very low bulk trap density and trap generation rate, and high endurance in stressing. In addition, this oxynitride film exhibits relatively weak temperature dependence due to a Fowler–Nordheim (FN) tunneling mechanism. This dielectric film appears to be promising for future ultralarge scale integrated (ULSI) devices.**

***Index Terms*—$N_2O$, $NH_3$, nitridation, oxynitride, rapid thermal annealing (RTA), $Si_3N_4$.**

## I. Introduction

THE MOSFET scaling trend sustains to outlive its usefulness in the foreseeable future as the device dimensions, including the gate oxide thickness, continue to shrink in each successive generation of new integrating circuit technology. Continuous scaling of thermal $SiO_2$ as the gate dielectric has run into difficulties due to excess leakage current when oxide thickness is less than 25 Å [1]. Moreover, it has been reported that the temperature acceleration effect and the stress induced leakage current (SILC) reliability were severe enough to raise concern over the further scaling down of thermal oxide [2]. However, the scaling of MOSFET is essential to increase the drive current of devices, which is proportional to the gate capacitance. In the course of searching for such an alternative gate dielectric, ultrathin silicon nitride films have been studied as the promising replacement for thermal oxide gate dielectric as gate dielectrics to meet the need for increased capacitance while maintaining a low gate leakage in future ultralarge scale integrated (ULSI) devices.

In addition, in EEPROM and Flash memory devices, the thickness of the tunnel oxide is limited by the SILC after many write/erase (WE) cycles. This oxide leakage current at low electric fields is increased by high-field stress, which is considered as one of the main causes for read disturb (soft write) [3]. This SILC phenomenon may be due to enhanced FN tunneling by buildup of the generated holes similarly to the intrinsic breakdown [4]. As the dielectric film is thinner, it has been a serious problem with regard to not only retention characteristic but also read disturb for Flash memories [5]. Ultrathin nitride or oxynitride films [6]–[8] have been reported with good performance in SILC. Hence, it becomes the most promising candidate to replace thermal $SiO_2$ film as the tunneling dielectric to improve WE endurance. However, the $Si_3N_4$/Si interface is not yet as good as the $SiO_2$/Si interface and the density of interface defects is also relatively high. One possible solution is to form a nitride/oxide (N/O) stack dielectric, which maintains the advantage of silicon nitride and still preserves the excellent $SiO_2$/Si interface [7]. Recently, the ultrathin silicon nitride by adding $N_2O$ treatment can reduce this interface state and bulk trap densities [9], [10]. It should be mentioned that conventional CVD O/N or O/N/O stack structures have been widely used as a DRAM storage dielectric. However, this stack dielectric is not adequate to meet the much more stringent requirements of the gate dielectric. For example, it is well known that the conventional CVD silicon nitride usually contains a large number of bulk traps and interface states, which give rise to severe reliability problems [11]–[13]. In this paper, we report a novel method to enhance nitrogen incorporation with $N$ located away from $SiO_2$/Si interface. An ultrathin oxynitride is grown by nitridizing the silicon substrate in $NH_3$ and with an additional $N_2O$ treatment is proposed. This oxynitride film not only increases dielectric constant of the resulting film to achieve thinner equivalent oxide thickness ($E_{OT}$) without degrading $SiO_2$/Si interface properties, but also has excellent electrical and reliability characteristics.

## II. Experimental

Samples were fabricated on 4-in p-type (100)-oriented silicon wafers with resistivity of 14–21 Ω-cm. After all wafers were cleaned by standard RCA clean method, a $Si_3N_4$ film of 15 Å was first grown by $NH_3$ (with flow rate of 105 sccm, pressure 500 mTorr) nitridation of the Si substrate in LPCVD system at 850 °C for 1 h. Samples were then immediately annealed at

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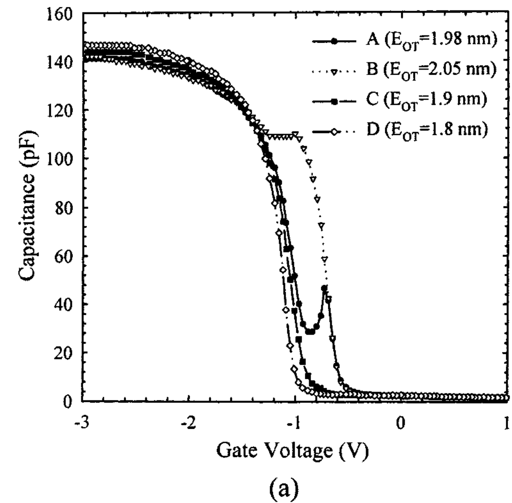
TABLE I
ANNEALING VARIOUS CONDITIONS FOR ULTRATHIN SILICON NITRIDE FILMS AND $k$-VALUE

| Condition | Annealing at 800℃ in different gas and time by RTP | k-value |
|---|---|---|
| A | Annealing in diluted $N_2O/N_2$=1/1 gas for 20 sec | 6.5 |
| B | Annealing in diluted $N_2O/N_2$=2/1 gas for 20 sec | 6.28 |
| C | Annealing in diluted $N_2O/N_2$=1/2 gas for 20 sec | 6.77 |
| D | Annealing in diluted $N_2O/N_2$=1/1 gas for 10 sec | 7.15 |

800 °C in a diluted $N_2O$ rapid thermal annealing (RTA) treatment, as listed in Table I. A 3000 Å poly-Si film was deposited by LPCVD and doped with $POCl_3$ at 900 °C for 30-min. An Al metal film of 5000 Å was deposited on the wafer by a thermal coater. The gate of metal–oxide-semiconductor (MOS) capacitor was defined by lithography, then the Al and poly-Si films were etched by wet etch chemistry. A 5000 Å Al film was also deposited on the backside of wafers after stripping the oxide on the backside. Finally, all the samples were sintered at 400 °C for 30 min in an $N_2$ ambient to form a good ohmic contact. Gate dielectrics of MOS capacitors with an area of $10^{-4}$ cm$^2$ were measured. NMOSFET transistors are fabricated using standard manufacturing with condition $D$. Using the spectroscopic ellipsometer, the thickness of ultrathin $Si_3N_4$ film was determined. The equivalent oxide thickness ($E_{OT}$) was determined from $C$–$V$ in strong accumulation region considering quantum mechanical effects. To double check, the physical thickness was obtained by TEM to determine the dielectric constant. The electrical properties and reliability characteristics of MOS capacitors were measured by using the Hewlett-Packard (HP) 4156B semiconductor parameter analyzer.

## III. RESULTS AND DISCUSSION

Fig. 1(a) shows high-frequency $C$–$V$ curves of oxynitride films of different thickness. The thickness of oxynitride film increases as the amount of $N_2O$ gas increases. This implies that $N_2O$ gas can reoxidize the silicon. The $V_{FB}$ values ($V_{FB} \cong -0.83$ V $\sim -0.95$ V) with different $C_{OX}$ imply less amount of fixed charge in these films. Since positive fixed charges in conventional $Si_3N_4$ film is due to N–H bonds at the interface [14]–[16], $N_2O$ oxidation of $NH_3$-nitridation $Si_3N_4$, removes H effectively and regrows the ultrathin interfacial oxide layer, which leaves negligible amount of positive fixed charge in oxynitride film [17]. A hump is exhibited in the depletion region of $C$–$V$ characteristics when $NH_3$-nitridation $Si_3N_4$ samples $N_2O$ are annealed in condition B. This could be explained by the fact that $N_2O$ annealing in condition B results in insufficient the oxygen concentration, which will leave bulk traps in this film. This phenomenon will be shown in Fig. 2(a). Negligible amount of hysteresis ($\Delta V_{FB} \cong 4.5$ mV) is observed in oxynitride film as shown in Fig. 1(b). Because $N_2O$ exhibits strong oxidizing capability, $N_2O$ annealing is more effective to passivate defects in $NH_3$-nitridation $Si_3N_4$ film. From SIMS data shown in Fig. 2(a) and (b), $N_2O$ annealing in condition D of $NH_3$-nitridation $Si_3N_4$ results in adequate amount of the Si–N and oxygen concentration, which shows a high dielectric constant and negligible amount of bulk trap densities.



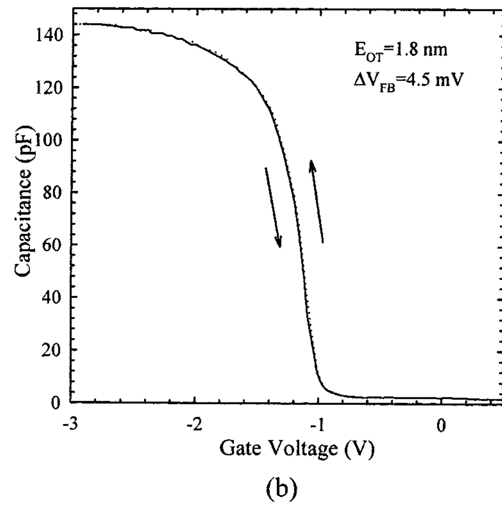




Fig. 1. (a) High frequency of $C$–$V$ curves of a 15 Å $Si_3N_4$ film with annealing at 800 °C in various conditions. (b) Hysteresis characteristics of oxynitride film annealed by condition D in Table I.

Fig. 3 shows the TEM image. It is found that $N_2O$ oxidation of $NH_3$-nitridation $Si_3N_4$/Si interface is very smooth. Such data also allows us to determine the physical thickness, when combined with our $C$–$V$ data, enables us to determine the relative dielectric constant of this nitride as being in range of 6.5–7.15, as listed in Table I. Mao [18] reported that angle-resolved XPS data of oxynitride film indicated an ultrathin (<10 Å) pure $SiO_2$ layer was formed between $Si_3N_4$ and Si after $N_2O$ oxidation. This suggests that the nitrogen be removed away from the $SiO_2$/Si interface during $N_2O$ oxidation. This result is the first time that a nitride/oxide stack layer is realized by low budget of thermal growth process.

The $J$–$V$ curves of oxynitride films with $E_{OT}$ are shown in Fig. 4. Significant reduction of leakage currents is obtained. It is found that sample with $E_{OT} = 18$ Å annealed in 800 °C shows a slightly lower leakage current than pure thermal oxide with $T_{OX} = 21$ Å. Effective nitrogen incorporation from $NH_3$-nitridation $Si_3N_4$ film increases dielectric constant, which allows physically thicker film with $E_{OT}$ to suppress the direct tunneling leakage current of $SiO_2$. Since in the conventional

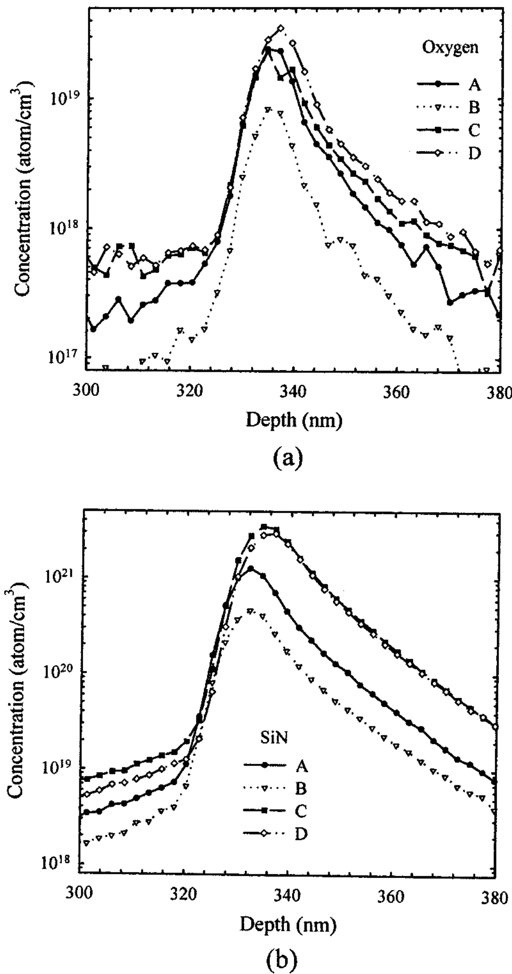



Fig. 2. (a) Oxygen and (b) SiN profiles at the oxynitride film after annealing at 800 °C in various conditions by SIMS measurement.

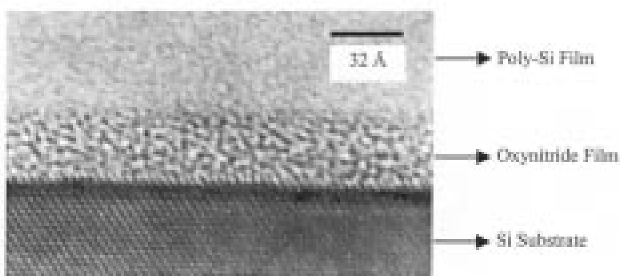



Fig. 3. TEM cross section view of $Si_3N_4$/Si stack film annealing at 800 °C in condition C for 20 s.

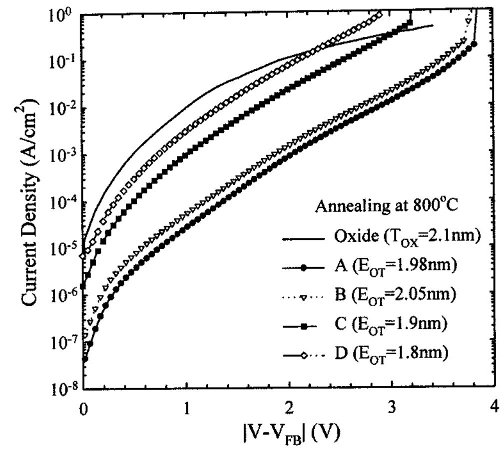
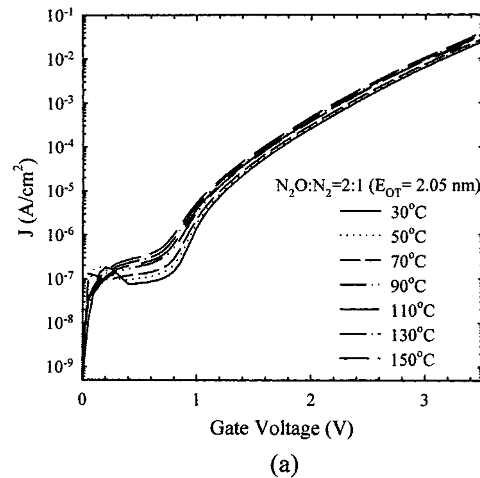



Fig. 4. $J$–$V$ characteristics of pure thermal oxide and a 15 Å $Si_3N_4$ films of $E_{\rm OT}$ with annealing at 800 °C in various conditions.



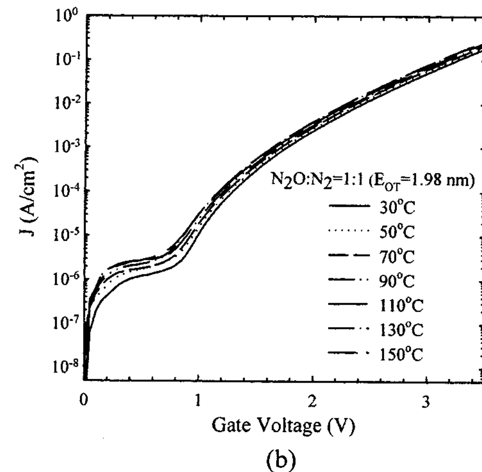
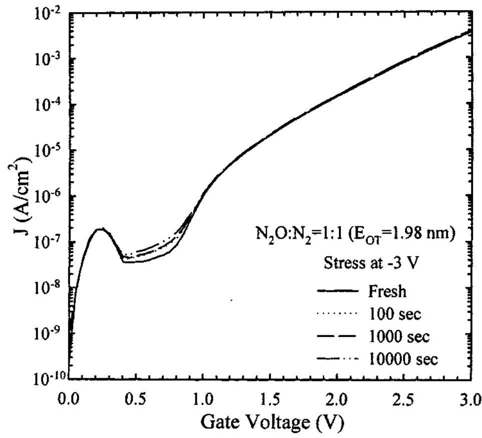




Fig. 5. $J$–$V$ characteristics at various temperatures for oxynitride film annealed at 800 °C in condition (a) A and (b) B.

CVD silicon nitride the dominant current component is due to the Frenkel–Poole (F–P) conduction mechanism, it is very interesting that $N_2O$ oxidation of $NH_3$-nitridation $Si_3N_4$ shows Fowler–Nordheim (FN) tunneling mechanism ($\phi_B = 2.2$ eV). We believe the limited of traps in this oxynitride film is probably responsible for this, because the F–P conduction requires a high density of traps. The fact that the dominant conduction mechanism in this oxynitride is tunneling is also verified by its relatively weak temperature dependence, as shown in Fig. 5(a) and (b).

Fig. 6(a) shows the result after constant voltage stress at $-3$ V for sample with $E_{\rm OT} = 19.8$ Å annealed at 800 °C. No significant SILC was observed after $10^4$-s stressing. In Fig. 6(b), it shows the sample after different constant voltages stressing during $10^3$-s stressing. No significant SILC increase of leakage current was showed for these samples also. The



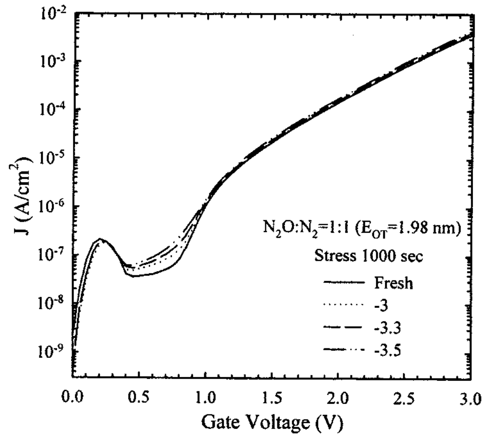




Fig. 6. SILC under constant voltage stress during different (a) voltage stress and (b) time stress for oxynitride film annealed at 800 °C.

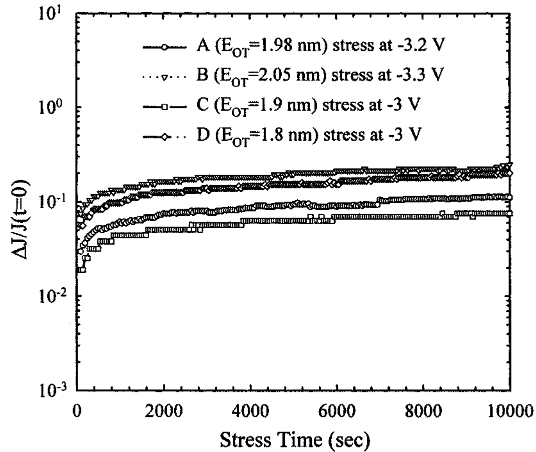



Fig. 7. $\Delta J/J(t=0)$ versus stress time plots of oxynitride film annealing at 800 °C in various conditions.

very lower SILC for this oxynitride can again be attributed to lower current fluence during the constant voltage stressing, which in return causes less trap generation and thus a very lower SILC. Fig. 7 shows gate current ($\Delta J/J(t=0)$, where $\Delta J = [J(t) - J(t=0)]$) for different constant voltage stressing after $10^4$-s stressing. No significant charge trapping

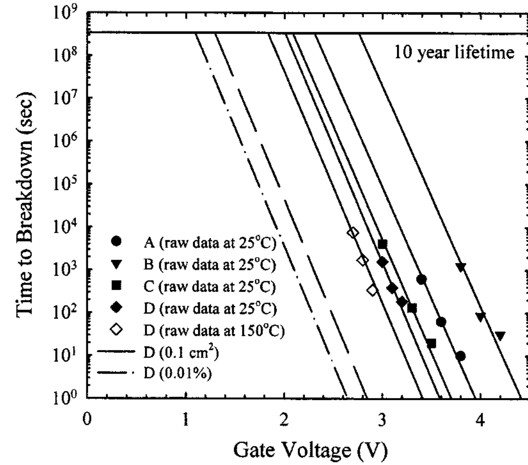



Fig. 8. Comparison of intrinsic lifetime projection for oxynitride film annealed at 800 °C in different conditions. Illustration of loss in the maximum operating voltage by temperature acceleration, scaling to effective area, and calculation 0.01% failure for condition D.

occurred during stress. Recently, gate oxide failure is reported to be a limiting factor for scaling of oxide thickness, since time-to-breakdown decreases exponentially with increasing gate leakage current [19]. Due to its significant reduction of lower leakage current, oxynitride film can extend the scaling limit of $SiO_2$ in terms of dielectric reliability as well as stand-by power consumption. In Fig. 8, the cumulative impact of area scaling, 0.01% failure rate, and temperature acceleration in ten years is evaluated [20]. For condition D annealed at 800 °C, figures drawn well fit to the measured time-to-breakdown ($T_{BD}$) at room temperature and 150 °C. The area scaling is calculated by assuming a Weibull distribution (63% value) with a random distribution of breakdown sites [21], [22]. The 150 °C-data have been a scaling of $10^{-4}$ cm$^2$ to 0.1 cm$^2$, and finally the 0.01%-line was calculated from the 150 °C-data. The maximum operating voltage could be as high as 1.1 V in these conditions. The longer time-to-breakdown ($T_{bd}$) for the oxynitride film is primarily attributed to its lower leakage current, which causes less damage to the dielectric and thus contributes to a longer dielectric lifetime.

Fig. 9(a) shows a family of drain current curves of an nMOSFET transistor while Fig. 9(b) shows the corresponding transconductance and current at $V_d = 0.1$ V characteristics. The oxynitride device exhibits high drain current and high transconductance (724 $\mu$S).

## IV. Conclusions

The ultrathin oxynitride (18–21 Å) dielectric films were produced by $N_2O$ oxidation of $NH_3$-nitridation $Si_3N_4$. Such films exhibit substantially lower leakage current than their thermal oxide counterparts. TEM image shows very smooth oxynitride/Si interface. The current transport properties in the oxynitride film differ significantly from those in conventional CVD silicon nitride film. The FN tunneling instead of F–P conduction dominates the current transport in the oxynitride film, which weakens the temperature dependence.

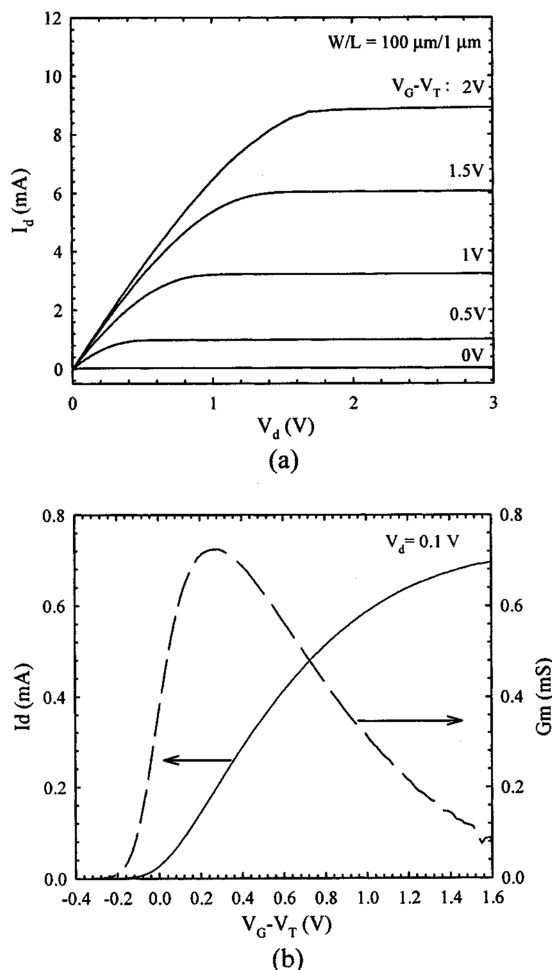



Fig. 9. (a) $I_d - V_d$ characteristics of oxynitride. (b) Gm and $I_d - V_g$ characteristic of oxynitride for nMOSFET.

The long $T_{bd}$ in the oxynitride film is attributed to its low leakage current, which causes less damage to the dielectric. Constant voltage stressing and SILC measurements indicated that there is very little charge trapping and trap generation in the oxynitride film. These results suggest that the oxynitride film may be considered as a potential candidate for alternative gate dielectric after thermal oxide in the upcoming generations of ULSI applications.

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