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Electrical and Compositional Properties of Co-Silicided Shallow p^+-n Junction Using Si-Capped/Boron-Doped $Si_{1-x}Ge_x$ Layer Deposited by UHVCME

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Co-silicided, strained boron-doped $Si_{1-x}Ge_x$ p^+/n junction with different Ge mole fractions deposited by ultrahigh vacuum chemical molecular epitaxy (UHVCME), suitable for raised source/drain metal oxide semiconductor field effect transistor applications, is studied. The electrical and compositional characteristics are presented. By using a Co/Si-cap/graded $Si_{1-x}Ge_x$ structure, optimum forward and reverse diode characteristics with a near perfect forward ideality factor (*i.e.*, <1.01) can be obtained for the p^+-n junction. The low area leakage current extracted from Si-capped samples confirms that serious lattice misfit problems during silicidation, typical of Co/pure $Si_{1-x}Ge_x$ samples, is largely eliminated by Si capping. In addition, the specific contact resistance is found to decrease as Ge mole fraction increases, and would be even lower if Si capping is used for silicidation. Finally, the composition of $Co/Si_{1-x}Ge_x$ and $Co/Si\text{-}cap/Si_{1-x}Ge_x$ interfacial reaction is studied by high-resolution X-ray spectra. Our results show that even after a second anneal at 850°C, very little lattice distortion is discovered. Five harmonic peaks still remain even after a second anneal at 850°C. Transmission electron micrograph also exhibits good uniformity and interface quality.
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The heterojunction bipolar transistor (HBT) with $Si_{1-x}Ge_x$ base has been extensively studied due to its potential advantage of overcoming the conflicting requirements between base resistance and transit time, a limitation which has plagued the conventional homojunction bipolar transistors.[1-3] The silicided SiGe layer has also been proposed for fabricating a raised source/drain region of metal-oxide-semiconductor (MOS) field-effect transistor, as well as for optical device applications.[4,5] By adding Ge to the strained $Si_{1-x}Ge_x$ layer, the cutoff wavelength can be extended.[6] Concurrently, with the recent surge in research interest of sub-0.1 μm complementary MOS (CMOS) technologies, the formation of shallow p^+ source/drain (S/D) junction with low contact resistivity has received particular research attention. One of the most effective ways to form a shallow p^+ S/D junction is to use selective epitaxy growth (SEG) for $Si_{1-x}Ge_x$ on the exposed S/D active area.[7-10] This results in a self-aligned raised S/D structure which is beneficial in reducing the effective junction depth and contact resistivity.

Significant efforts have thus been made to understand the phase formations and properties of metal/$Si_{1-x}Ge_x$ reactions.[11-23] Among the potential metal silicides, $CoSi_2$ is particularly attractive for its low resistivity, cubic crystal structure, relatively small lattice mismatch with Si, and its compatibility with self-aligned silicide (SALICIDE) scheme. In the past few years, the reaction of the Co/strained-$Si_{1-x}Ge_x$/Si system has been actively studied.[16,17,20-23] The compound formation after thermal treatment and the stability of the strained $Si_{1-x}Ge_x$ layer during silicide formation were investigated. For high-speed device applications, $Si_{1-x}Ge_x$ layer is usually heavily doped. The effects of the high dopant concentration on the Co silicidation process with Si or $Si_{1-x}Ge_x$, and the redistribution of dopants during silicidation were studied.[22,24,25] A significant accumulation of Ge between the unreacted SiGe and the silicided region was observed on the boron-doped $Si_{0.8}Ge_{0.2}$ samples, suggesting that the redistributions of B and Ge occur.

Since undesirable SiGe precipitants and the resultant dislocations occurred for direct reaction between Co and $Si_{1-x}Ge_x$, Co silicidation by using Si as sacrificial layer on top of $Si_{1-x}Ge_x$ film have been studied to achieve better metal silicide/$Si_{1-x}Ge_x$ interface.[26,27] However, a detailed study of Ge ratio on electrical and compositional characteristics of Co/Si-cap/SiGe SEG p^+/n diode were not available in the literature.

The present paper examines the electrical and compositional properties of Co-silicided SEG $Si_{1-x}Ge_x$/Si p^+-n heterojunction diodes by using ultrahigh vacuum chemical molecular epitaxy (UHVCME) deposited $Si_{1-x}Ge_x$ layer with different Ge mole fractions (*i.e.*, $=x$). The diodes were fabricated on silicon wafers containing oxide patterns. In addition to being a low temperature process, UHVCME is also known to be advantageous in minimizing the impurity contamination due to its low base pressure. This study thus paves the way for future device applications of $Si_{1-x}Ge_x$ heterojunction bipolar transistor and advanced MOS transistors using a raised silicided $Si_{1-x}Ge_x$ source/drain.

Experimental

n-Type 6 in. silicon (100) wafers of 10-15 Ω cm were used as the starting substrates. The exposed active regions were first defined by patterning and etching a 300 nm isolation oxide. Then, following a standard RCA clean and a 1:50 HF:H_2O dip, 100 nm boron-doped $Si_{1-x}Ge_x$ (x = 0, 0.09, 0.14, and 0.2) layers, with or without a Si-capping layer, were selectively deposited using an UHVCME system.[28] Briefly, the growth chamber was pumped with a 1000 L/s turbomolecular pump to a base pressure of 2×10^{-10} Torr. Next, wafers were heated to the final deposition temperature of 550°C at a ramp rate of ~150°C/min. For growing boron-doped $Si_{1-x}Ge_x$ layer, pure Si_2H_6, GeH_4, and B_2H_6 were introduced into the growth chamber. For graded $Si_{1-x}Ge_x$ (for instance, $Si_{0.86}Ge_{0.14}$) structure, a 5 nm $Si_{1-x}Ge_x$ film with lower Ge mole fraction (*i.e.*, x = 0.03, 0.06, 0.09, 0.11) was grown before depositing the main $Si_{1-x}Ge_x$ (x = 0.14) layer. After a 900°C, 30 s activation anneal, wafers were loaded into a sputter deposition chamber for a 10 nm Co deposition. Next, a 30 nm thick TiN capping layer was deposited on top of the Co film to prevent metal oxidation and improve uniformity.[29,30] The $Co/Si_{1-x}Ge_x$ reaction was performed in a rapid thermal annealing (RTA) system equipped with high intensity halogen tungsten lamps. The RTA treatment was carried out in nitrogen ambient for 30 s at 450°C. After selectively removing the unreacted species by wet etching in $4H_2SO_4$:$1H_2O_2$ (30%) solution for 5 min, a second RTA was executed at 800°C for 30 s.

At this stage, some samples from each split were removed for structural, compositional, and planar sheet resistance measurements. The planar sheet resistance was measured by a conventional four-point probe system. While the structural and compositional properties of the reacted thin films were carefully examined by X-ray diffractometry (XRD), high resolution X-ray diffraction with high

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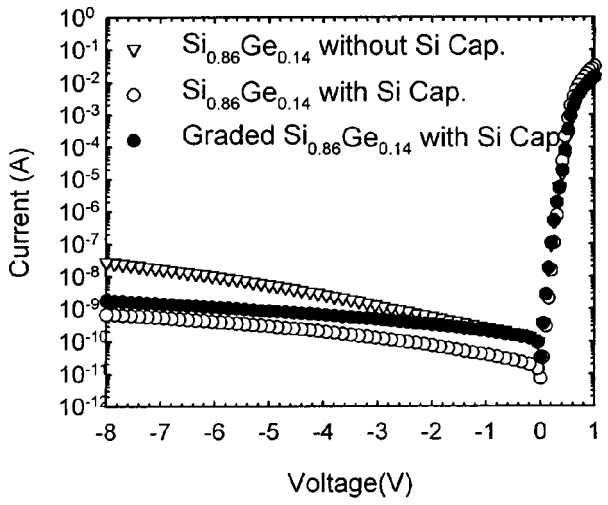

Figure 1. Forward and reverse characteristics for silicide/SiGe/Si p^+-n junction with and without Si cap. The diode area is 1000 × 1000 μm.

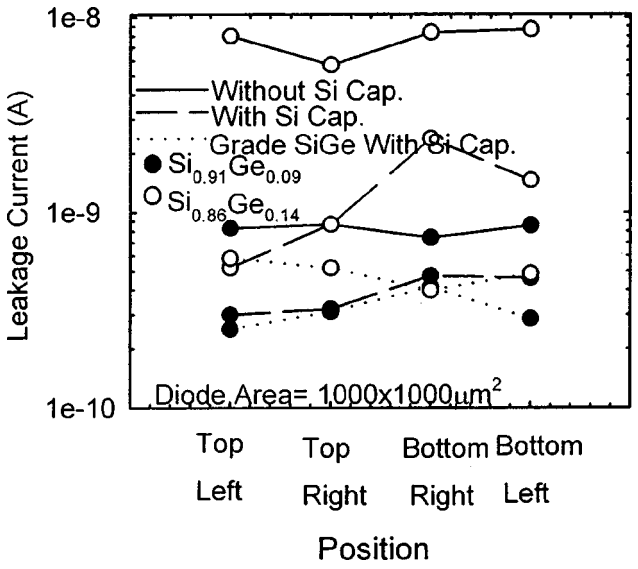

Figure 2. The reverse leakage current density (J_{OFF}) for $Si_{0.91}Ge_{0.09}$ and $Si_{0.86}Ge_{0.14}$ SEG diodes at −5 V at different position on a wafer with different structures (diode area: 1000 × 1000 μm).

energy X-ray beams, Auger electron spectroscopy (AES), and secondary ion mass spectroscopy (SIMS). The high resolution asymmetric θ-2θ X-ray diffraction measurements consist of a Huber Cu target source with a Si(111) crystal monochromator and a Ragaku scintillation NaI detector to detect the diffracted beams. The test sample was mounted in air at the center of the five-circle diffractometer axes. SIMS measurements were performed in a Cameca IMS5f apparatus. Finally, the morphologies of interfaces were analyzed using cross-sectional transmission electron microscopy (XTEM).

The rest of the wafers continued to receive a back-end passivation oxide. After contact opening, a TiN/Al-4%Cu/TiN/Ti four-layer metal was sputtered and patterned to form the metal interconnect. The electrical characteristics were measured by a HP4145B semiconductor parameter analyzer. The sheet resistance was also extracted using both the transfer length method (TLM) and cross-bridge resistor structure. While the contact resistance was measured by both TLM and Kelvin cross structures.

Results and Discussion

Electrical characteristics.—Figure 1 shows the forward and reverse current-voltage (I-V) characteristics of Co-silicided $Si_{0.86}Ge_{0.14}$ diodes with different structures (*i.e.*, with or without Si cap, conventional or graded $Si_{0.86}Ge_{0.14}$ structure). The $Si_{0.86}Ge_{0.14}$ layer thickness is 100 nm for all samples. It can be seen that the reverse leakage current (I_{OFF}) decreases significantly with the use of a 35 nm Si-cap structure. Moreover, I_{OFF} could be reduced even further with Si cap/graded SiGe structure. This is confirmed again on the leakage current measured at −5 V as a function of diode position on a wafer, as shown in Fig. 2. The depth of all the junctions were all deeper than 45 nm based on SIMS analyses, as the depth was defined when B equals 2×10^{17} cm^{-3}.[31,32] A large I_{OFF} for the pure $Si_{0.86}Ge_{0.14}$ diode is believed to be due to the large misfit dislocations caused by $Co/Si_{1-x}Ge_x$ ternary phase reaction. This is further confirmed by extracting the area component of the leakage current, J_A, by calculating diodes with different areas and peripheries. The resultant J_A as a function of Ge mole fraction for various diode structures is shown in Fig. 3. It can be seen that diodes without Si-cap layer exhibit the highest area leakage current, and the area leakage current increases dramatically with Ge mole fraction. In contrast, the graded structure with Si-cap depicts the lowest area leakage current. Moreover, the area leakage current dependence on the Ge mole fraction is significantly reduced. Because the area leakage current represents the degree of defects and dislocations extended to the junction interface, the above results confirm that the large I_{OFF} for the pure $Si_{0.86}Ge_{0.14}$ diode is indeed caused by large misfit dislocations of $Co/Si_{1-x}Ge_x$. A graded structure could further alleviate the defect problem during epitaxial process, especially for samples with large Ge ratio.

For forward bias condition, as also shown in Fig. 1, the Si cap/graded $Si_{0.86}Ge_{0.14}$ diode depicts the highest forward current among all splits, especially at a high current level. This is consistent with a lower contact resistance as a result of smaller dislocation density due to reduced $Si_{1-x}Ge_x$ lattice stress. The forward ideality factor *vs.* Ge composition for Co-silicided $Si_{0.86}Ge_{0.14}$ diodes with different structures is plotted in Fig. 4. As Ge composition increases, the ideality factor in general increases due to worsened junction quality caused by larger misfit dislocations associated with increased amount of Ge atoms. With the addition of a Si-capped layer for Co silicidation (*i.e.*, 35 nm Si layer for 10 nm Co film), the underlying SiGe layer could remain intact. So the ideality factor is determined mainly by the quality of SiGe epitaxy. Furthermore, with the graded

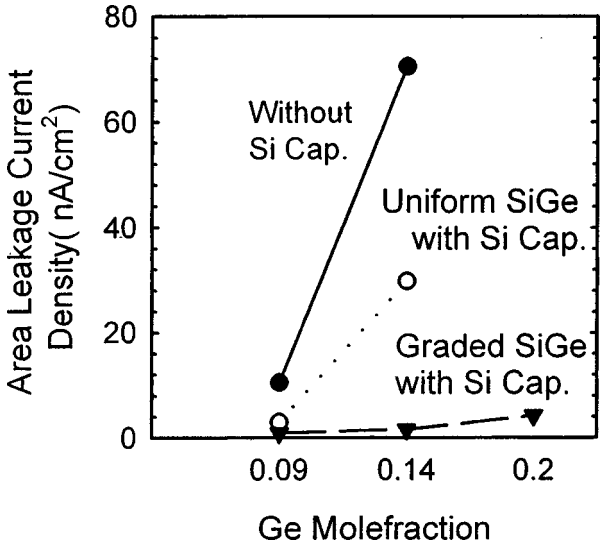

Figure 3. The extracted area leakage component J_A *vs.* Ge composition for SEG diodes with different structures.

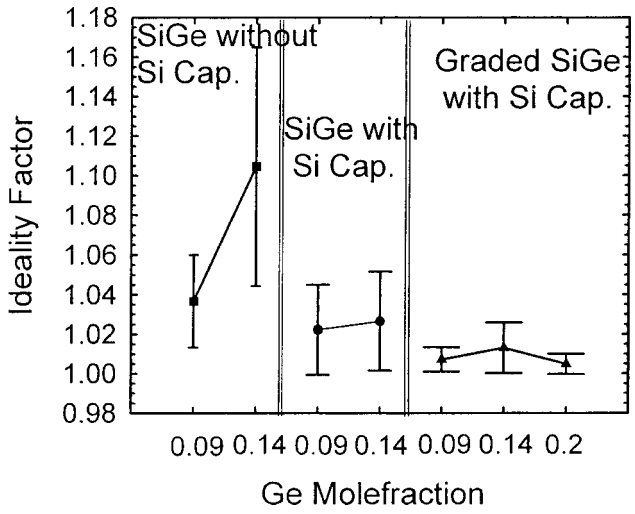

Figure 4. Forward ideality factor *vs.* Ge composition for different SEG diode structures.

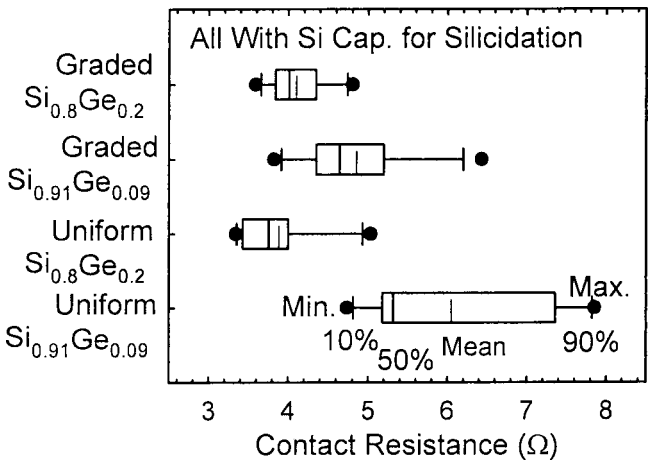

Figure 6. The calculated specific contact resistivity by cross-bridge Kelvin resistor (CBKR) method for samples with different Ge mole fractions and epitaxial structures.

$Si_{1-x}Ge_x$ structure, the mean and deviation of ideality factor could be further improved, because of better lattice quality. An ideality factor of less than 1.005 can be achieved under such a condition.

The mean and deviation of sheet resistance (ρ_S) measured by cross-bridge resistors of each sample as a function of Ge mole fraction are plotted in Fig. 5. It can be seen that for diodes without a Si cap, sheet resistance increases sharply with increasing Ge mole fraction, due to incomplete transformation to $CoSi_2$ during the second RTA anneal at 800°C. This is contrary to previous reports that low-resistivity $CoSi_2$ is formed at 800°C for a plane $Co/Si_{0.86}Ge_{0.14}$ reaction.[22] It could be that the reaction of $Si_{1-x}Ge_x$ silicidation at small or narrow area (*e.g.*, 10 × 500 μm in this study) is blocked by the Si-Ge-Co ternary phase. In order to complete the transformation to $CoSi_2$, the second RTA temperature has to be increased to 900°C for non-Si-capped $Si_{0.86}Ge_{0.14}$ diodes. On the contrary, successful $CoSi_2$ transformation is evidently achieved for Si-capped samples with 800°C anneal, irrespective of the Ge mole fraction. This is evidenced by the low sheet resistance value of 6.7 Ω/□ obtained. From these results, it is essential that Ge atoms be prevented from incorporating into the silicide reaction, as Ge would cause precipitation and retard the reaction.

Measurement of specific contact resistance (R_C) was performed using cross-bridge Kelvin resistors. The results are summarized in Fig. 6. Theoretically, the barrier height (φ_{BP}) formed at a metal/semiconductor interface is known to be a critical factor in determining the contact resistivity (ρ_C). The work function difference between $p^+Si_{1-x}Ge_x$ and p^+Si, due to their energy bandgap difference, results in a lower Schottky barrier height (SBH) for metal/$p^+Si_{1-x}Ge_x$ junction, compared to that of metal/p^+Si junction.[33] For pseudomorphic p-$Si_{0.86}Ge_{0.14}$ layer, the SBH is expected to be lower than that of metal/p^+Si by 0.07 eV, thus effectively reducing the specific contact resistivity (ρ_C). From Fig. 6, the contact resistance indeed decreases as Ge relative ratio changes from 0.09 to 0.2, as predicted. A minimum ρ_C value of 3.38×10^{-2} μΩ cm^2 is observed for the $Si_{0.8}Ge_{0.2}$ sample. Furthermore, by employing graded structure, the distribution of both sheet resistance and contact resistance would become more uniform with smaller deviation.

Comparison between Co/$Si_{1-x}Ge_x$ and Co/Si-cap/$Si_{1-x}Ge_x$ reaction.—Figure 7 shows the dependence of planar sheet resistance, measured by four-point probe, on the RTA temperature for

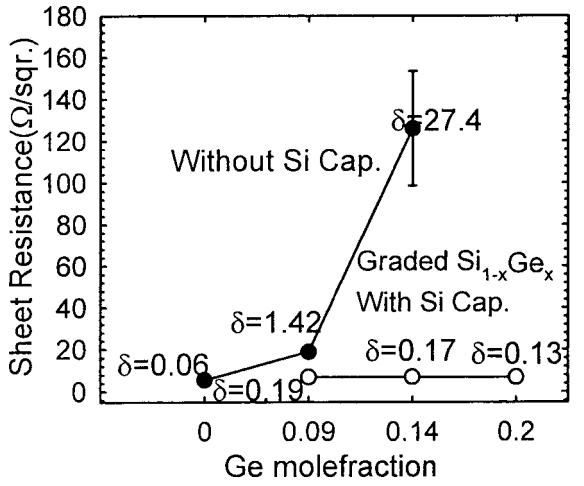

Figure 5. Sheet resistance *vs.* Ge mole fraction measured by cross-bridge resistors with or without Si sacrificial layer.

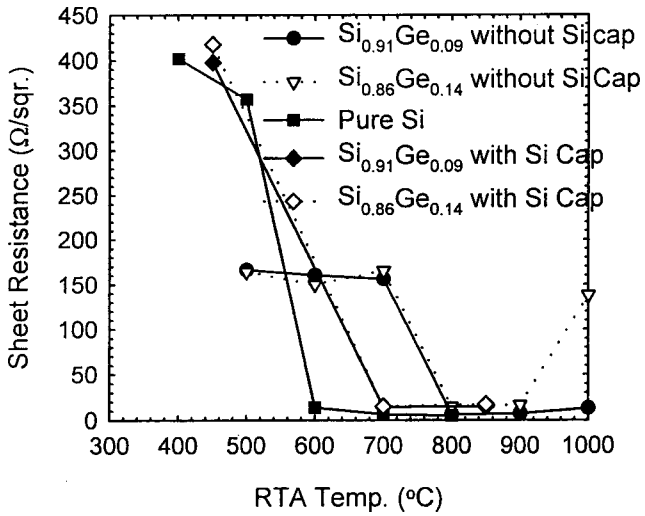

Figure 7. Planar sheet resistance *vs.* RTA temperature for Co (80 Å) film on various SiGe samples with and without Si-capping. The annealing time is 30 s.

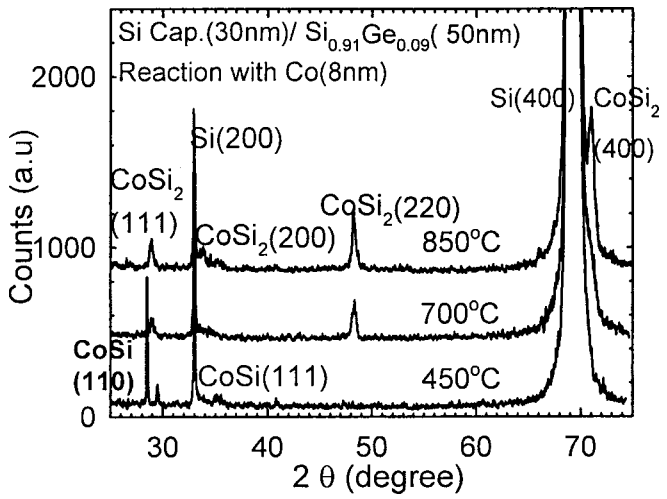

Figure 8. XRD spectra of 80 Å Co deposited on 30 nm Si-cap/50 nm $Si_{0.91}Ge_{0.09}$ layer after first anneal at 450°C for 30 s, and after another anneal at 700 or 850°C for 30 s.

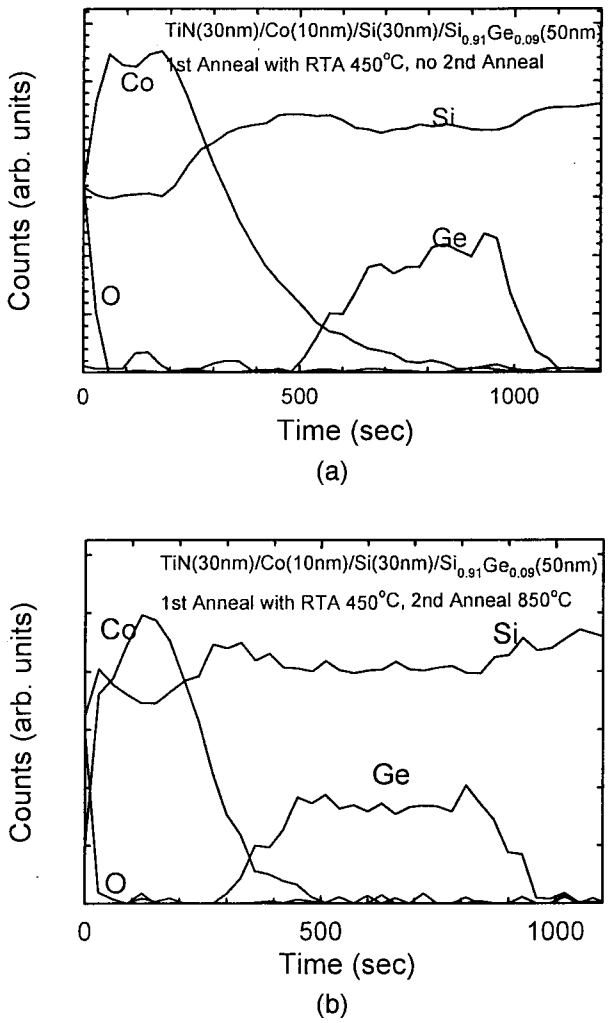

Figure 9. AES depth profiles of Co (80 Å)/Si-cap/$Si_{0.91}Ge_{0.09}$ sample after (a) 450°C, 30 s for 1st step, and (b) 850°C, 30 s for 2nd step annealing.

samples with Co(10 nm)/$Si_{1-x}Ge_x$(100 nm), and Co(10 nm)/Si-cap(30 nm)/$Si_{1-x}Ge_x$(50 nm) structures. The conventional Co/pure-Si samples were also measured for comparison. The Co(10 nm)/Si-cap (30 nm)/SiGe (50 nm) samples behave similarly to pure Co/Si samples. Specifically, at lower RTA temperature (*i.e.*, 500°C), while Co/$Si_{1-x}Ge_x$ samples exhibit a lower value due to CoGe phase formation with lower resistivity, both Co(10 nm)/Si-cap (30 nm)/SiGe (50 nm) and pure Co/Si samples exhibit a much higher sheet resistance. However, at intermediate temperatures (*i.e.*, 600 and 700°C), $CoSi_2$ phase has already been formed for Co/pure-Si and Co/Si-cap(30 nm)/$Si_{1-x}Ge_x$ samples, as is confirmed from the X-ray diffraction spectra, so the sheet resistance value reduces sharply to a very low value. With a Si-cap layer, the Co/Si-cap/$Si_{1-x}Ge_x$ sample is immune to the problem caused by SiGe segregation to the Co/$Si_{1-x}Ge_x$ reaction interface that blocks $CoSi_2$ silicidation.[22] Finally, the sheet resistance of all samples is reduced to less than 15 Ω/□ after annealing at 800 and 900°C, indicating that CoSi has been converted to the $CoSi_2$ phase eventually for all samples.

The phase formation sequence during Co reaction with Si-cap/$Si_{1-x}Ge_x$ and the crystallographic orientation of silicide were monitored by symmetric X-ray diffraction in the θ-2θ geometry. Figure 8 shows the undoped Co/Si-cap/$Si_{0.91}Ge_{0.09}$XRD spectra with the first anneal at 450°C and the second anneal at either 700 or 850°C. We can see that with 450°C RTA, the predominant phase is CoSi(110) and (111), because Co_2Si phase is removed during the selective wet etching of TiN/Co film. After the second annealing at 700°C, disilicide phases can be identified already. At 850°C, the intensity of each $CoSi_2$ phase becomes even stronger. In addition, the (400) orientation of the disilicide phase is very pronounced at 850°C, compared to other diffraction peaks in XRD spectra. This indicates that the main crystal orientation of $CoSi_2$(400) is the same as that of the $Si_{1-x}Ge_x$ epitaxy and Si substrate.

Figure 9a and b shows the AES depth profiles for Co/Si-cap/$Si_{0.86}Ge_{0.09}$ layers after annealing at 450°C and another annealing at 850°C for 30 s, respectively. Figure 9a exhibits a uniform layer of Co, Si and Ge on top of $Si_{1-x}Ge_x$ layer for samples which have undergone RTA at 450°C for 30 s, indicating a CoSi phase formation. After the second anneal at 850°C for 30 s, the Co/Si-cap/$Si_{1-x}Ge_x$ sample was fully converted to the $CoSi_2$ phase, as shown in Fig. 9b. The amount of Co atoms in the silicided region decreases, as compared with the sample annealed at 450°C only. In addition, Co atoms distributed over the Si cap region uniformly. No accumulation phenomenon was observed for Si or Ge atoms in Co silicide or $Si_{1-x}Ge_x$ layer. On the other hand, Ge accumulation was observed in the middle of the reacted Co/$Si_{1-x}Ge_x$ layer for the Co/pure $Si_{1-x}Ge_x$ reaction at 700 and 900°C.[22] Certain Ge accumulation is expected to be the Ge-rich $Si_{1-z}Ge_z$ precipitants ($z > x$) agglomerating around silicide grain boundaries.[22]

SIMS depth profiles for Co/Si-cap/boron-doped $Si_{0.86}Ge_{0.14}$ samples after first anneal at 450°C and second anneal at 850°C are shown in Fig. 10a and b, respectively. For the sample with 450°C-only RTA annealing (Fig. 10a), a surface accumulation of boron is found. Additionally, a peak of about 2×10^{18} cm^{-3} boron atoms is accumulated at the upper Co/$Si_{1-x}Ge_x$ reaction region for sample which received a second anneal at 850°C, as shown in Fig. 10b. The reason for boron pileup may be the low solubility of boron in crystalline Co silicides ($\sim 5 \times 10^{19}$ cm^{-3}). Thus boron atoms could be pushed out from the Co/$Si_{1-x}Ge_x$ or Co/Si silicide region and nucleate at the upper grain boundary region.

Figure 11 demonstrates the high-resolution XRD (400) asymmetric θ-2θ spectra of Co/Si-cap/$Si_{0.8}Ge_{0.2}$ layer after first annealing at 450°C, and after a second annealing at 700 and 850°C, respectively. The reaction of Co with $Si_{1-x}Ge_x$ layer would cause some changes in $Si_{1-x}Ge_x$ structure quality such as lattice mismatch. The resultant lattice relaxation of the underlying $Si_{1-x}Ge_x$ layer would cause some shift of the $Si_{1-x}Ge_x$(400) peak in the XRD spectra toward the Si(400) peak, and at the same time, would broaden the bandwidth of

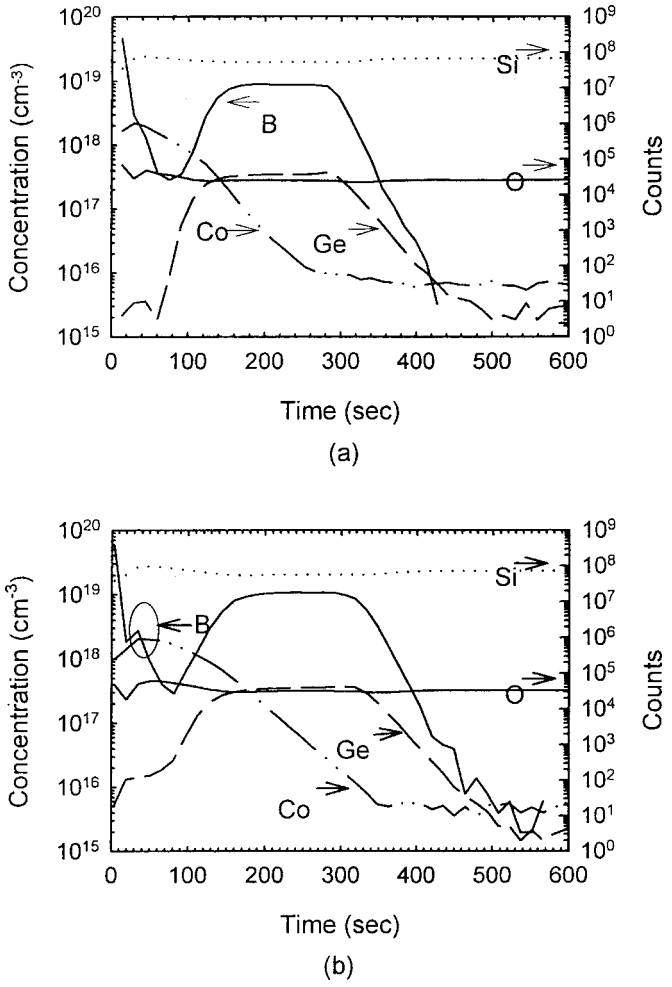

Figure 10. SIMS depth profiles of Co (10 nm)/Si-cap/$Si_{0.86}Ge_{0.14}$ (50 nm) sample after (a) 1st step at 450°C and (b) 2nd step at 850°C annealing for 30 s.

the SiGe(400) peak. Besides, the harmonic peaks may vanish at the same time. However, as could be seen in Fig. 11, no specific movement for SiGe(400) was discovered, irrespective of the annealing temperature. Five harmonic peaks still remain even after a second

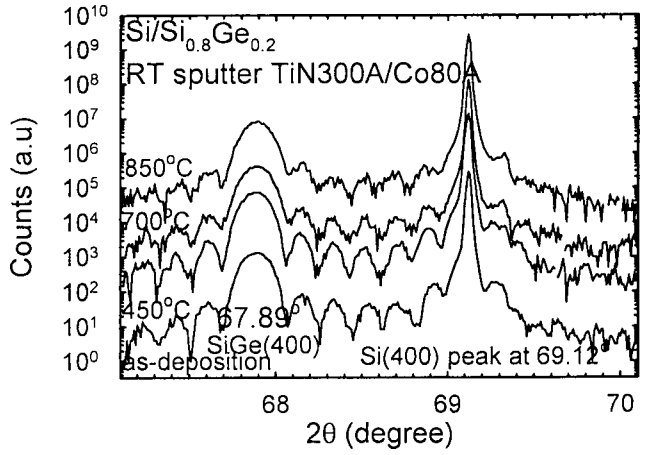

Figure 11. High-resolution XRD spectra of Co film deposited on $Si_{0.8}Ge_{0.2}$ layers with a Si sacrificial layer after annealing at different temperatures for 30 s.

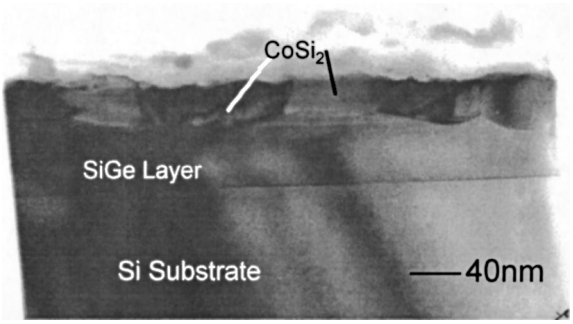

Figure 12. XTEM micrograph of Co (10 nm)/Si-cap(30 nm)/$Si_{0.86}Ge_{0.14}$ (50 nm) sample after a first anneal at 450°C for 30 s and a second anneal at 800°C for 30 s.

anneal at 850°C. However, remarkable differences in harmonic peaks could be found after samples were annealed at various temperature stages. The reason should be the total consumption of the Si cap layer, which could be proved by TEM micrographs. The reaction front of the silicidation process touches the strained SiGe layer, and defect problems will occur. The longer the reaction with the strained SiGe layers the higher the relaxation level, due to generation of dislocations. Similar results are also obtained for Co/Si-cap/$Si_{0.91}Ge_{0.09}$ and Co/Si-cap/$Si_{0.86}Ge_{0.14}$ samples (data not shown).

The cross-sectional view of Co/Si-cap/$Si_{0.8}Ge_{0.2}$ interface which received a first anneal at 450°C and a second anneal at 800°C is shown in Fig. 12. A smooth $CoSi_2$ surface layer with an almost intact $Si_{0.86}Ge_{0.14}$ underlayer could be found. The size of CoSi grains is nearly identical to that shown in Fig. 12. No dislocation line or any nucleation could be found around silicide grain boundaries. Nevertheless, in order to achieve low specific contact resistivity, the Si-cap layer must be totally consumed to make good Co silicide/$Si_{0.86}Ge_{0.14}$ contact directly. By carefully examining Fig. 12, Si sacrificial layer does not seem to be completely reacted in some region, and this would cause some fluctuations in the measured R_C.

Figure 13 is the TEM photograph of the Co/$Si_{0.86}Ge_{0.14}$ sample after 700°C RTA annealing. From XRD analysis, both CoSi and $CoSi_2$ phases can be found at this temperature, represented by the large grains in the upper region with a rough crystal distribution. The underlying $Si_{0.86}Ge_{0.14}$ layer is not totally consumed and is displayed as a line region in the TEM picture. Severe dislocations can be found to extend into the Si substrate, as is clearly shown in Fig. 13. Furthermore, some small decorations around the silicide grain boundaries are also found. It has been reported that these decorations are Ge-rich $Si_{1-z}Ge_z$ ($z > x$) alloys.[25,34] The $Si_{1-x}Ge_x$ layer had been damaged and silicidation would also destroy the Si substrate quality.

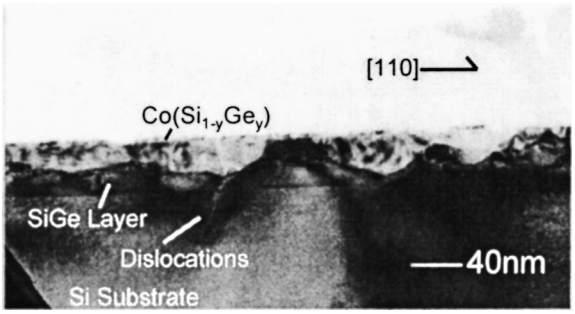

Figure 13. XTEM micrograph of Co/$Si_{0.86}Ge_{0.14}$ sample after 700°C RTA annealing for 30 s.

Conclusions

The electrical characteristics of Co-silicided Co/Si-cap/selective epitaxial growth of boron-doped $Si_{1-x}Ge_x$ shallow p^+/n diodes fabricated by UHVCME were reported. High forward current and low reverse leakage with a near perfect ideality factor (*i.e.*, <1.01) are obtained on diodes employing Co/Si-cap/$Si_{1-x}Ge_x$ graded structure. The strain problem, due to mismatch between $Si_{1-x}Ge_x$ and silicon substrate, is essentially eliminated by employing graded $Si_{1-x}Ge_x$ structure, even for samples with high Ge mole fraction. The specific contact resistance is found to improve with silicide using Si-cap as sacrificial layer. Furthermore, a detailed comparison on the Co reaction with strained $Si_{1-x}Ge_x$ were studied on samples with and without Si-cap. With Si-capping, excellent interface quality could be detected by high resolution XRD, AES, and TEM photography. In addition, undesirable SiGe precipitation and dislocations could be eliminated completely. Finally, a low $CoSi_2$ formation temperature, similar to that in a Co/pure-Si reaction, is necessary for the Co/Si-cap/$Si_{1-x}Ge_x$ structure. These results should be useful for future applications to heterojunction devices and advanced MOS transistors with a raised source/drain.

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